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Front End Readout Electronics of the MicroBooNE Experiment

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Content :

The MicroBooNE experiment is to build a ~100 ton Liquid Argon (LAr) Time Projection Chamber (TPC) detector that will observe interactions of neutrinos from the on-axis Booster Neutrino Beam and the off-axis NuMI Beam at Fermi National Accelerator Laboratory. The experiment will address the low energy excess observed by the MiniBooNE experiment, measure low energy neutrino cross sections, and serve as the necessary next step in a phased program towards massive Liquid Argon TPC detectors.

The MicroBooNE TPC will have 3 readout wire planes with a total of 8,256 wires/signal channels. All the signals will be pre-amplified, shaped, digitized and pre-processed online before being recorded for offline analysis of a wide variety of physics programs. To optimize the detector performance and signal-to-noise ratio, an analog front end ASIC designed in 180 nm CMOS technology will be deployed and operated in LAr. Pre-amplified and shaped detector signals will be differentially driven to ADC boards operated in the detector hall where signals will be digitized and prepared for online data pre-processing in FPGAs. We present here an overview of the front end readout architecture of the MicroBooNE experiment, describe the development of the front end readout electronics and preliminary test results.

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