

WIT2012 Workshop on Intelligent Trackers

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Use of Associative Memories for L1 triggering in LHC environment.

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Content :

Modern high energy physics experiments search for extremely rare processes hidden in much larger background levels. As the experiment complexity, the accelerator backgrounds and luminosity increase we need increasingly exclusive selections to efficiently select the rare events inside the huge background.

In the framework of the CMS experiment at LHC one of the identified challenges for future upgrade is the capability of using the tracker information to trigger events already at L1 (now they are used at L2).

This strategy requires massive computing power to minimize the online execution time of complex tracking algorithms and the “combinatorial challenge”.

Associative Memories (AM) have been already used in other experiments (CDF) as a way to compare the tracker informations of each event to pre-calculated “expectations” (pattern matching) in a very short time and contribute to the trigger decision. To use the AM approach for the CMS tracker one of the main challenges is to make available the tracker data to the AM processor in a very short time (6 ns is the L1 latency for CMS).

We describe a possible application of AM in the CMS environment using the existing hardware developed for other experiments, the AMBSlim mother board consisting of 4 smaller boards, the Local Associative Memory Banks (LAMB), each hosting 32 AM chips to contain the stored patterns with the readout logic. The ability of a single AMBSlim to process a single event is much less than the amount of input data foreseen for the CMS case, and the latency strongly depends on the time necessary to load the data in the AM system and to process a single event.

One possible solution is to parallelize the event processing inside the AMBSlim board assigning each event to one LAMB. We describe the firmware implementation of this concept in the current hardware and the results obtained.

Finally we discuss a possible modification of the LAMB hardware in order to obtain the minimum delay time for processing events.

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