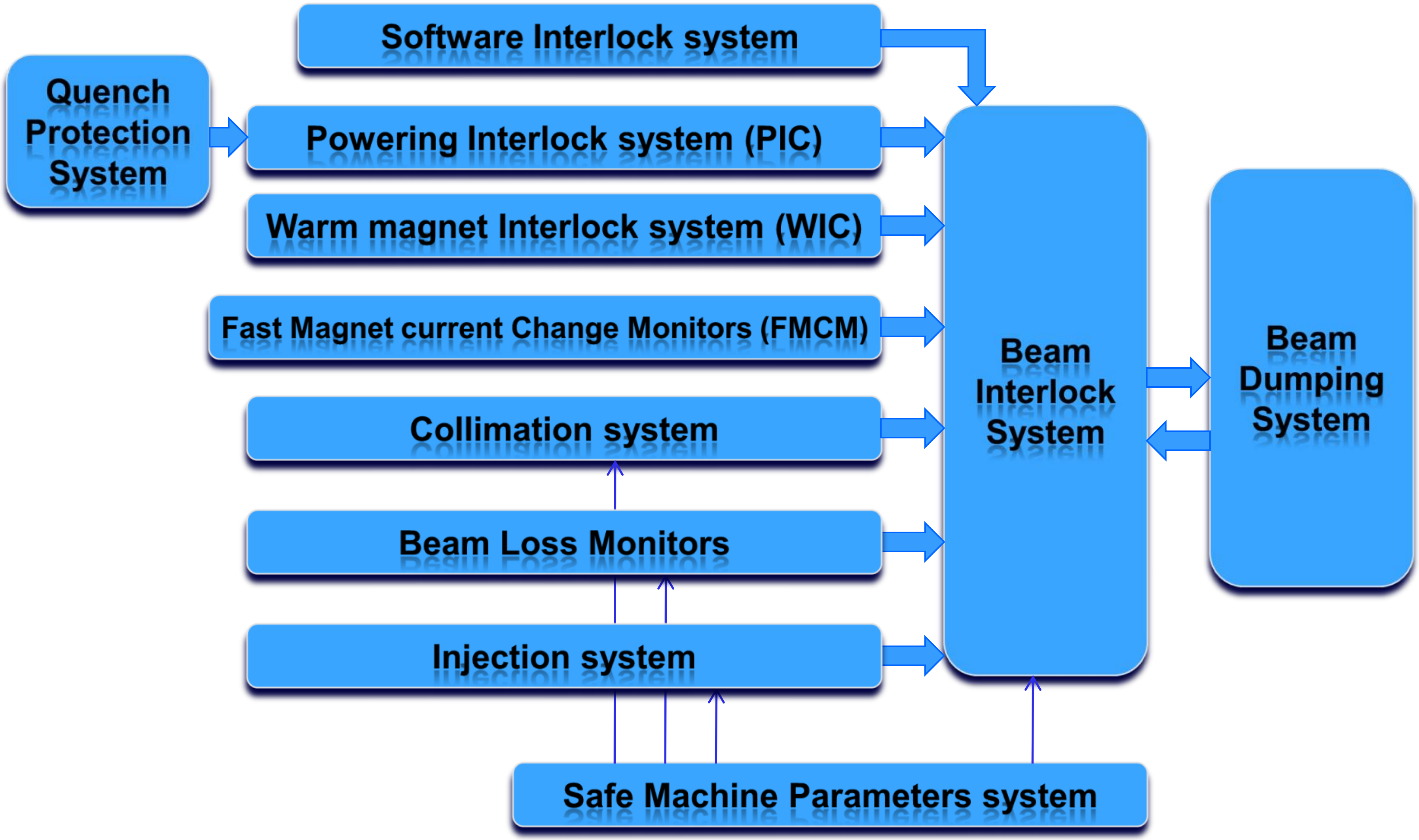
Overview of Beam Interlocking

B.PUCCIO & B. TODD

MP Review

6-8th Sept. 2010

Presentation in two parts:



Machine Protection systems

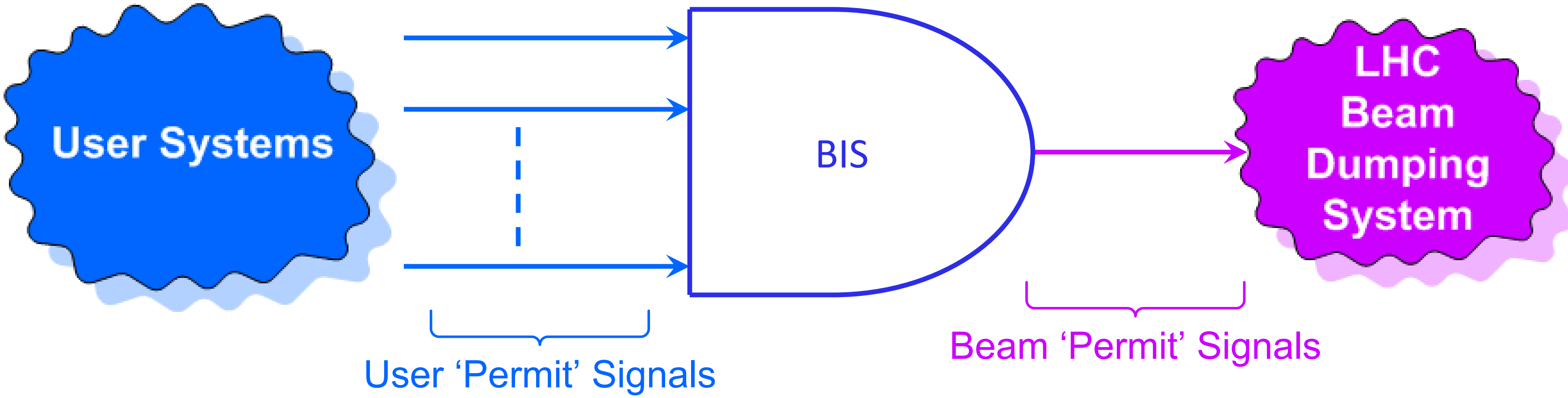
Beam Interlock System

Bruno PUCCIO

MP Review

6-8th Sept. 2010

Beam Interlock System Function



~200 inputs distributed over 27 kms

LHC has 2 Beams
Some User Systems give simultaneous permit → Both-Beam
Others give independent permit → Beam-1, Beam-2

Beam Permit Loops & BICs

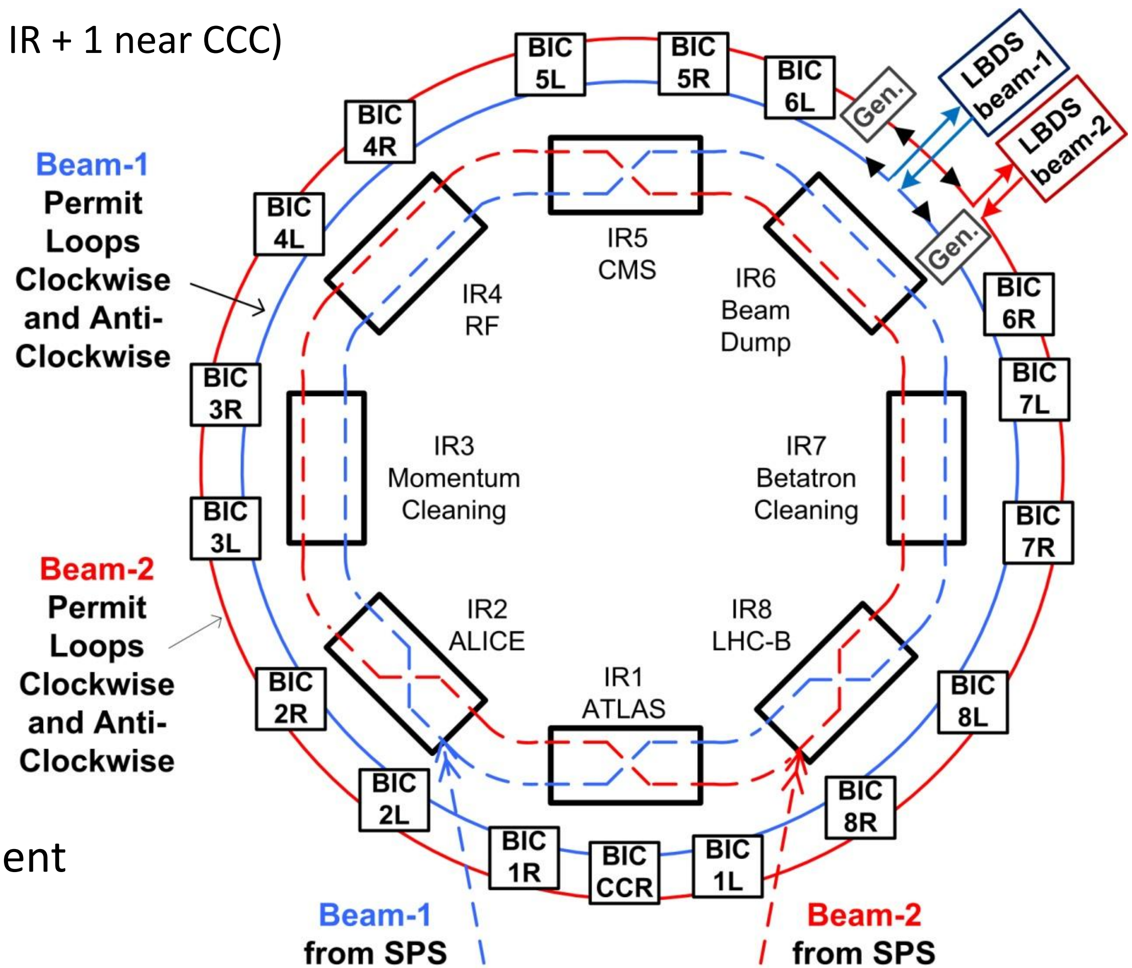
17 Beam Interlock Controllers (2 per IR + 1 near CCC)

4 fibre-optic channels from Point 6
- 1 clockwise &
- 1 anticlockwise for **each** Beam

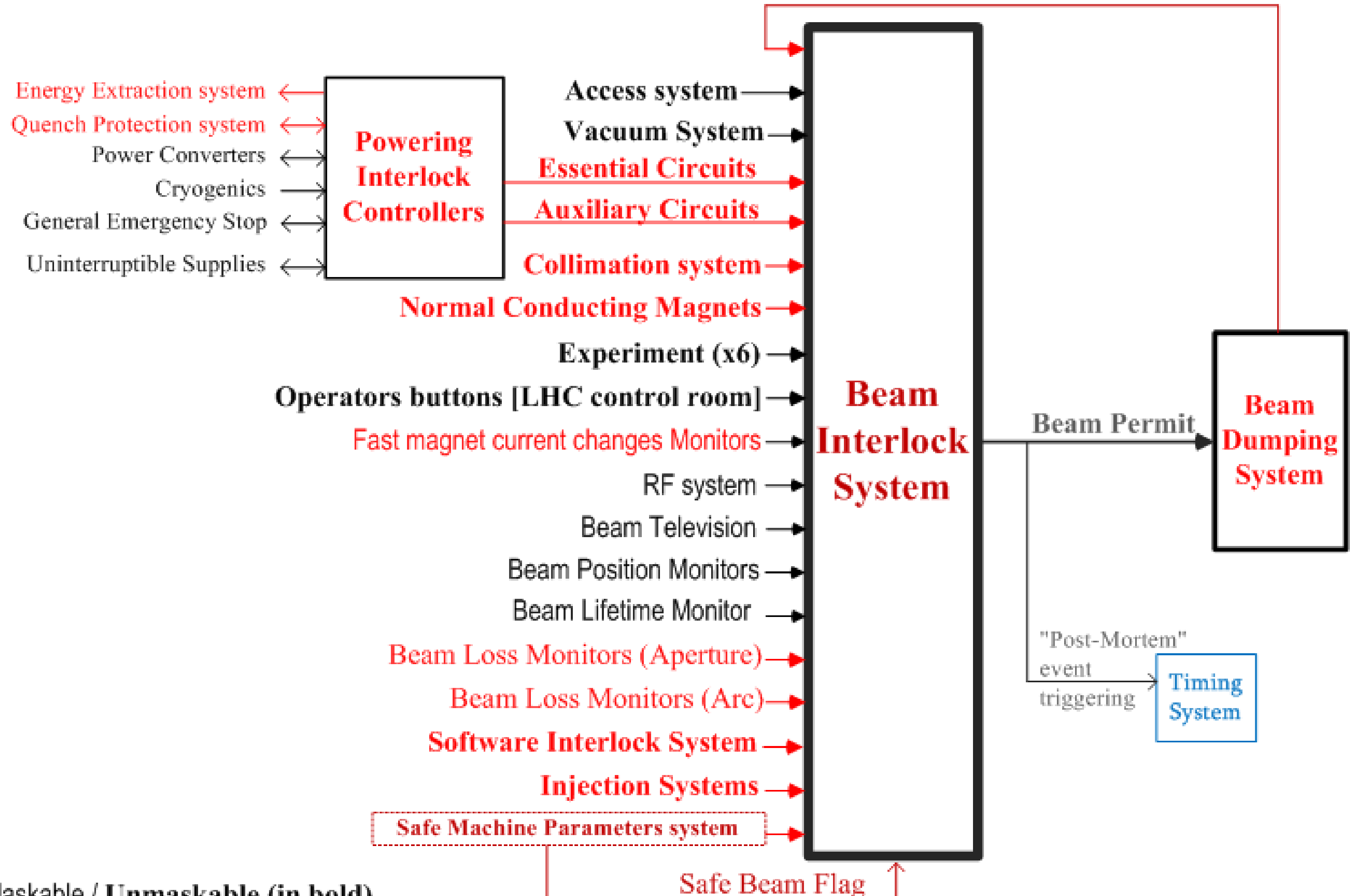
Square wave generated at IP6:
Signal can be **cut** and **monitored** by any Controller

When any of the four signals are absent at IP6, **BEAM DUMP!**

Beam-1 / Beam-2 loops are independent but they can be linked (or unlinked)



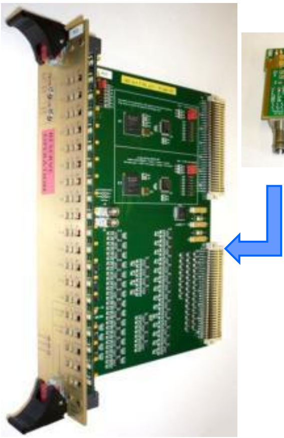
Connected systems



Maskable / **Unmaskable (in bold)**

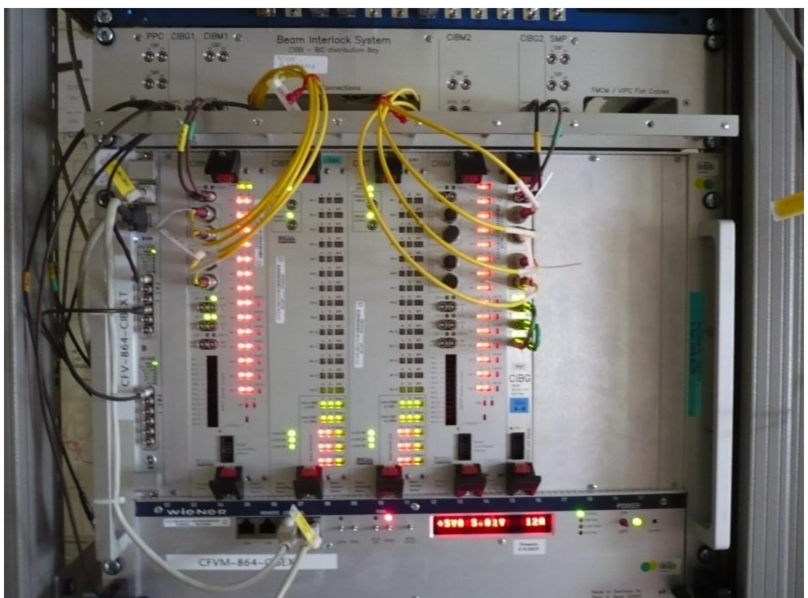
Machine Protection system

Typical Hardware



User Interface

Beam Interlock Controller (hosted in VME system)



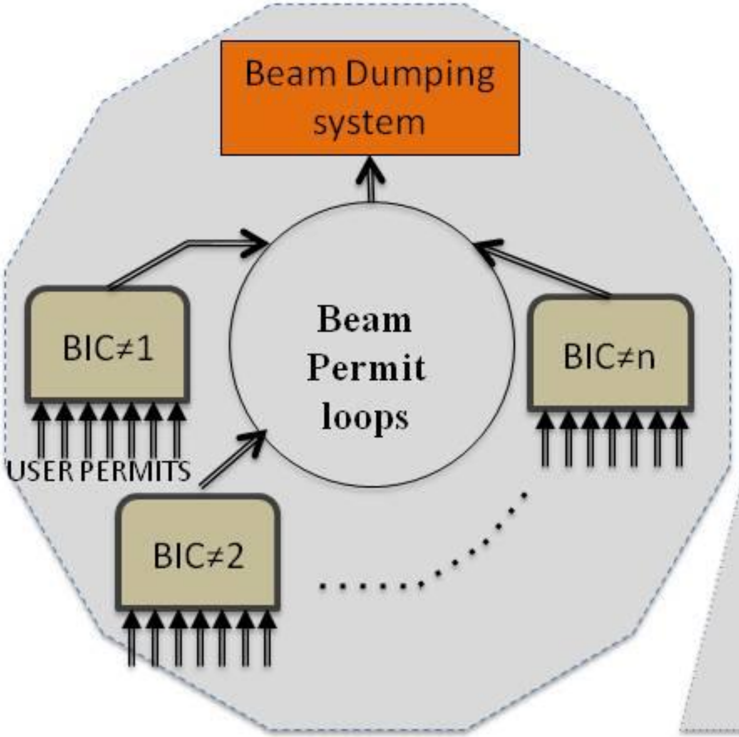
(Front view)

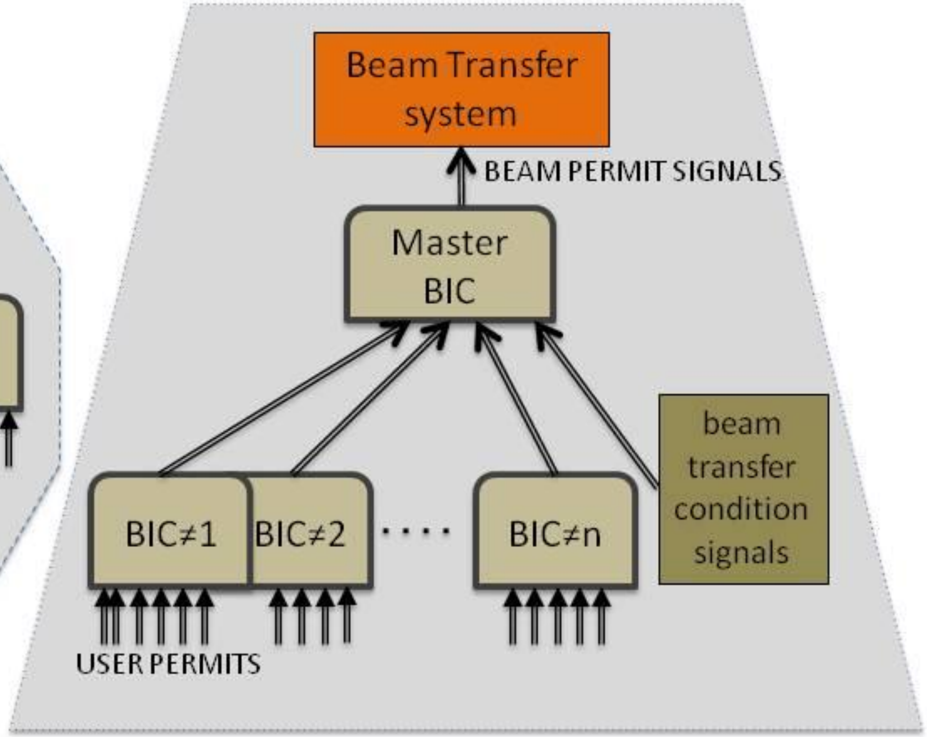
(Rear view)

Beam Interlock System types

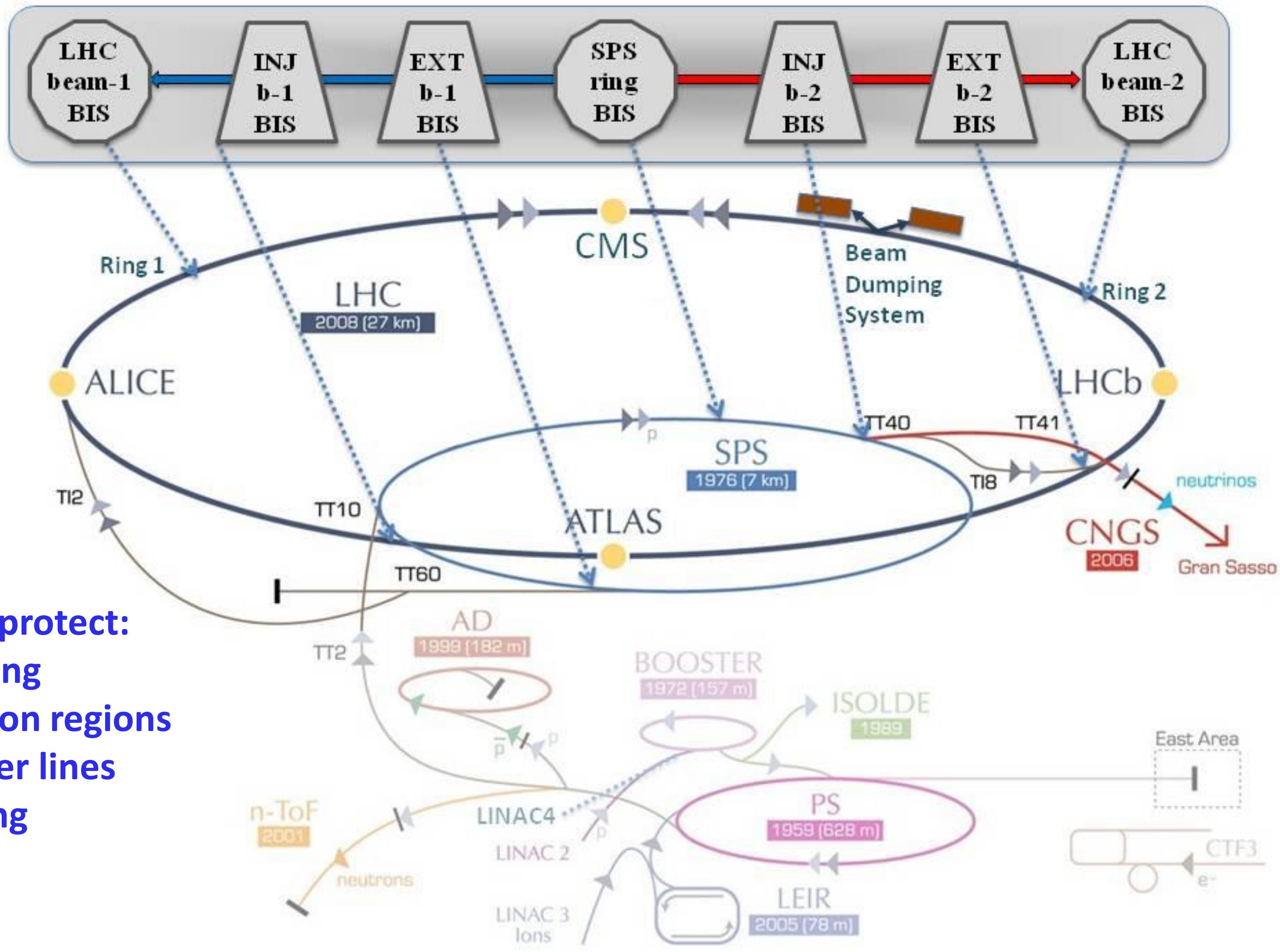
Two types of layout:

- **ring architecture**
- **tree architecture**





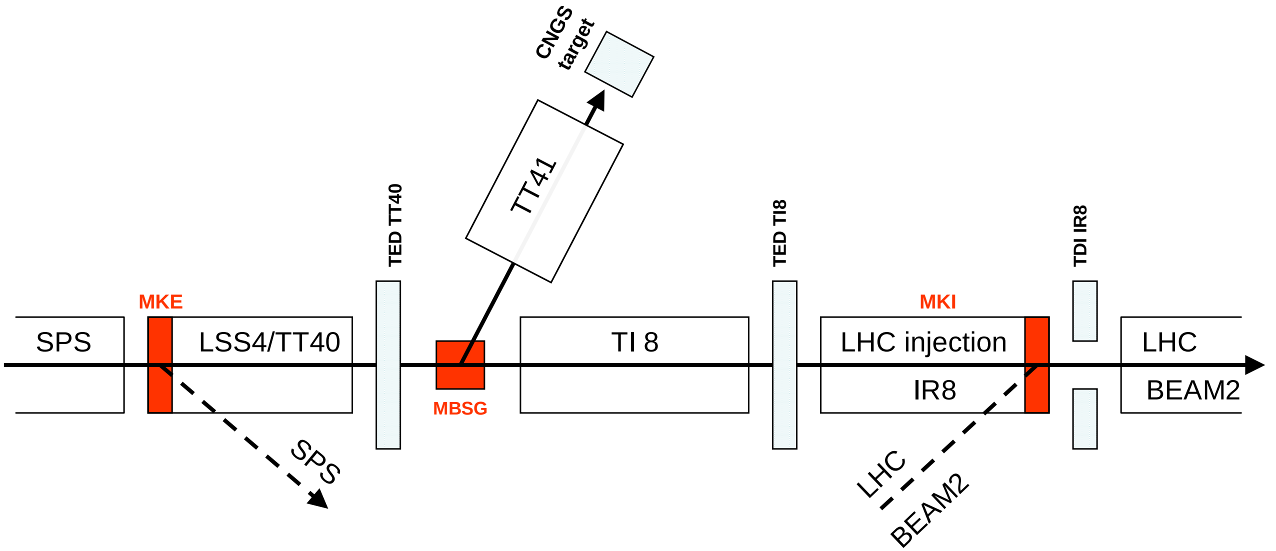
BIS Locations



Designed to protect:

- **LHC ring**
- **Injection regions**
- **Transfer lines**
- **SPS ring**

Operating modes for Transfer Line SPS-LHC-CNGS



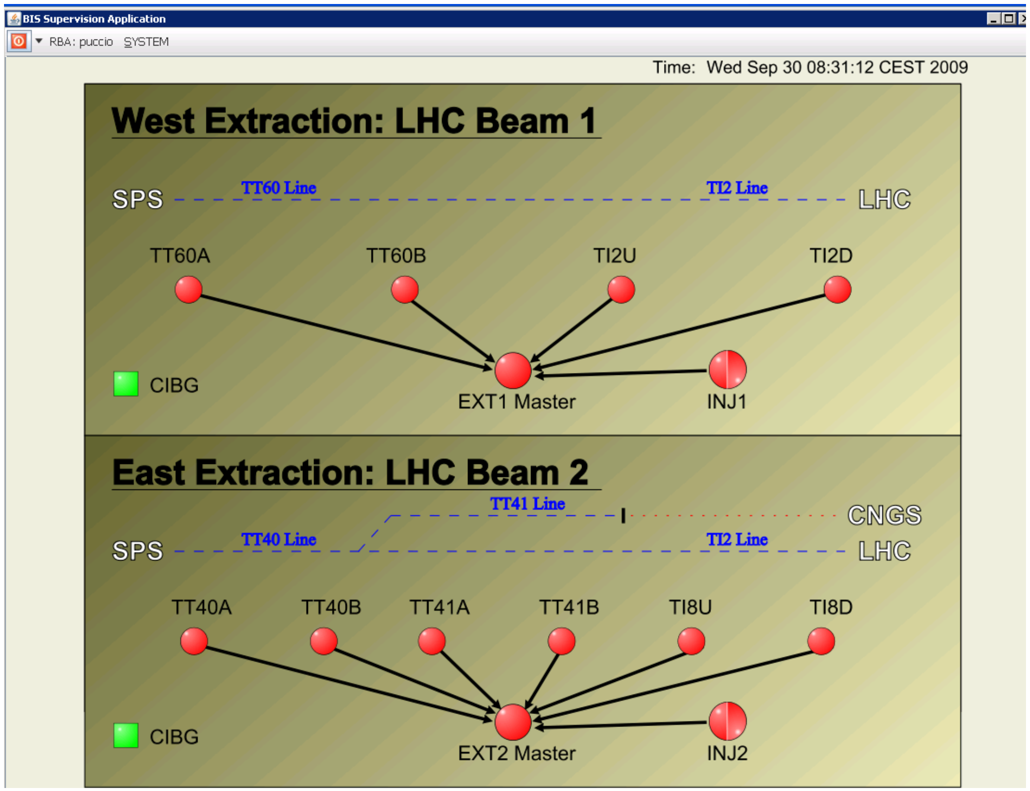
Various operating modes:

- Beam to TT40 TED
  (setting up of the SPS extractions),
- Beam onto downstream TED
  (setting up of the transfer line),
- Low intensity beam into the LHC
  (setting up of the LHC injections…),
- High intensity beam into the LHC
  (filling the LHC),
- Beam to CNGS target.
  (interleaved CNGS operation are required)

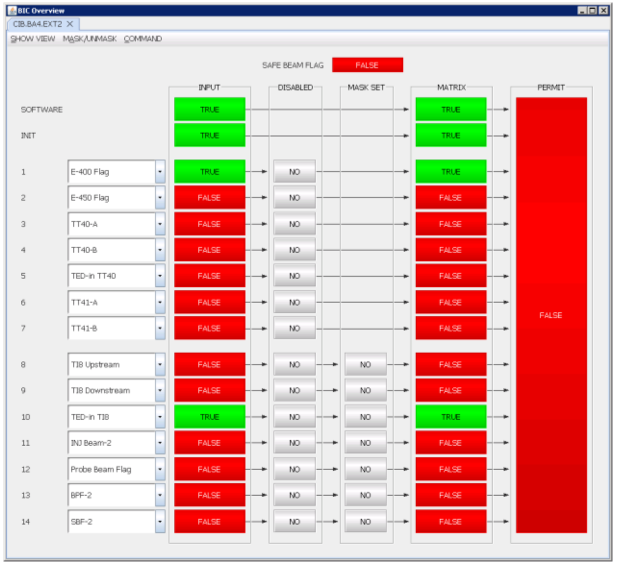
Corresponding **Truth Table** for Master BIC:

Inputs	User permits				Dumps					SPS/LHC							Output	
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15		1	2
Mode	LSS4 extraction/TT40 user permits	TT41/CNGS user permit	TI 8 upstream and downstream user permits	LHC IR8 injection user permits	TED upstream 'IN beam'	TED upstream 'OUT of beam'	TED downstream 'IN beam'	TED downstream 'OUT of beam'	TDI / TCLI in 'PROTECT' position	LHC beam permit	LHC beam presence flag	LHC safe beam flag	SPS safe beam flag	LHC beam type (timing signal)	CNGS beam type (timing signal)		SPS LSS4 extraction permit	LHC IR8 injection permit
1. Beam to LSS4/TT40 TED	1	x	x	x	1	0	x	x	x	x	x	x	x	x	x		1	0
2. Beam to TI 8 TED	1	0	1	x	0	1	1	0	x	x	x	x	x	1	0		1	0
3. Low intensity beam to LHC	1	0	1	1	0	1	0	1	x	1	x	x	1	1	0		1	1
4. High intensity beam to LHC	1	0	1	1	0	1	0	1	1	1	1	0	x	1	0		1	1
5. Beam to CNGS	1	1	0	x	0	1	x	x	x	x	x	x	x	0	1		1	0

BIS for Transfer Lines



Layout of Transfer Lines BIS



Master BIC (AND + OR function)

System Performance

Safe: (Safety Integrity Level 3 was used as a guideline).

Must react with a probability of unsafe failure of less than 10^{-7} per hour and,
Beam abort less than 1% of missions due to internal failure
(2 to 4 failures per year).

Reliable: (whole design studied using Military and Failure Modes Handbooks)

Results from the LHC analysis are:

P (false beam dump) per hour = 9.1×10^{-4}

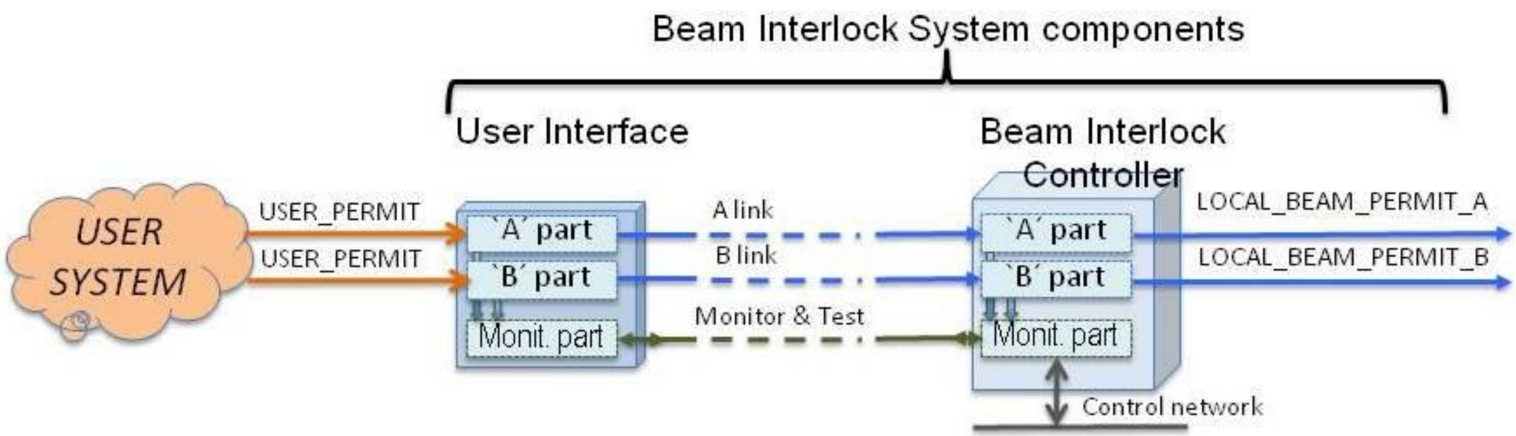
P (missed beam dump) per hour = 3.3×10^{-9}

Critical process in Hardware:

- ♦ functionality into 2 redundant matrices
- ♦ VHDL code written by different engineers following same specification.

Critical versus Non-Critical:

- ♦ Critical functionality always separated from non-critical.
- ♦ Monitoring elements fully independent of the two redundant safety channels.



100% Online Test Coverage:

Can be easily tested from end-to end in a safe manner
=> recovered "good as new"

System Performance (3 of 3)

"Flexible":

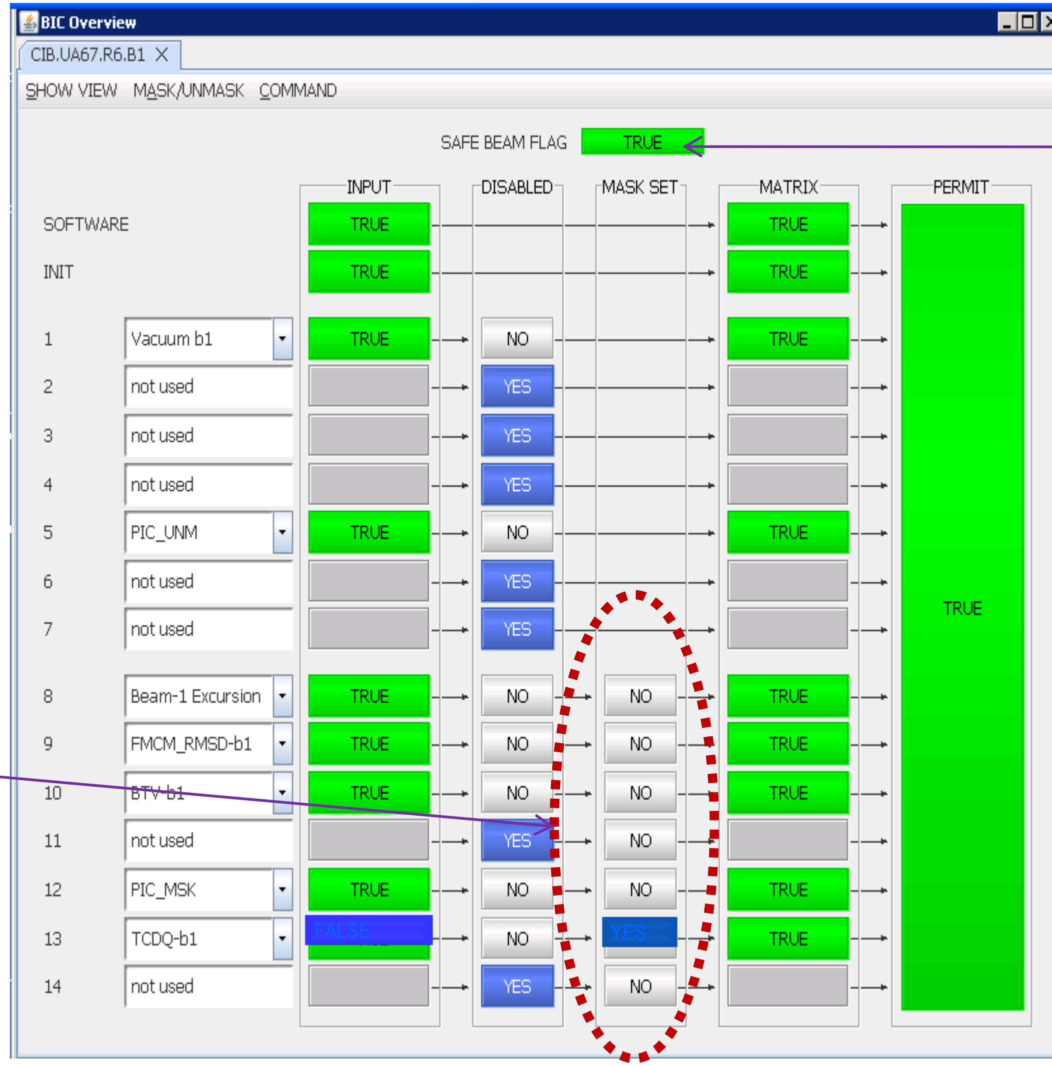
thanks to Input Masking

Masking depends on an external condition:

the **Setup Beam Flag**

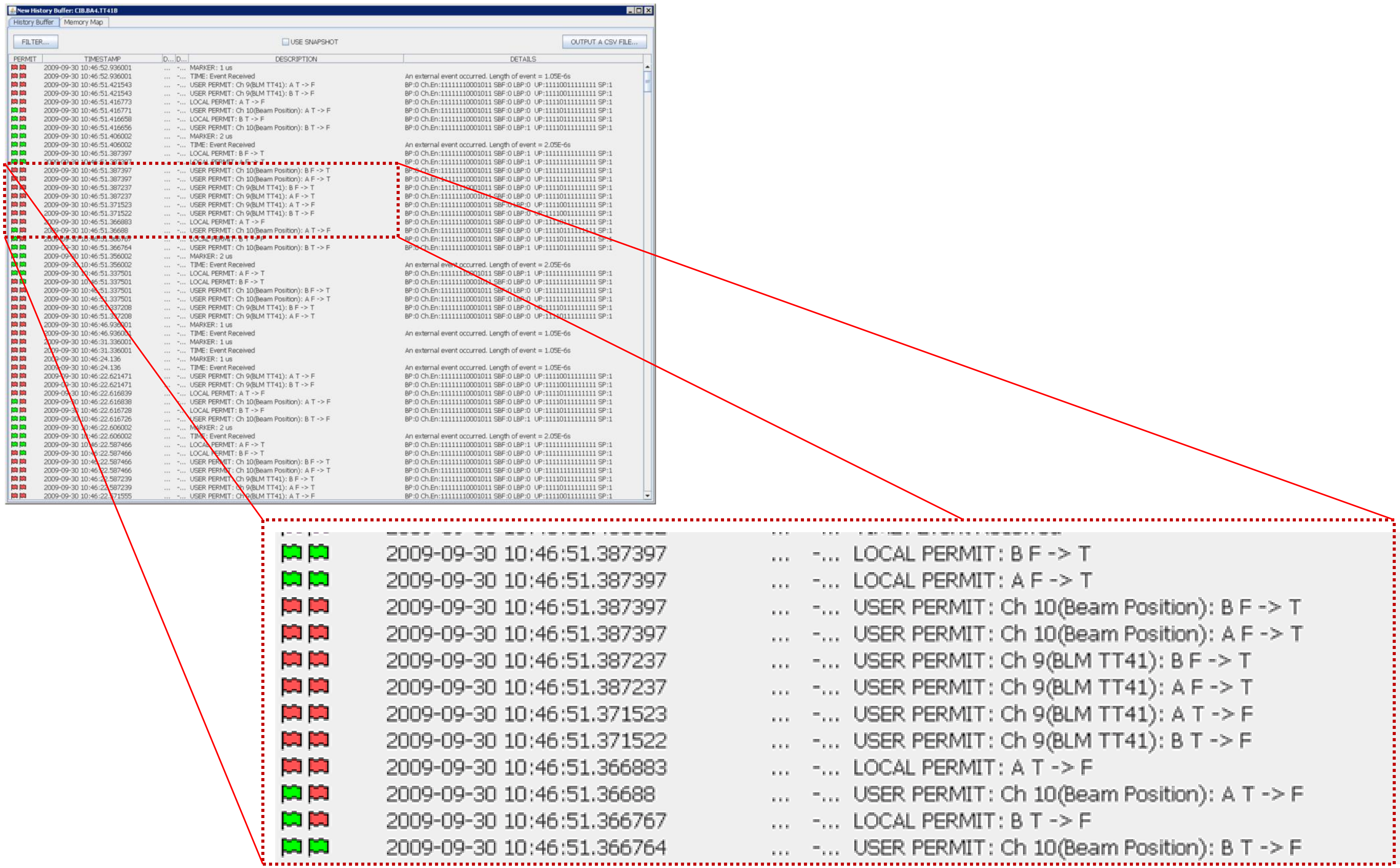
the SBF is generated by the SMP system (*see 2nd part of the presentation*) and is distributed by Timing

Within a fixed partition, half of *User Permit* signals could be remotely masked



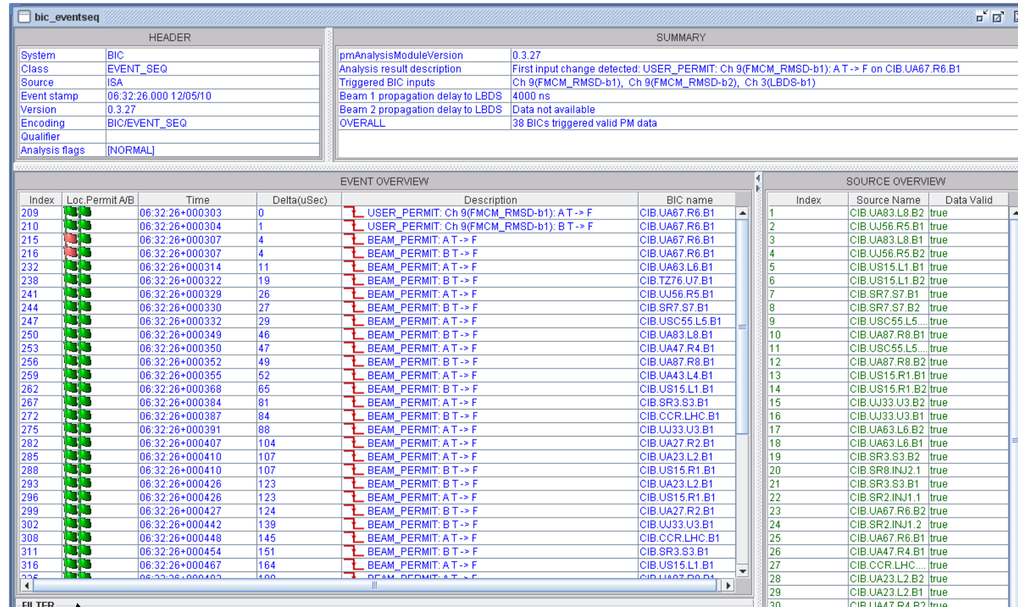
Masking automatically removed when "Setup Beam Flag" is FALSE

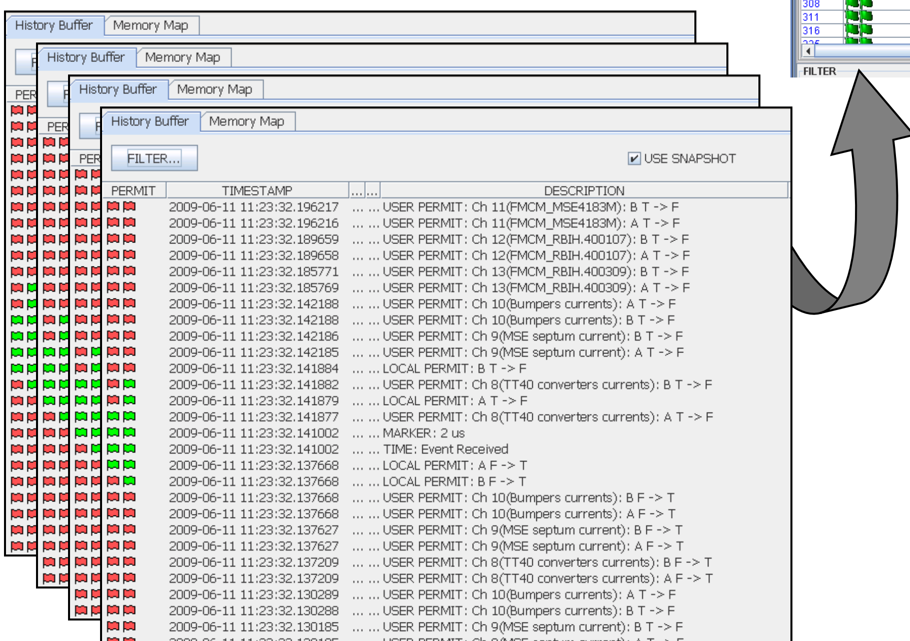
BIS monitoring: History Buffer



Key element of Post Mortem analysis

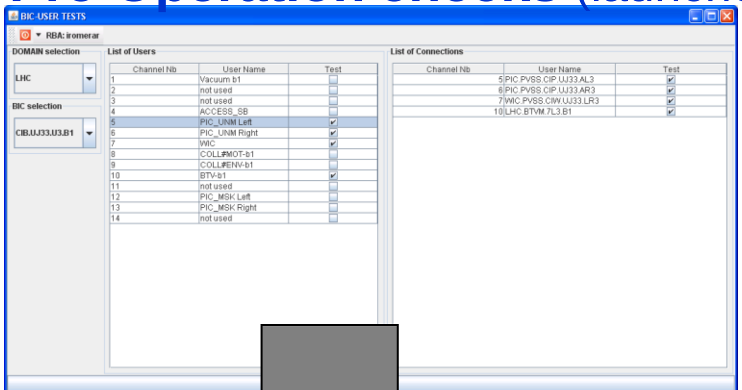
Thanks to the different gathered History Buffers:
- Identification of the beam dump source
- Reconstruction to the sequence of events that has led to the beam dump





Operational Tests

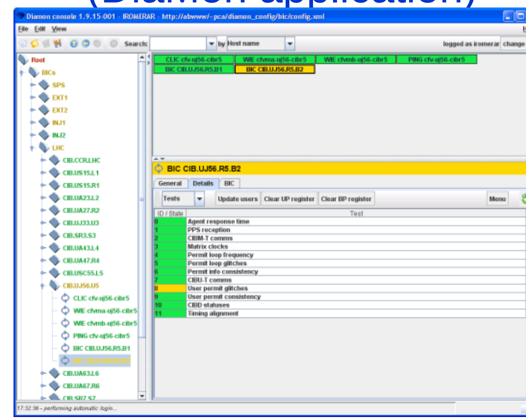
Pre-Operation checks (launched by Beam Sequencer)



configuration verification and integrity check

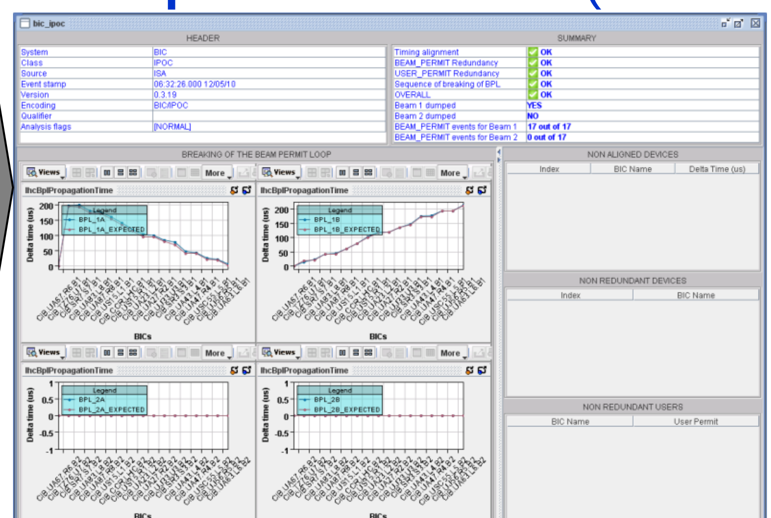
During Operation (DiaMon application)

fault diagnosis and monitoring



Post-Operation checks (included in PM)

response analysis



In order to ensure that its safety is not compromised, the verification of the BIS is carried out in three stages

Operational Experience

- Originally designed for LHC and firstly installed in its pre-injector for validation.
- **Since 2006**, fully operational for the SPS ring and its transfer lines.
- Very high availability (99.996%) with only one stop due to a failure from one of the BIC modules.
- No **false dump has been noticed**.
- For the Transfer lines: “millions” of extractions to CNGS target have been safely managed.
- As foreseen, some PSU failed; thanks to redundancy, it has never lead to a beam operation disruption.
- Since restart in Nov.09, LHC-ring BIS extensively exercised with ~1000 emergency dumps; Promising availability (only few failures with redundant VME Power Supplies and with VME Processor boards)

Summary

- Core of the LHC machine protection
- more than 20 connected systems
- Protects also the Transfer lines and both LHC Injection regions
- Fully redundant and Critical process separated from Monitoring
- 100% test coverage => recovered “good as new”
- 3-stage verification:
  - Validation prior to beam operation
  - On-line diagnostics during beam operation
  - Post operation checks
- In operation since 2006: any malfunction has been reported.
- Reviewed in 2006 and in 2009

Safe Machine Parameter System

Benjamin TODD

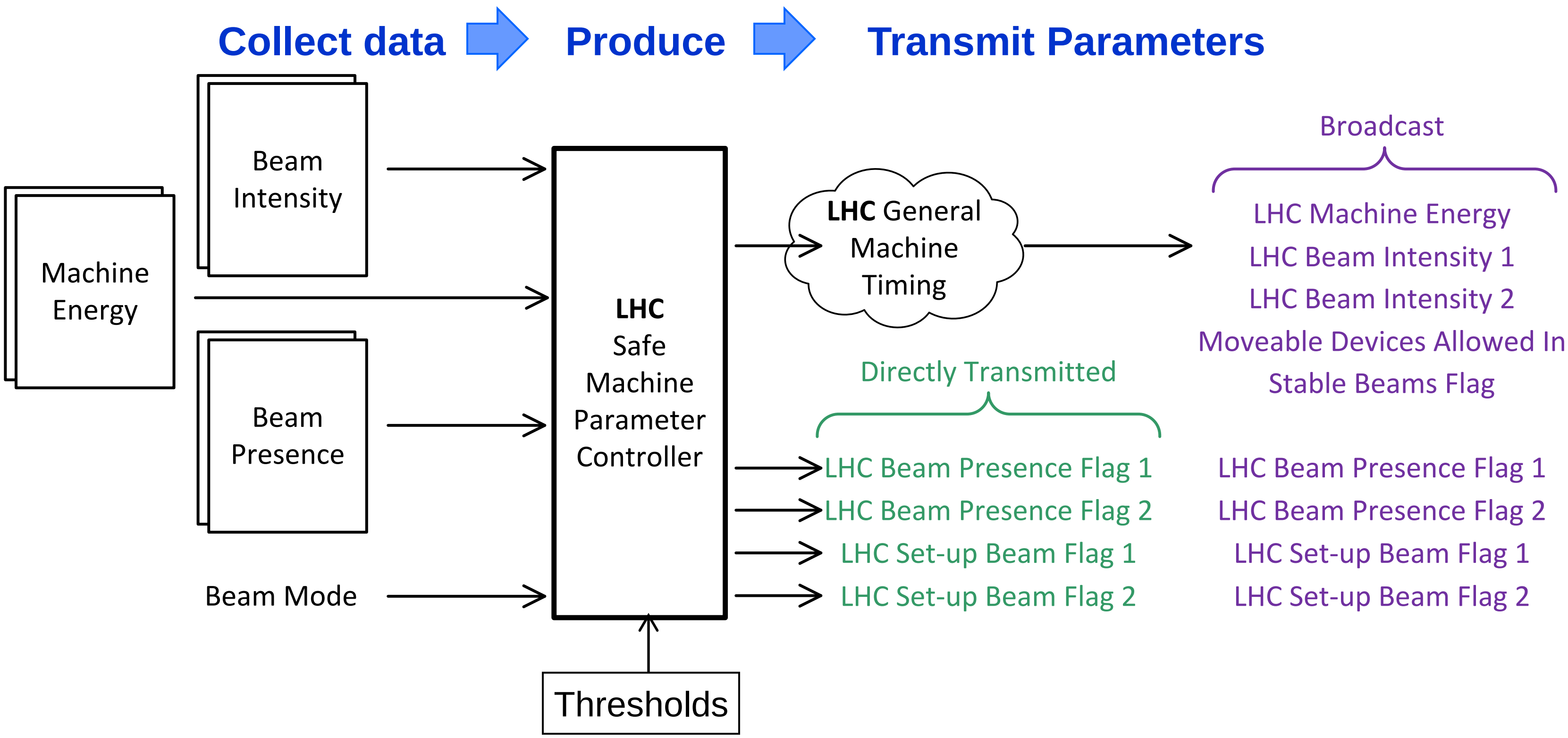
MP Review

6-8th Sept. 2010

Safe Machine Parameters in LHC

Function: for safe operation, **generate** several mission **critical parameters** and **distribute** them around the LHC and the SPS extraction regions.

Safe Machine Parameters (SMP) derived from operational conditions of SPS and LHC accelerators, by two Safe Machine Parameter Controllers: one for LHC + one for SPS.



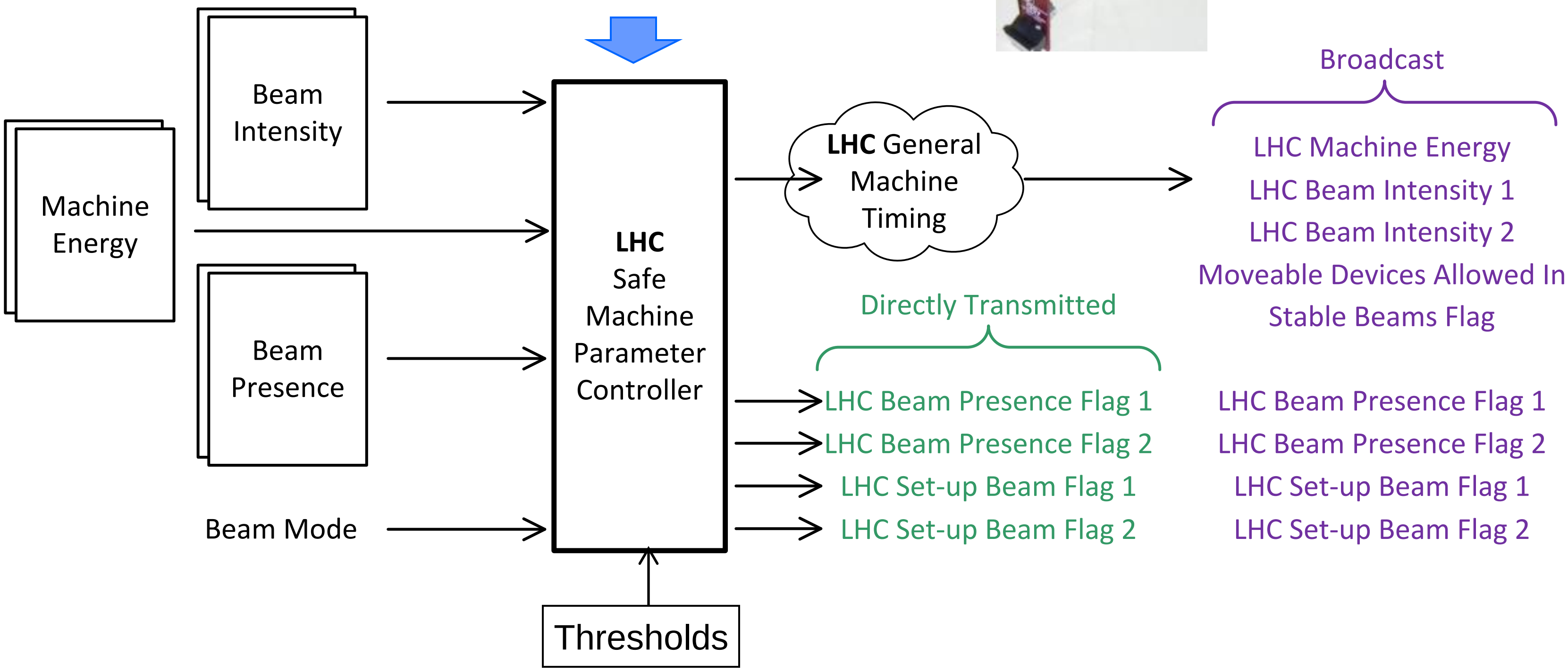
LHC SMP controller inputs & outputs

(similar layout for the SPS)

Hardware in VME format

Set of boards installed in a VME-bus system: the SMP Controller

dedicated VME-bus SMP receiver board (CISV) installed in each SMP User's crate



LHC Parameters currently processed

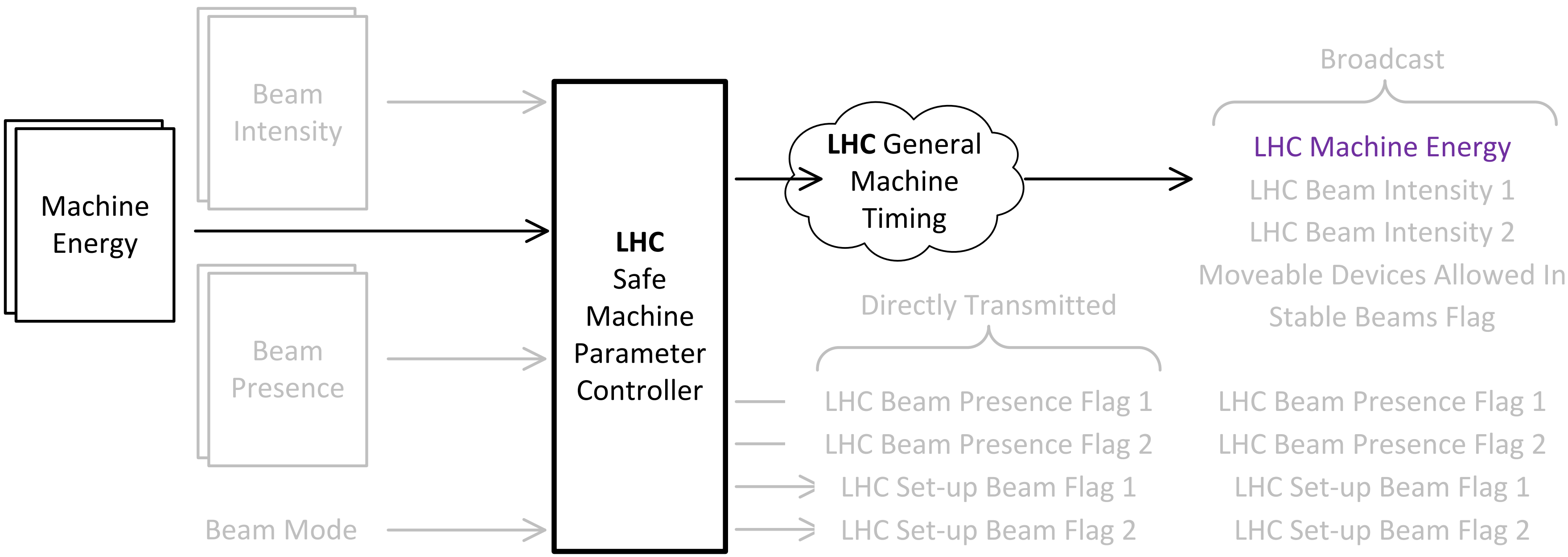
Name	Source(s)	Machine Prot. User(s)	Transmitted via
Machine Energy	LHC BETS	Beam Dumping System Collimation Injection Kickers Beam Loss Monitors Radio Frequency	Timing
Beam Intensity 1 & 2	LHC SLOW BCT	none	Timing
Beam Presence Flags (1 & 2)	LHC FAST BCT LHC BPM	Extraction BIS	direct link
Set-up Beam Flags (1 & 2)	LHC SLOW BCT LHC BETS	Extraction BIS	direct link
		LHC BIS	Timing
"Moveable Devices allowed in" Flag	LHC BETS Sequencer	Experiments	Timing
Stable Beam Flag	LHC BETS Sequencer	Experiments	Timing

SPS Parameters currently processed

Name	Source(s)	Machine Prot. User(s)	Transmitted via
SPS Probe Beam Flag	SPS BCT-4 INTENSITY	Extraction BIS	direct link
SPS Set-up Beam Flag	SPS BCT-3 INTENSITY	Extraction BIS	direct link
CNGS Cycle Flag	Beam Energy Meter (BEM)	Extraction BIS	direct link
LHC Cycle Flag			
HiRadMat Cycle Flag			

Safe Machine Parameters in LHC

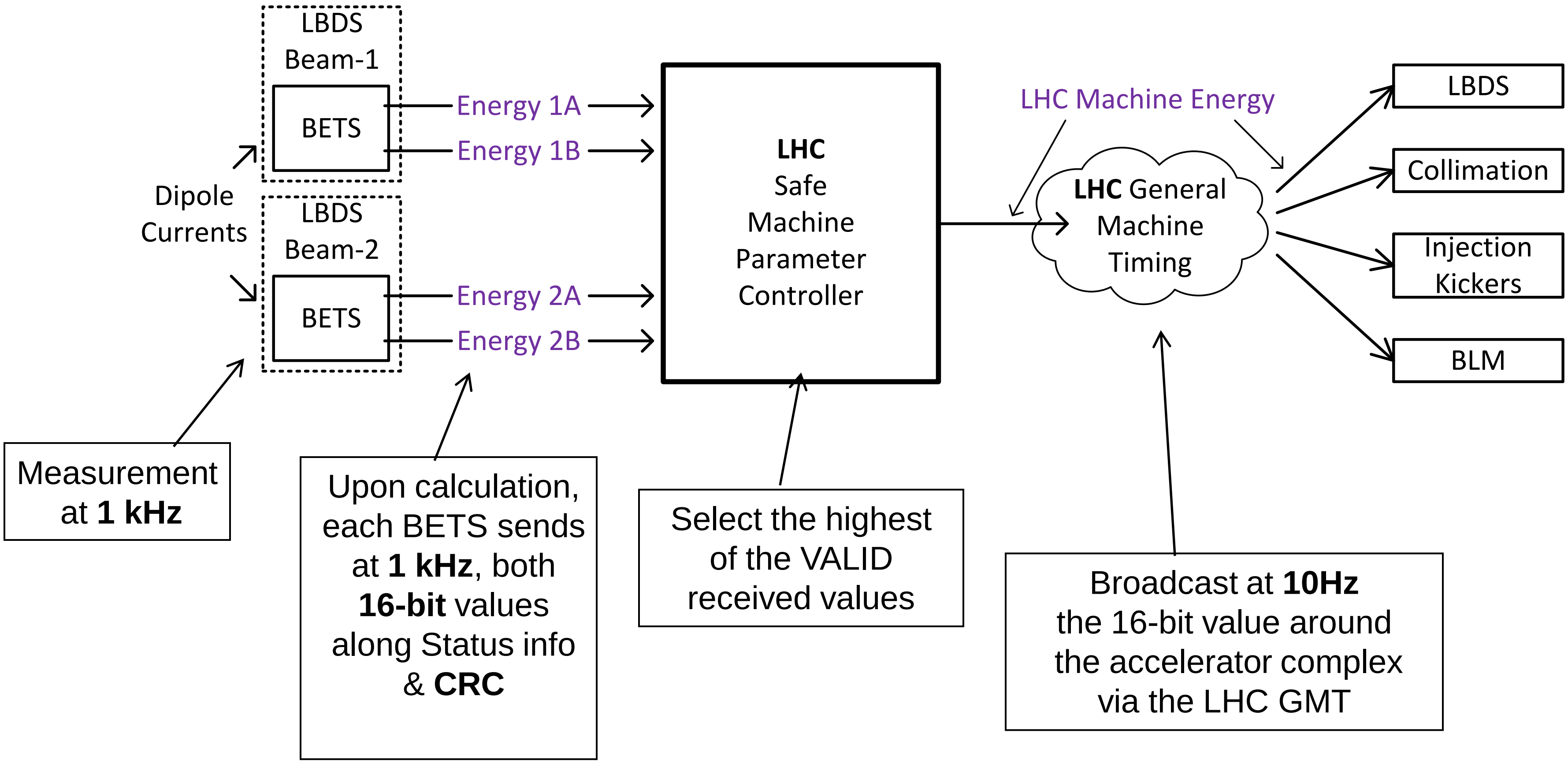
...LHC Machine ENERGY...



Machine Energy Layout

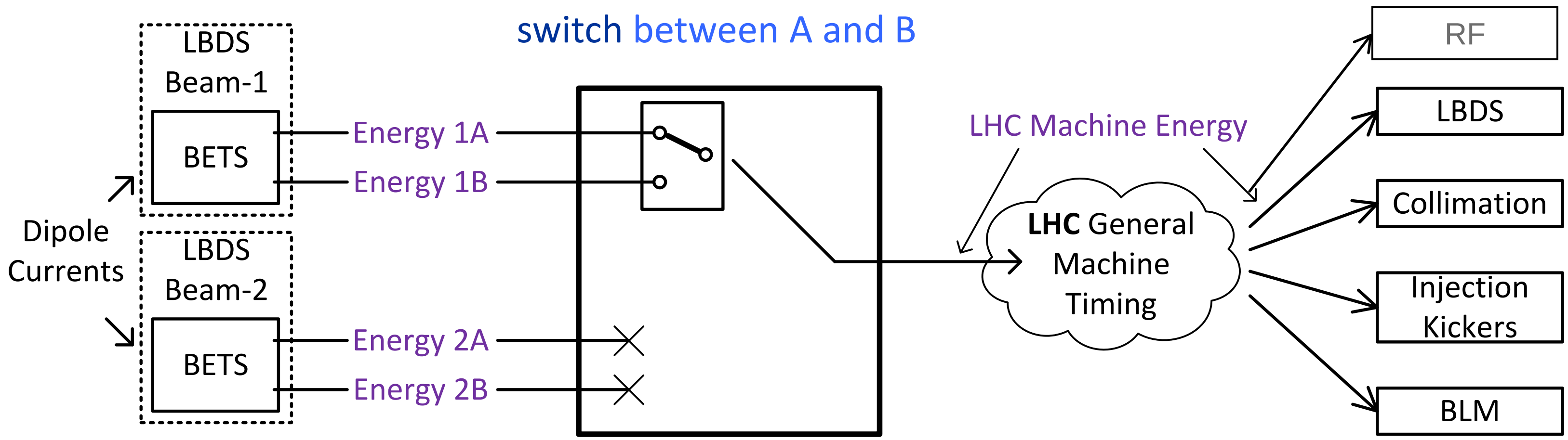
Energy values represented in **16-bit** format (**120 MeV** granularity)

Fail-safe value => maximum value 0xFFFF: $(2^{16} - 1) \times 120$ [MeV] = 7864.200 GeV
Value for nominal physics energy (7TeV) => 0xE3DE: (5834x 120 [MeV] = 7000.80 GeV

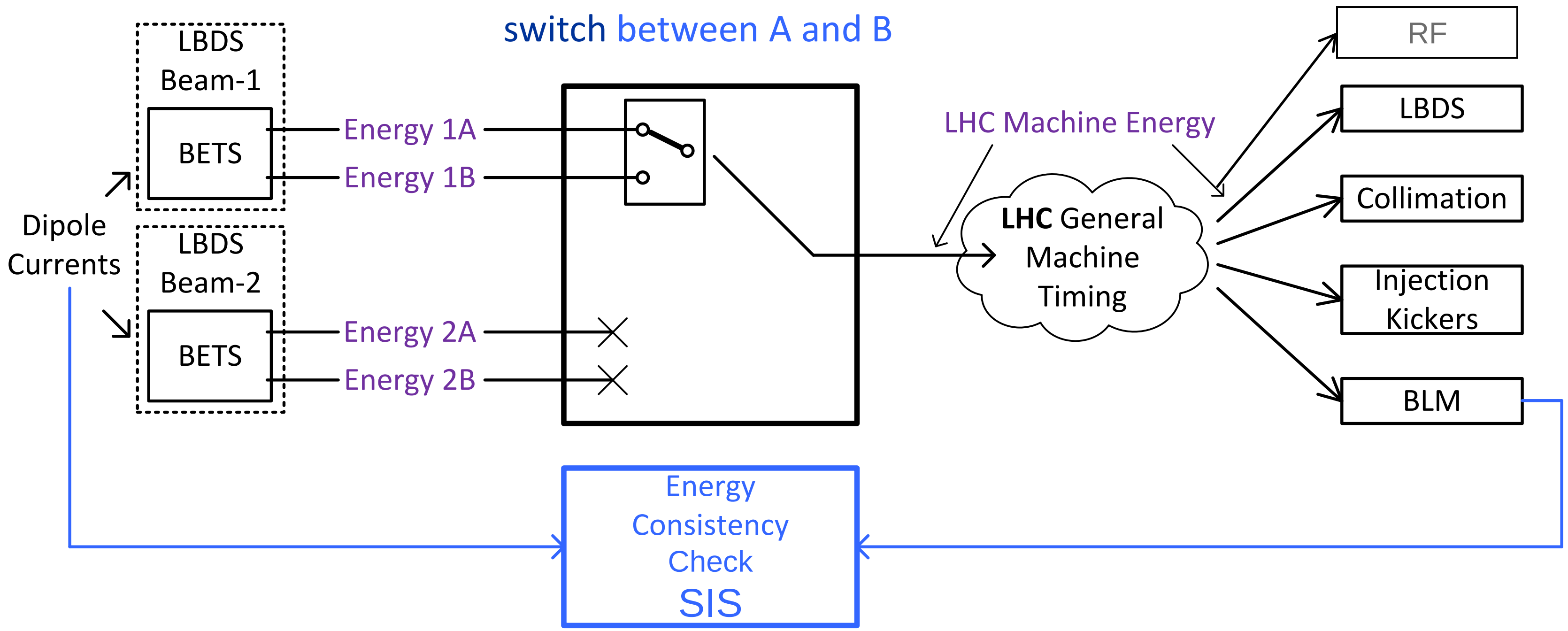


BETS : Beam Energy Tracker System

Implementation in 2010



Implementation in 2010



≈ 0.5 Hz cross-check

dipole currents must be equivalent to BLM energy reading (1%)

In 2011, the upgraded version (SMP 3v0) will implement complete redundancy.

SMP for LHC: Set up Beam Flags

Name	Source(s)	Machine Prot. User(s)	Transmitted via
Machine Energy	LHC BETS	Beam Dumping System Collimation Injection Kickers Beam Loss Monitors Radio Frequency	Timing
Beam Intensity 1 & 2	LHC SLOW BCT	none	Timing
Beam Presence Flags (1 & 2)	LHC FAST BCT LHC BPM	Extraction BIS	direct link
Set-up Beam Flags (1 & 2)	LHC SLOW BCT LHC BETS	Extraction BIS	direct link
		LHC BIS	Timing
"Moveable Devices allowed in" Flag	LHC BETS Sequencer	Experiments	Timing
Stable Beam Flag	LHC BETS Sequencer	Experiments	Timing

LHC Setup Beam Flag: definition

- Used by LHC BIS where maskable inputs can be masked when this flag is TRUE.

- Additionally used by the SPS Extraction BIS, as one of the pre-defined conditions for extracting beam above defined limits.

- Derived from LHC_INTENSITY (beam-1 & beam-2) and LHC_MACHINE_ENERGY:

NORMAL equation

$$\left(\frac{\text{ENERGY[GeV]}}{450\text{[GeV]}}\right)^{1.7} \times \text{INTENSITY[p]} < 1 \times 10^{11}$$

RELAXED equation

$$\left(\frac{\text{ENERGY[GeV]}}{450\text{[GeV]}}\right)^{1.7} \times \text{INTENSITY[p]} < 4 \times 10^{11}$$

SMP controller able to manage 2 more equations like **Very relaxed** and **ION** : TBD

- Implemented in the Safe Machine Parameters Controller in using the following function:

$$\text{INTENSITY[p]} < \text{f(ENERGY[GeV])}$$

$$\text{f(ENERGY[GeV])} = \text{THRESHOLD}$$

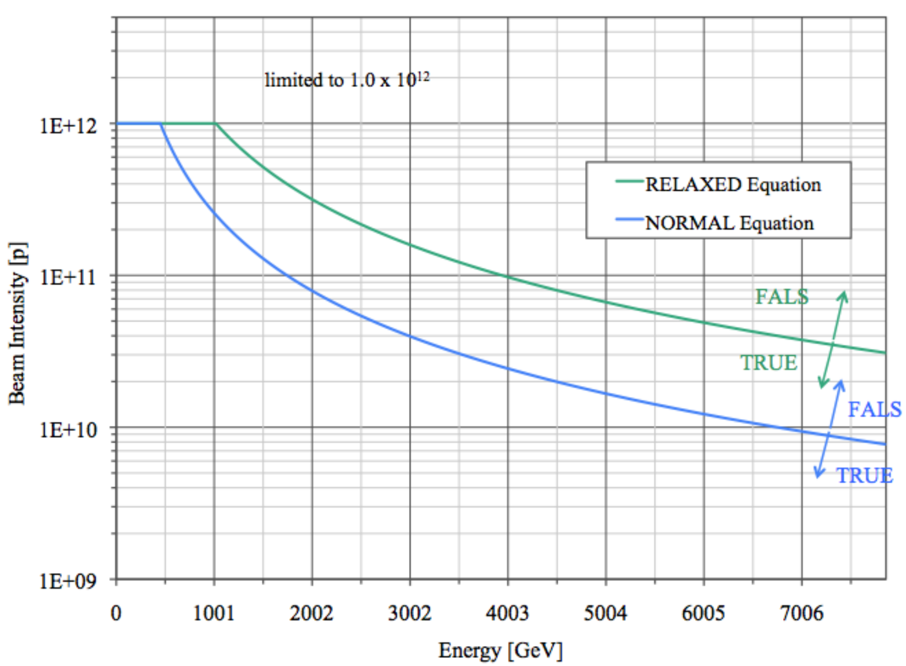
LHC Setup Beam Flag: implementation

In all cases, **I[p] restricted to** absolute maximum of **$1x10^{12}$ protons**
$\Rightarrow$ corresponding Set-up Beam Flag = **FALSE if** beam intensity **above** this limit.

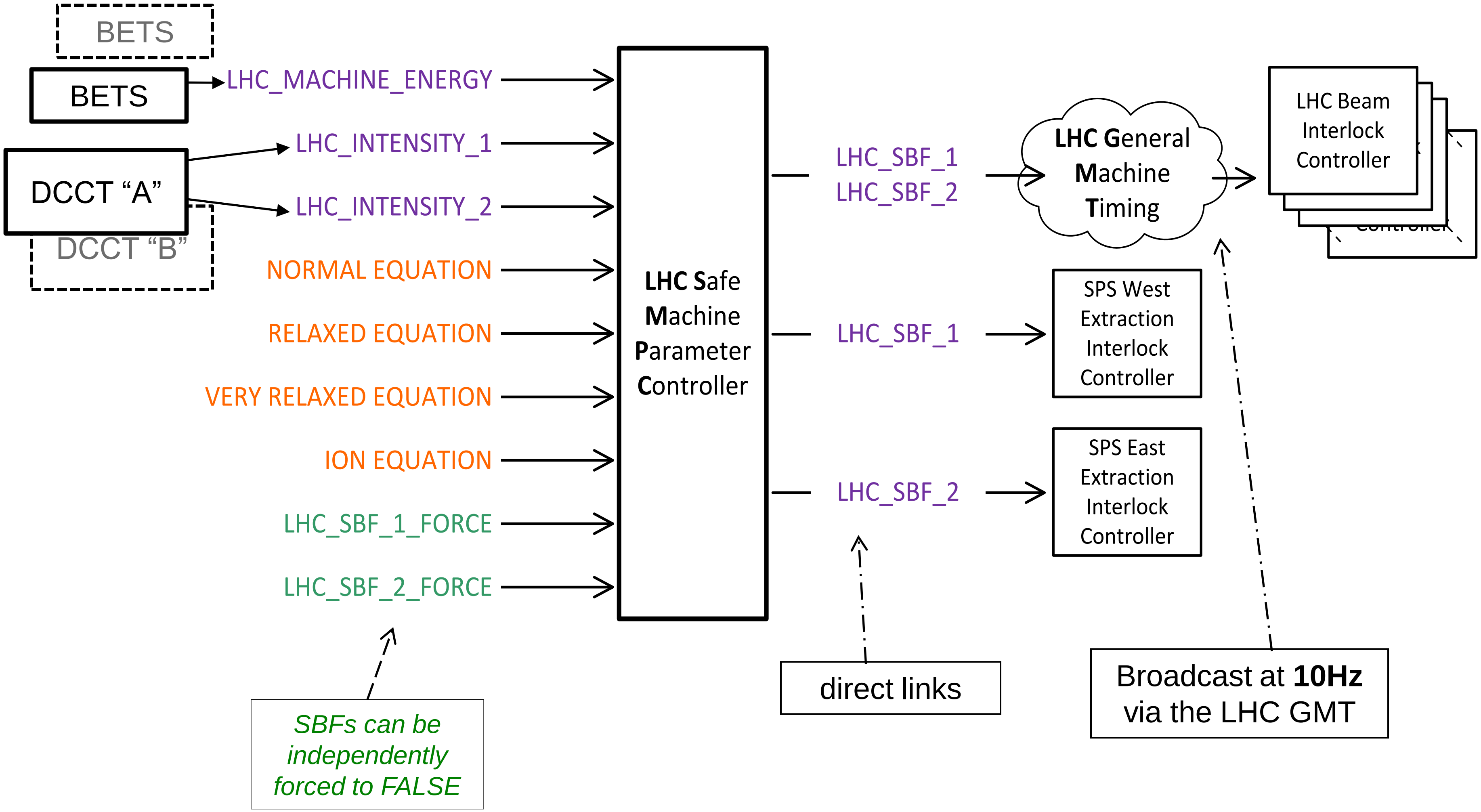
Examples of the corresponding beam intensity limits at various energies are:

Energy [GeV]	NORMAL Equation [p]	RELAXED Equation [p]
450	1.00×10^{12}	1.00×10^{12}
1000	2.65×10^{11}	1.00×10^{12}
2000	8.15×10^{10}	3.26×10^{11}
3500	3.14×10^{10}	1.26×10^{11}
5000	1.71×10^{10}	6.86×10^{10}
7000	9.60×10^{9}	3.87×10^{10}

Normal Vs Relaxed chart



LHC Setup Beam Flag: generation



SMP for LHC: Beam Presence Flags

Name	Source(s)	Machine Prot. User(s)	Transmitted via
Machine Energy	LHC BETS	Beam Dumping System Collimation Injection Kickers Beam Loss Monitors Radio Frequency	Timing
Beam Intensity 1 & 2	LHC SLOW BCT	none	Timing
Beam Presence Flags (1 & 2)	LHC FAST BCT LHC BPM	Extraction BIS	direct link
Set-up Beam Flags (1 & 2)	LHC SLOW BCT LHC BETS	Extraction BIS LHC BIS	direct link Timing
"Moveable Devices allowed in" Flag	LHC BETS Sequencer	Experiments	Timing
Stable Beam Flag	LHC BETS Sequencer	Experiments	Timing

LHC Beam Presence Flag: definition

- Extraction of high intensity beam from SPS towards LHC is allowed when a circulating beam is **already present** in the LHC.

- To ensure this, **two** Beam_Presence Flags are produced and transmitted to both beam Extraction interlock systems of the SPS.

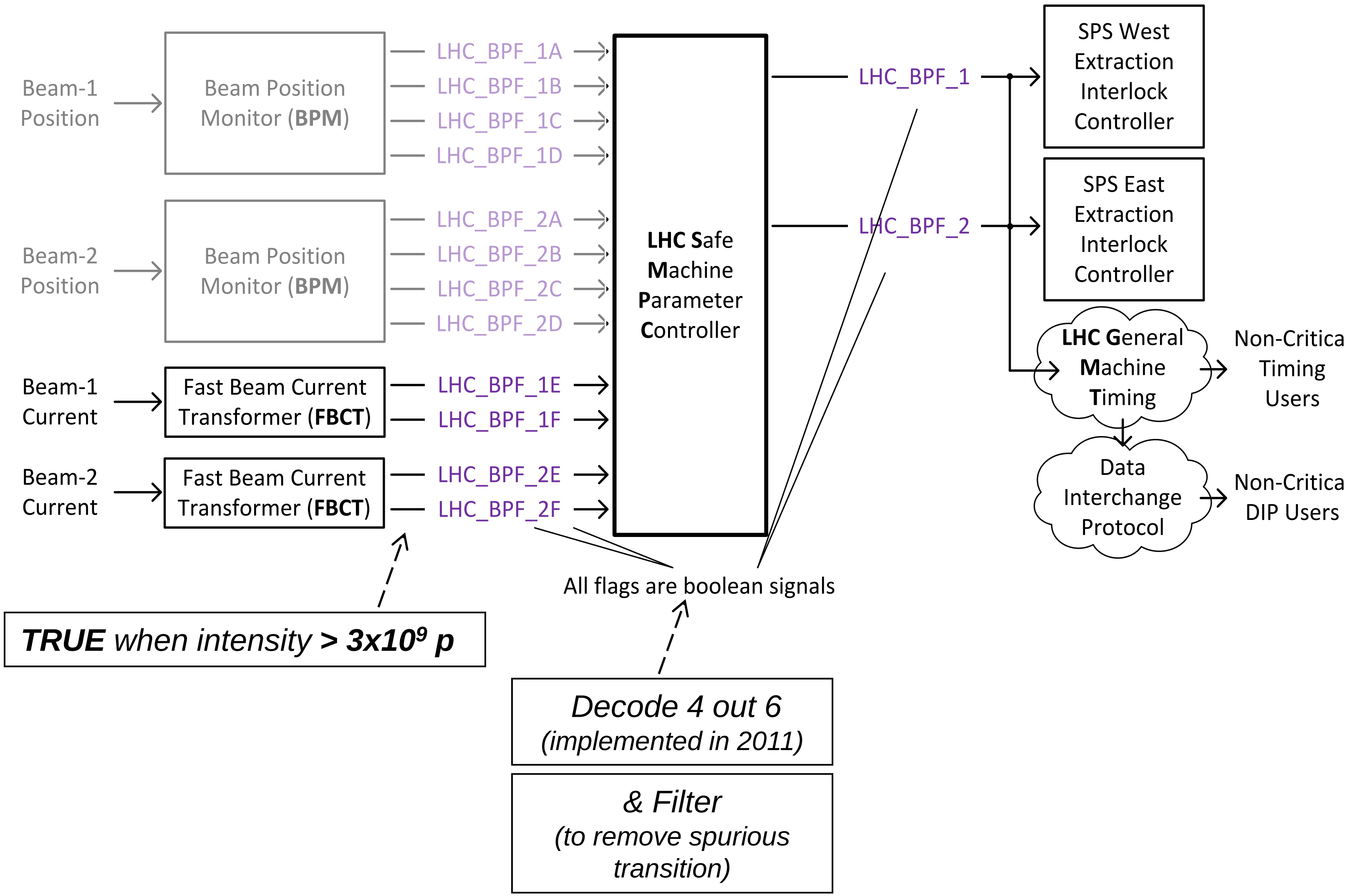
- Two sources of beam presence are (going to be) used:

  - Fast Beam Current Transformers (**FBCTs**):
    => 2 Beam_Presence Flags derived per beam

  - [from 2011] a hardware chain linked to Beam Position Monitor (**BPM**) electronics:
    => 4 Beam_Presence Flags derived per beam

- The SMP Controller uses the Flags given by these systems, filter them and derive a single Beam_Presence Flag per beam:
  - Directly transmitted to the Extraction BIS
  - also broadcast over the GMT (for general use only)

LHC Beam Presence Flag: layout

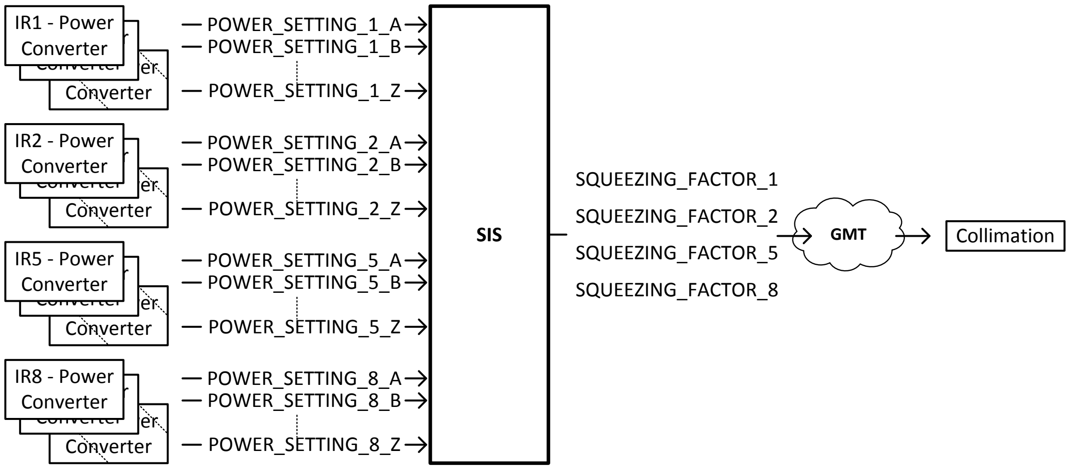


Future development: Squeeze Factors

- Used by Collimation system to ensure that placement of collimator jaws tracks the changes in beam orbit during the beam squeezing phase.

- four factors: one per Experiment (ATLAS, ALICE, CMS and LHCb)
  each is determined by power converter settings around the experimental area

- Current solution is using the **S**oftware **I**nterlock **S**ystem:



- Could be replaced by an Hw solution:
  the upgraded 2011 version will be designed with sufficient resources to be able implement squeezing factor reception, generation and transmission.
  Meanwhile, the Collimation system is possibly not to consider Squeeze Factors as dependable value at this time. TBC.

Cross-checking of the SMP Distribution

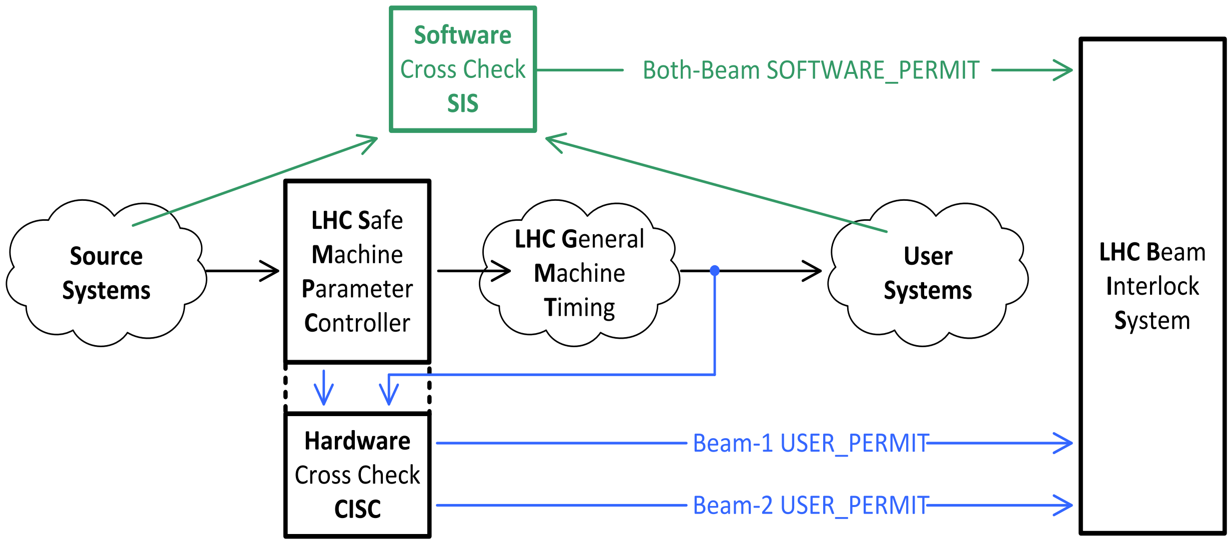
The GMT system has not been designed to transmit safe parameters…

=> Additional features have been implemented in the Timing Receiver board

- Time-out and fail-safe state
- History buffer

=> Cross-checking is performed

- by the Software Interlock System (current solution)
- by an additional Hw solution (in 2011)



Cross-checking by Sw Interlock System

- Compare **Source System** information with **User System** status
  - like LHC Machine Energy:

    with a cross-check between LHC dipole currents, and energy received by BLM.

- Rate of **0.1 to 1 Hz**, making complex checks involving multiple variables from around the LHC machine.

- Result is used to derive a SOFTWARE_PERMIT connected to the LHC BIS. (if an inconsistency is detected, the LHC beam permit will be removed)

- Further cross-checks could be applied in the next future, like:
  - SPS Probe Beam Flag:

    cross-check that flag is not TRUE for longer than 3 seconds.
  - SPS Set-up Beam Flag:

    cross-check that flag is not TRUE for longer than 3 seconds.
  - SPS Probe vs Set-up Beam Flag:

    cross-check that the two flags are in agreement, i.e. PROBE should not be TRUE if SET-UP is FALSE.

SMP Summary

- Used to modify configuration of some LHC Machine Protection systems
- 2 systems (LHC + SPS), Various parameters, different sources & customers
- In operation for SPS Extractions since 2008
- Depends on data sources (accuracy and latency)
- Critical process separated from Monitoring
- Has to balance Safety Vs Availability
- SMP Distribution by the Timing System
- Cross-checking by Software System System
- Improvements foreseen in 2011:
  - Able to manage multiple sources
  - Fully redundant together with 100% test coverage
  - Hw Cross-checking by closing the loop SMP➡GMT➡SMP
  - 3-stage verification: prior/during/post beam operation

Fin

Thank you for your attention

Spare Slides

Number of BIS channels

COLLIM. (Environm.)	20	(0/20)
COLLIM. (Motors)	22	(0/22)
PIC	32	(16/16)
VACUUM	30	(30/0)
BLM	16	(8/8)
FMCM	12	(0/12)
BTV	9	(0/9)
WIC	8	(8/0)
ATLAS	4	(3/1)
CMS	3	(2/1)
LHCb	3	(2/1)
TOTEM	3	(3/0)
ALICE	2	(1/1)
ACCESS	4	(4/0)
RF	4	(4/0)
BPM	4	(0/4)
LBDS	3	(2/1)
MKI	2	(2/0)
BCT	2	(0/2)
MKQA	2	(2/0)
Operator Switch	2	(2/0)
Program. B.D.	2	(2/0)
SMP	2	(2/0)
TCDQ	2	(0/2)
MKI test mode key	1	(0/1)
LHCF	1	(1/0)

(with Unmaskable / Maskable partition)

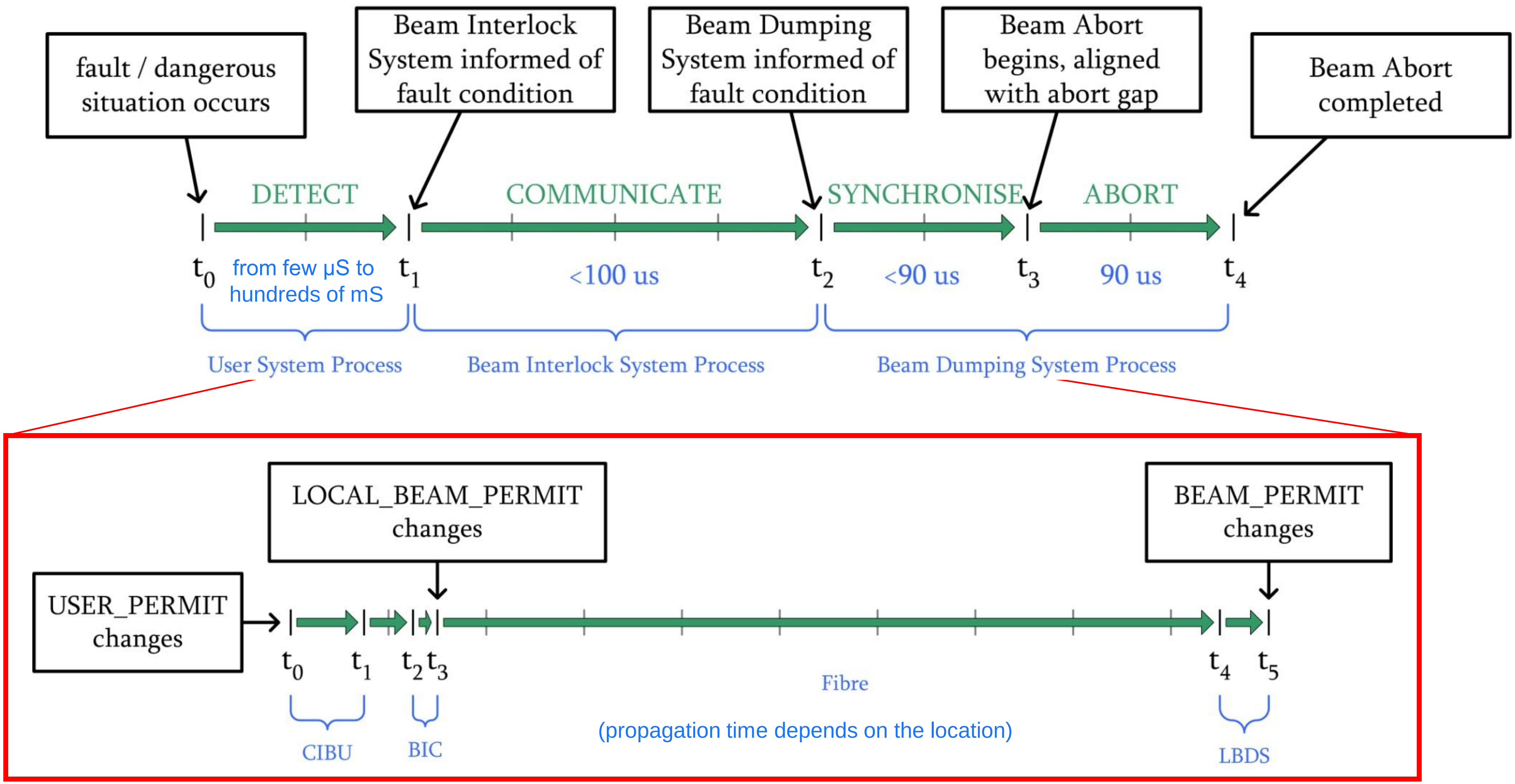
~ 190 connections for LHC-ring BIS

~30 more for Injection BIS

~130 more for the Extraction lines SPS-LHC-CNGS

Machine Protection systems in red

Global response time



Reviews of the Beam Interlock System

- **Internal Review in 2006:**

Audit performed by a team of experts (*) external to the BIS team.

<< Generally, we found that the design and implementation of the BIS is sound, complete, straight-forward, and, in particular, conform to the requirement on a high inherent level of safety, reliability and availability >>*

Recommendations have been made

=> all have been applied in the following months

(*) Matthias.Werner@desy.de **+** Reiner Denz; Philippe Farthouat; Stefan Lueders; Javier Serrano; Yves Thurel

- **External Review in 2009:**

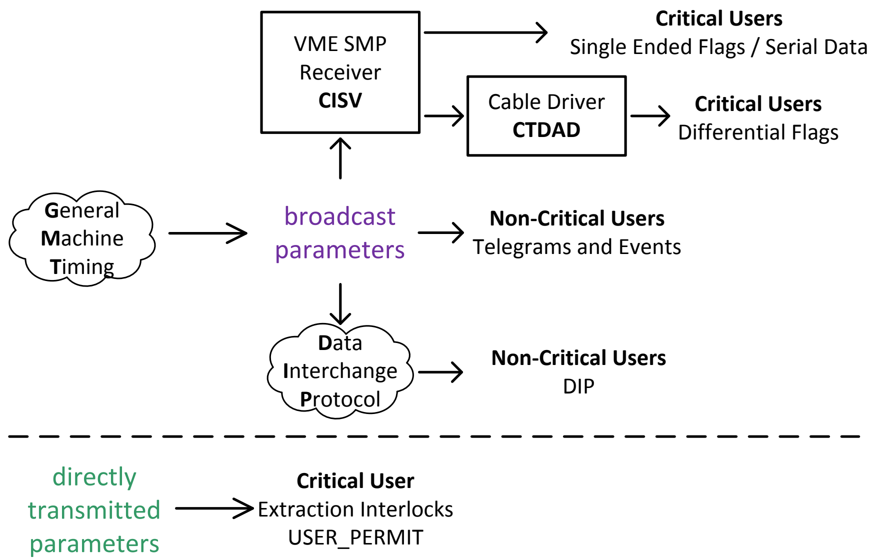
Performed by Critical Systems Labs, Inc. (Canada)

<< … CSL has found nothing in the design of the BIS that suggests a possible weakness with the potential to jeopardize the safety function of the BIS. Subject to the limitations of this review with respect to scope and resources, CSL concludes that there is sufficient reason to be confident that the BIS will perform its intended safety function… >>

Recommendations have been made. None is critical.

SMP Distribution

- User systems can receive SMPs using different methods, being classed as **Critical** or **Non-Critical**:



- Directly transmitted to Critical Users:
  - by hard-wired links (both Extraction beam controllers)
  - via **G**eneral **M**achine **T**iming; then a dedicated VME SMP receiver board (**CISV**) and optional differential driver board can be used

SMP: Validation and operational checks

Foreseen for 2011:

PRE-OPERATIONAL CHECKS: at regular intervals, tests are performed to ensure critical paths are working to specification.

DIAGNOSIS AND MONITORING: checks effecting dependability, such as:

- Infrastructure issues
- Source system input status changes
- Internal system status changes
- Transmitted information status changes

POST-OPERATIONAL CHECKS:

Post-operational check sequence integrated into the **Post-Mortem** system

This sequence is to verify:

- Redundancy was functionally correct
- Role played in the last beam abort.
- Connection to LHC-BIS: (once mature enough) the goal is to inhibit the operation of LHC in the case of a serious problem being observed)

ON-DEMAND TESTING:

Designed for testing without putting the LHC in a dangerous situation.

For example, SMP may be duplicated into redundant A and B values, where one of these at a time could be forced into an unsafe condition for testing purposes.