Tests for preparing the GaAs test beam at DESY

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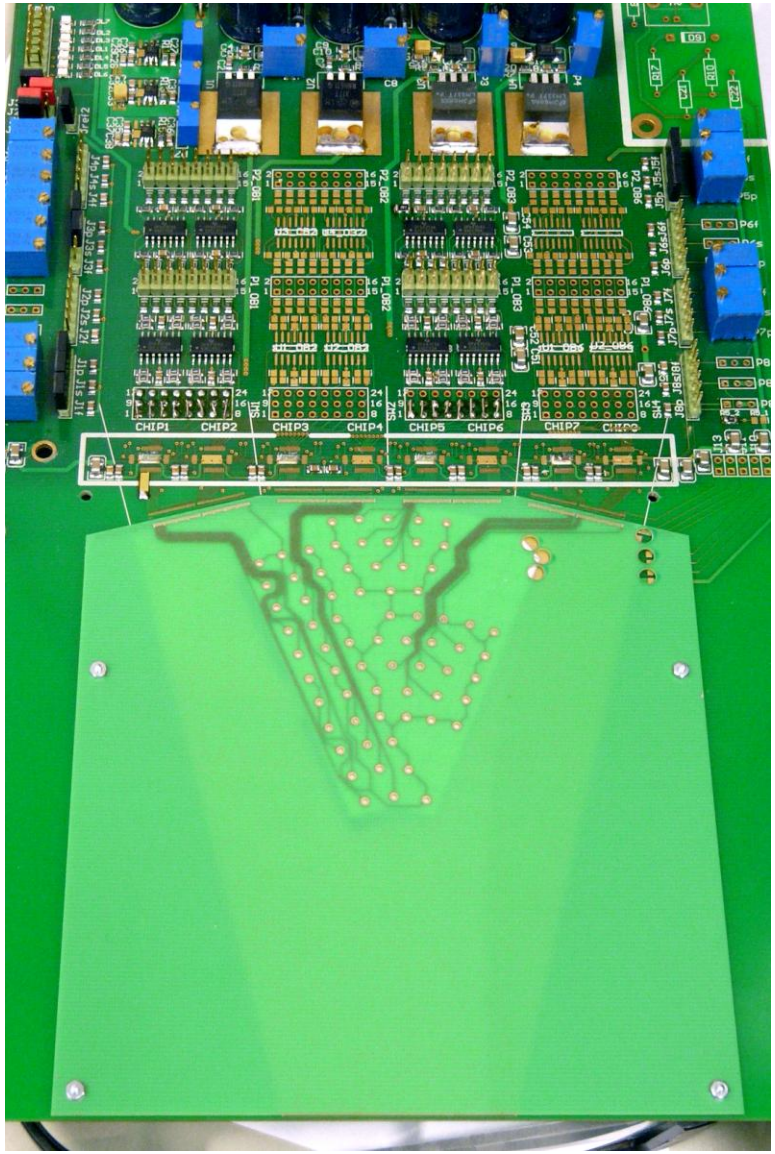
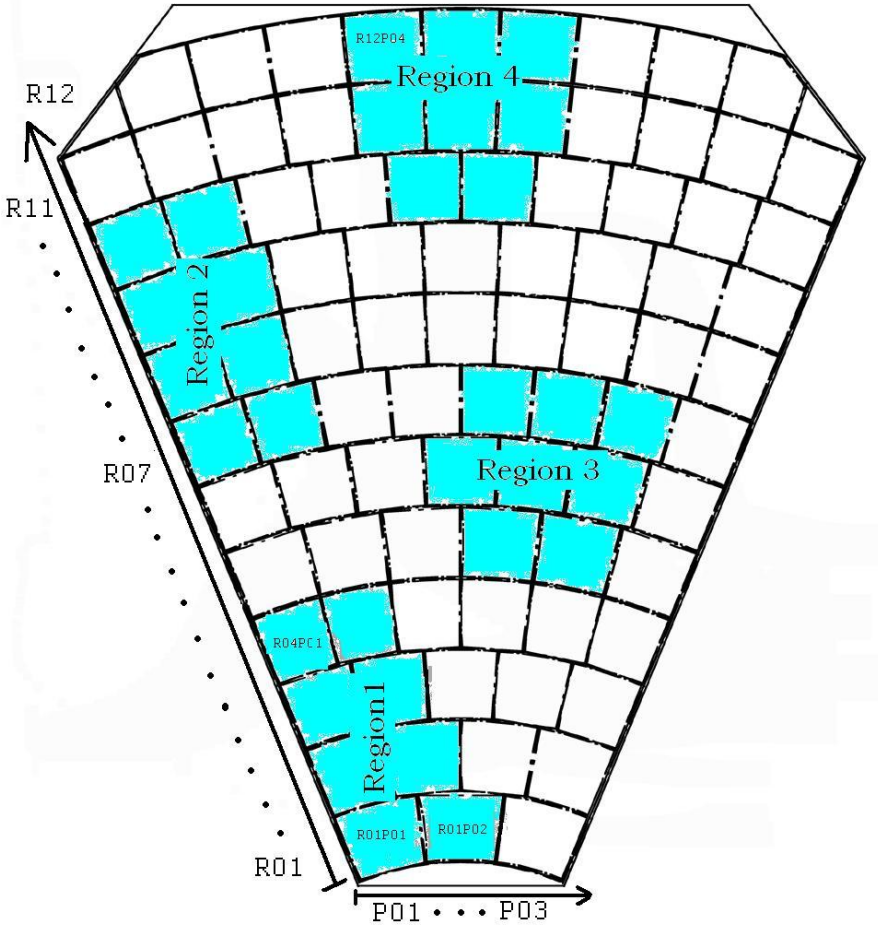
Outline

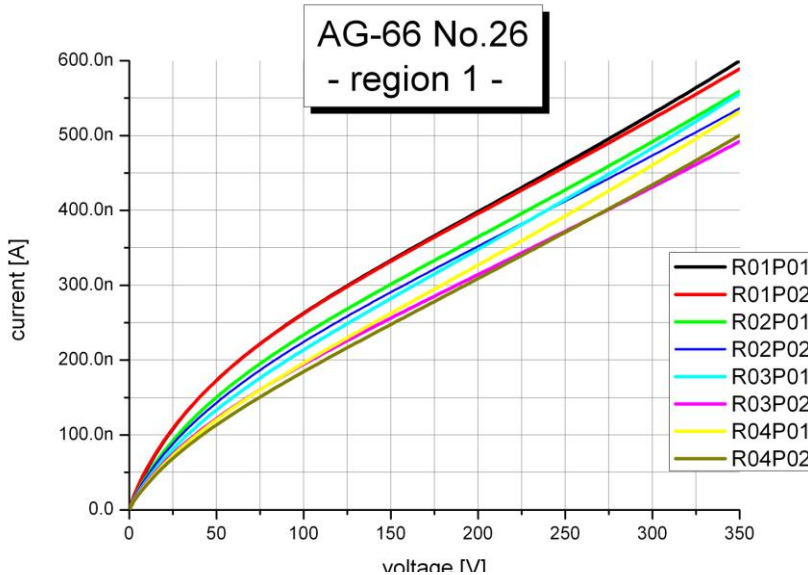
- GaAs detectors
  - IV-measurements
- Fanout
  - Capacitance measurements
- Readout chips
  - linearity test
  - signal size
  - signal to noise
  - calibration

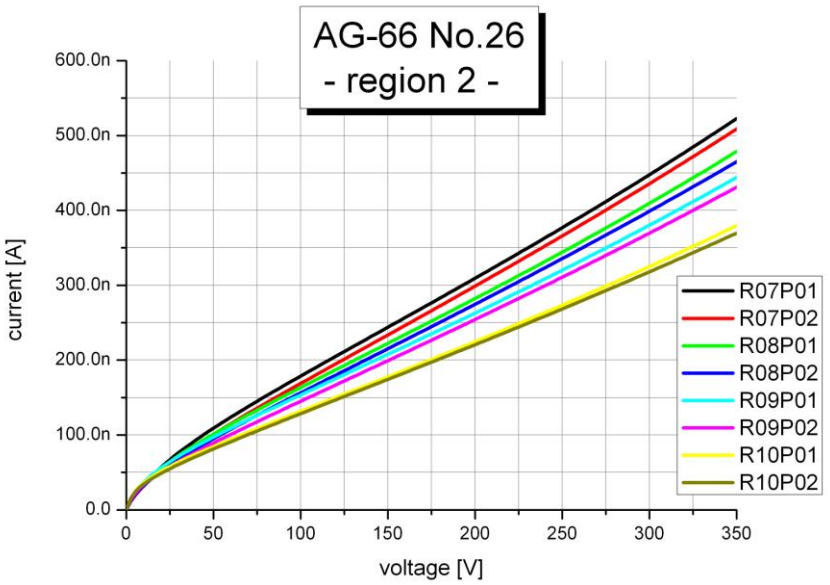


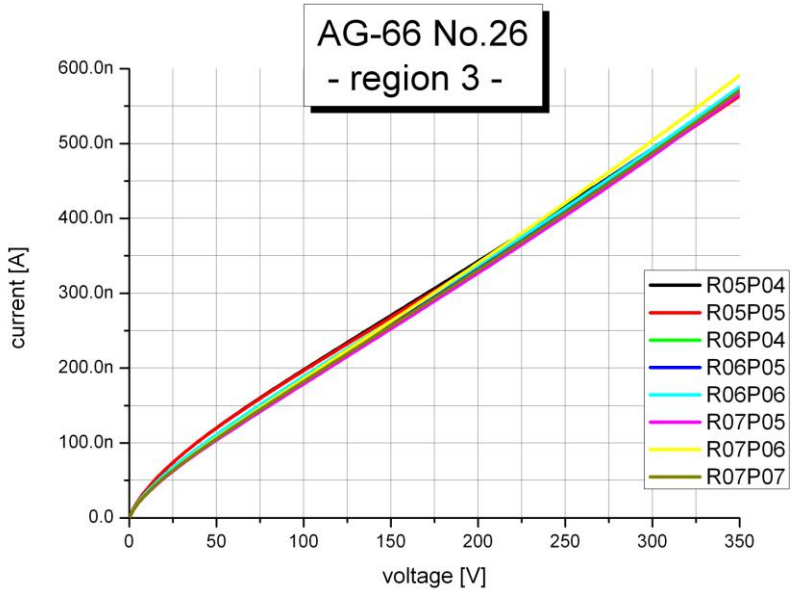
GaAs-sensors: IV-measurements

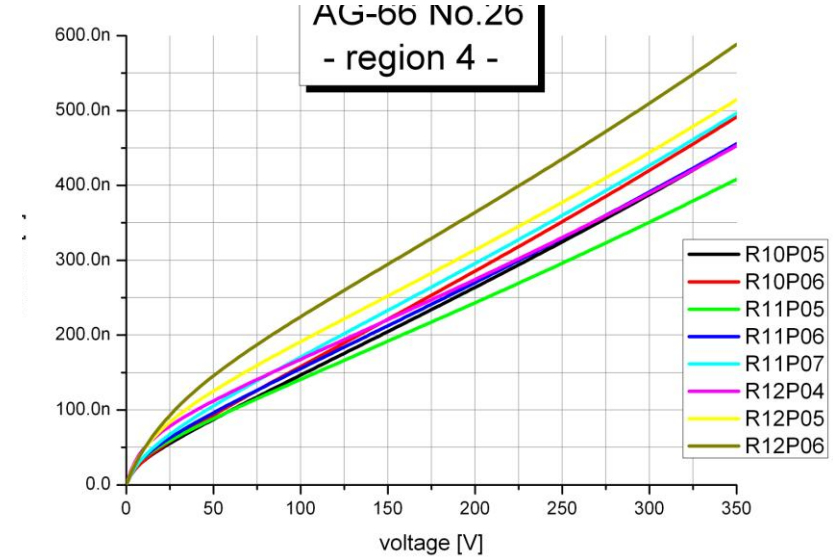
- was planned to irradiate 32 pads in 4 clusters in the test beam
- have five GaAs-sensor prototypes (AG-66/7; AG-66/21; AG-66/26; AG-66/34 and AG-84/5)
- measured IV-curves for all 32 pads for each sensor
- applied voltages:
  - 0V … 350V
  - 2.5V-steps







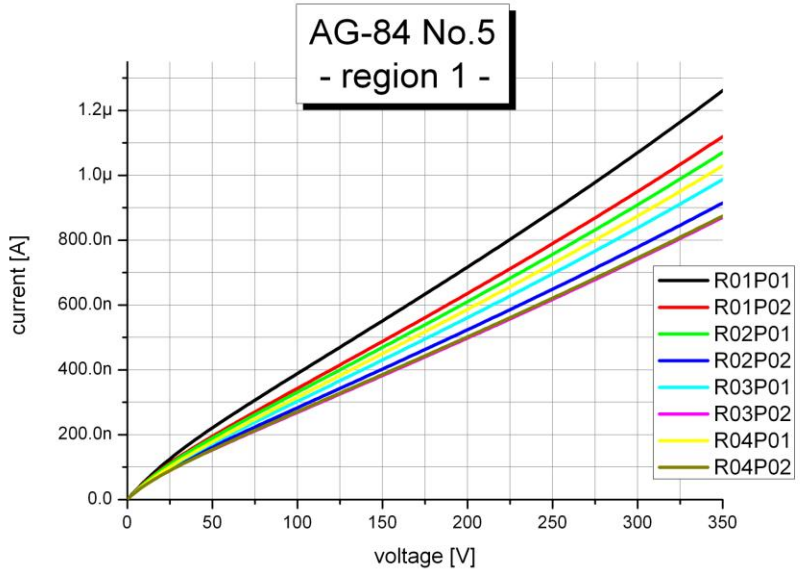


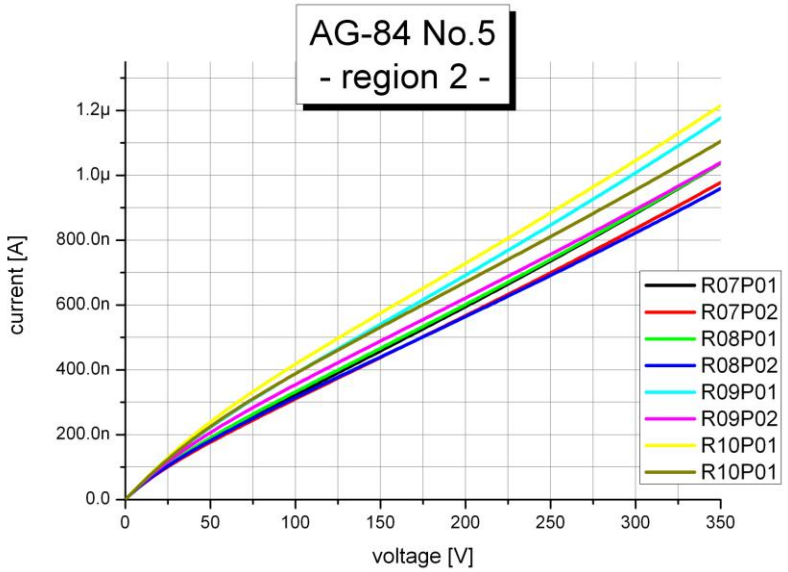


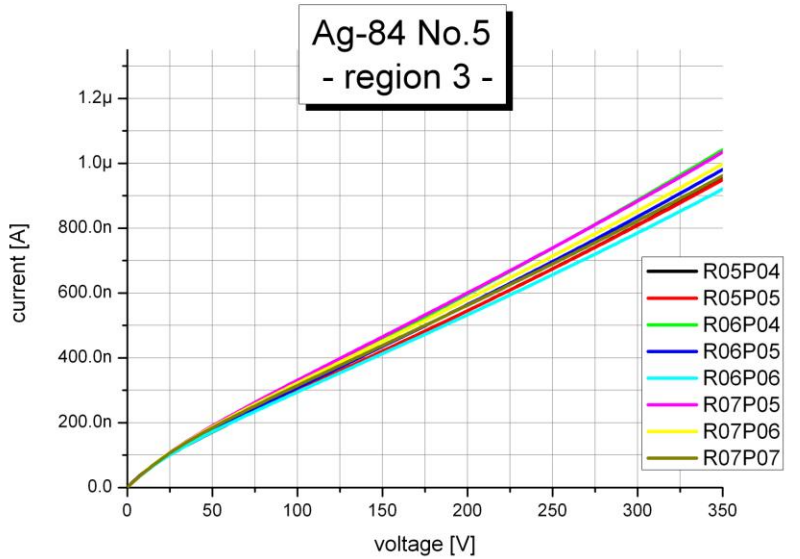
stats @ 350V:

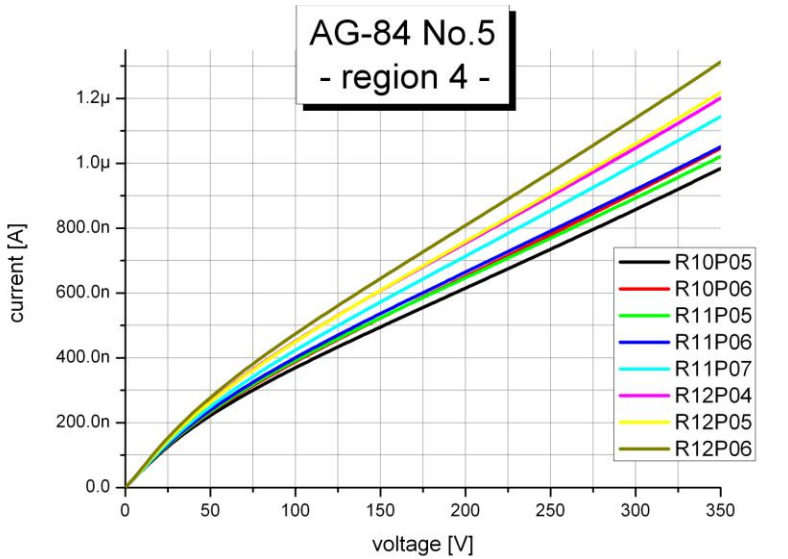
min: 370 nA average: 513 nA

max: 600 nA variation: 38.4%









stats @ 350V:

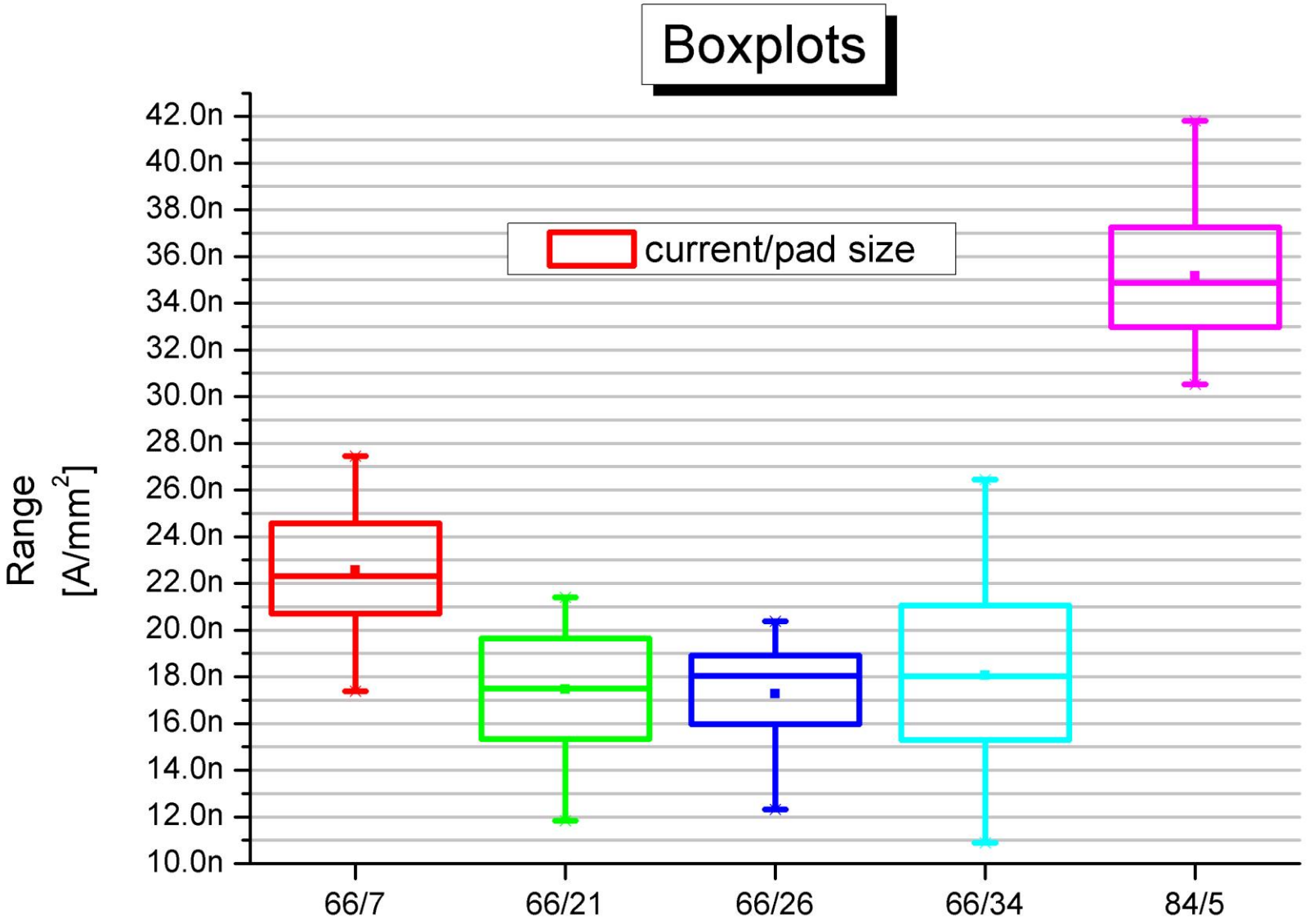
min: 870 nA average: 1.05 µA

max: 1.31 µA variation: 33.7%

Comparison of the sensors

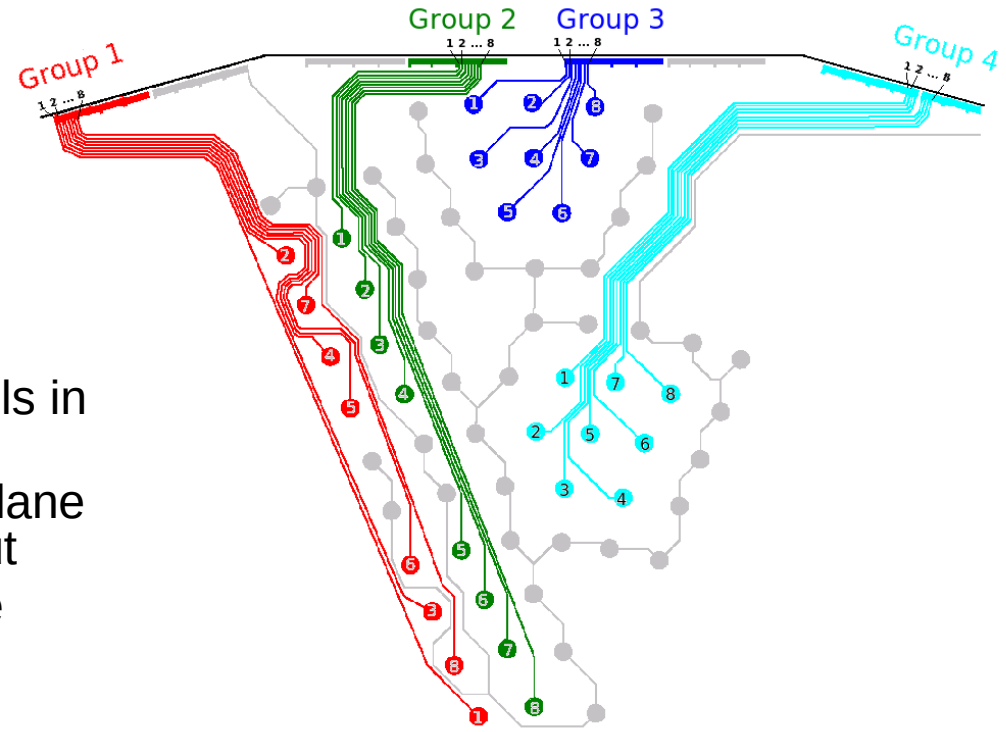
- pad sizes differs in a range of 15%
- for comparison the current at 350V was divided by pad size

current per pad size		
sensor	arithmetic mean	standard deviation
	[nA/mm²]	[nA/mm²]
66/7	22.57	2.63
66/21	17.47	2.53
66/26	17.26	2.19
66/34	18.05	4.05
84/5	35.15	3.02


Boxplots
current/pad size
Range
[A/mm^2]
42.0n
40.0n
38.0n
36.0n
34.0n
32.0n
30.0n
28.0n
26.0n
24.0n
22.0n
20.0n
18.0n
16.0n
14.0n
12.0n
10.0n
66/7
66/21
66/26
66/34
84/5

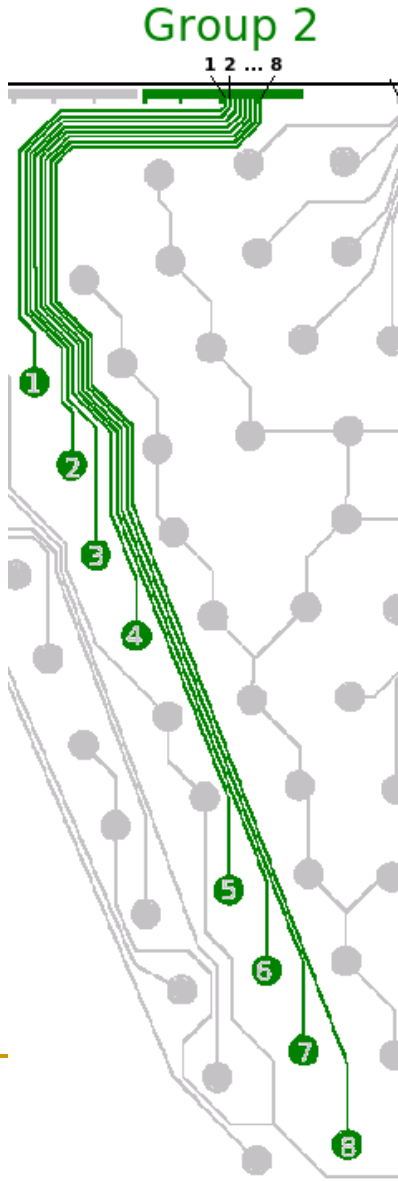
Fanout: capacitances

- Measurement device:
  - C-Meter (Hewlett Packard 4263B LCR Meter)
  - used settings:
    - 1000 mV amplitude
    - 100 kHz frequency
- Measurements for group 2:
  - capacitance between one channel and all other channels in parallel
  - one channel vs. all + metal plane on the backside of the Fanout
    - metal plane simulates the metalized surface of the sensor



Fanout: capacitances

Group 2			
channels	capacitance [pF]	channels	capacitance [pF]
5 vs all	3.53	5 vs all+BP	4.47
6 vs all	3.98	6 vs all+BP	4.95
7 vs all	4.32	7 vs all+BP	5.26
8 vs all	2.90	8 vs all+BP	4.68



- largest measured capacitance was 5.26 pF for “channel 7 vs all+BP”

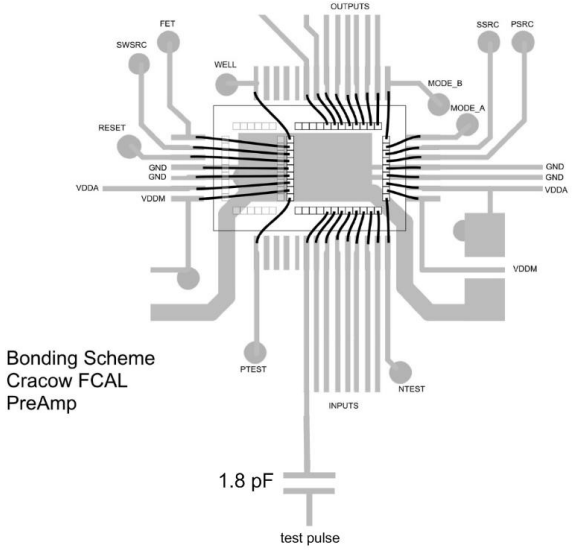
BP = Back Plain (metal plain on the backside of the Fanout)

tests on the readout chips

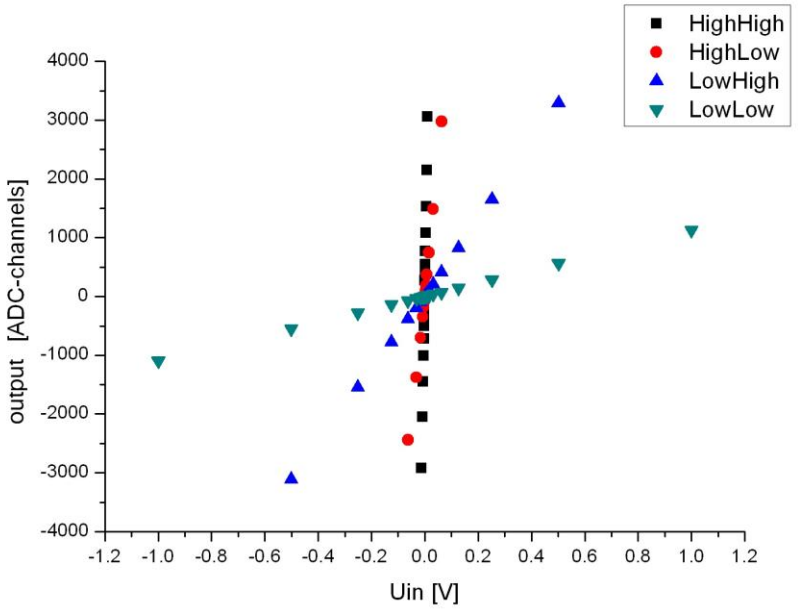
- chips have four possible gain settings
  - preamplifier: High or Low
  - shaper: High or Low
- chip 1, chip 3, chip 5 were bonded so far
- Linearity test:
  - for channel 0, chip 1
  - for all four gain settings (HighHigh, HighLow, LowHigh, LowLow)
- calibration measurements:
  - signal size at fixed input voltage
  - signal to noise
  - done for all channels, all chips and three gain settings (HighHigh, HighLow, LowHigh)
- DAQ:
  - 8 channel charge integrating ADC (C.A.E.N. V265)

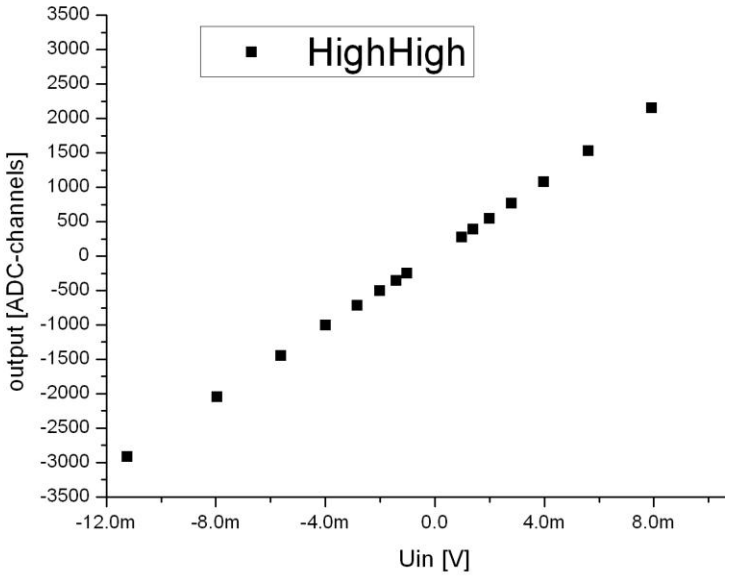
Linearity test

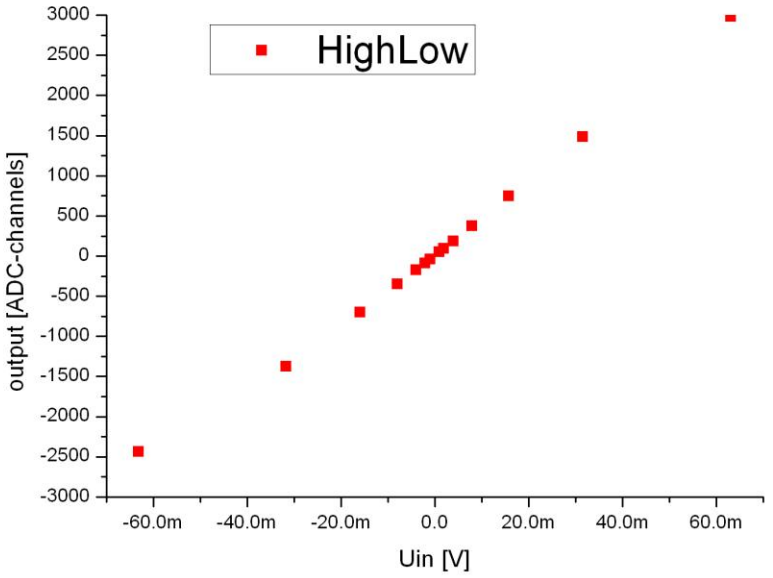
- sent test pulses from a pulse generator to channel 0, chip 1
- bonded a capacitor (1.8 pF) directly to chip input
- so we know the input charge from input voltage

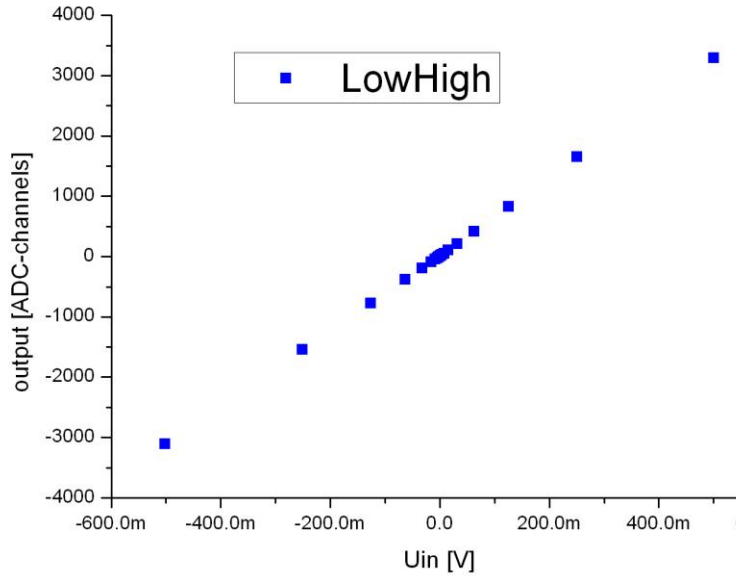


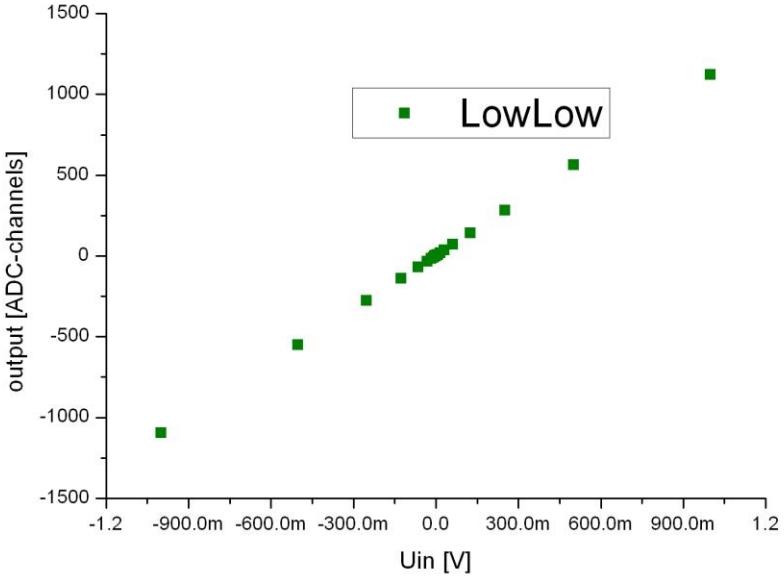
- +/-1V pulses by generator
- used attenuator to vary input voltage
  - from 0 dB in 3dB- or 6dB-steps
  - 110dB for pedestal measurements
- converter between board output and ADC input for positiv test pulses (ADC needs negativ input)




HighHigh
output [ADC-channels]
Uin [V]
3500
3000
2500
2000
1500
1000
500
0
-500
-1000
-1500
-2000
-2500
-3000
-3500
-12.0m
-8.0m
-4.0m
0.0
4.0m
8.0m

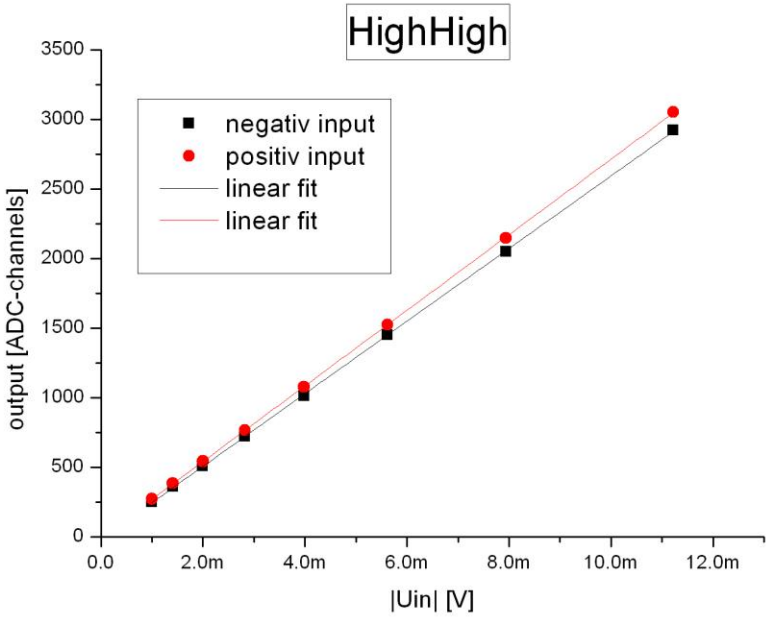

HighLow
output [ADC-channels]
Uin [V]
3000
2500
2000
1500
1000
500
0
-500
-1000
-1500
-2000
-2500
-3000
-60.0m
-40.0m
-20.0m
0.0
20.0m
40.0m
60.0m


LowHigh
output [ADC-channels]
Uin [V]
4000
3000
2000
1000
0
-1000
-2000
-3000
-4000
-600.0m
-400.0m
-200.0m
0.0
200.0m
400.0m


LowLow
output [ADC-channels]
Uin [V]
1500
1000
500
0
-500
-1000
-1500
-1.2
-900.0m
-600.0m
-300.0m
0.0
300.0m
600.0m
900.0m
1.2

Calibration factors

- separately linear fits for positive and negative input voltage

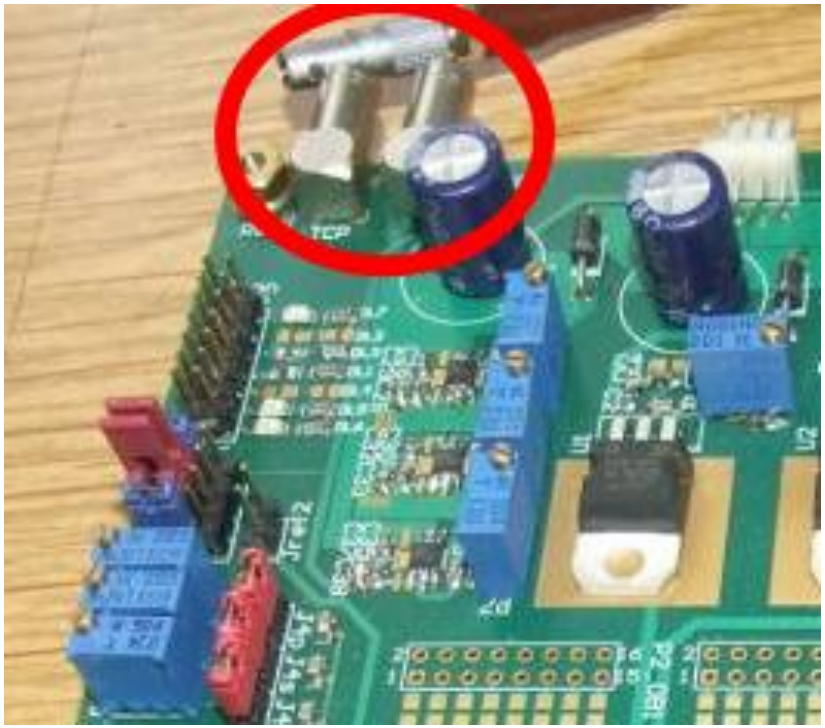


	Negative Uin	Positiv Uin
	[ADC-ch./V]	[ADC-ch./V]
HighHigh	261 057	271 703
HighLow	(43 709)*	47 183
LowHigh	6 205	6 572
LowLow	1 098	1 122

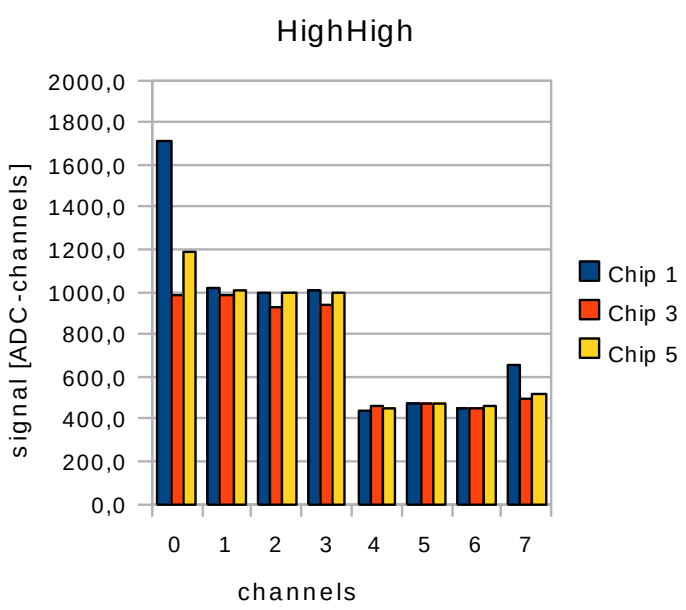
*without the value at -63 mV

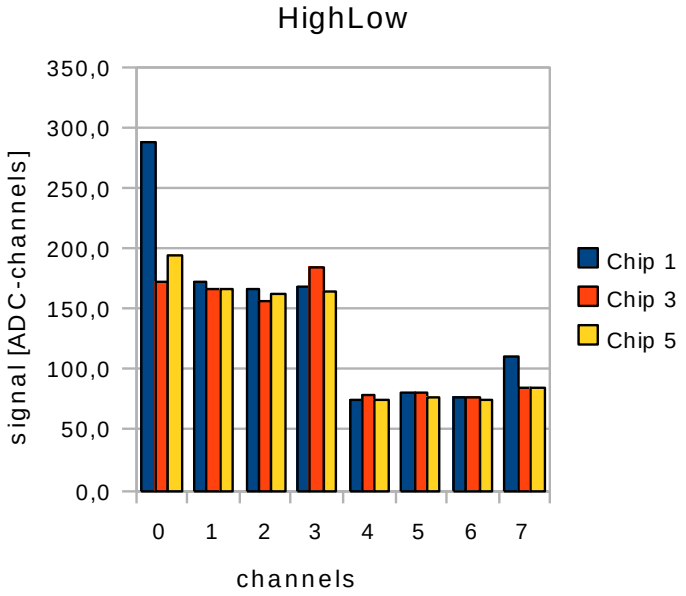
Calibration measurements

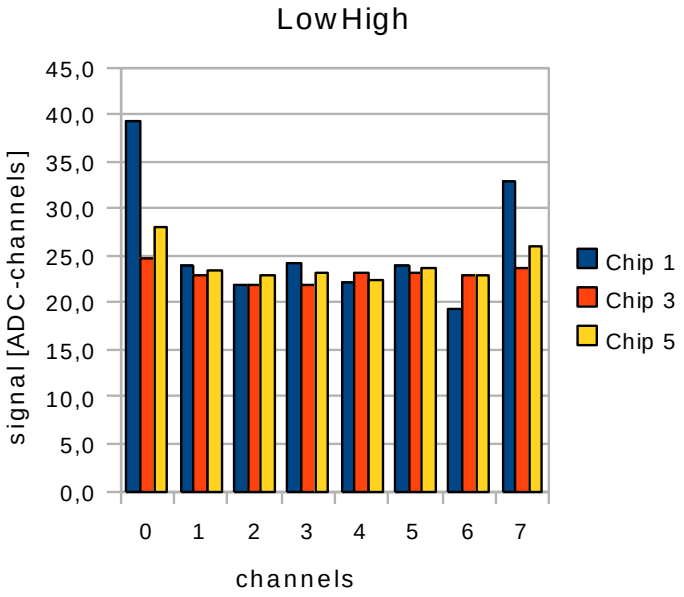
- in principle the same setting as before
- external capacitor was removed
- test pulses now send to board input
  - two inputs: one for even and one for odd channels
  - input pulse to 4 channels at the same time
- fixed negative input voltage (42dB = -7.9mV)
- measured all channels, all channels, three gain settings



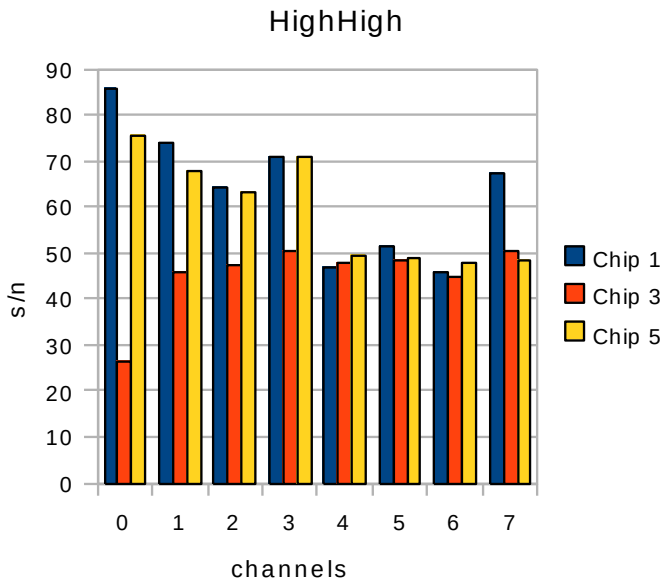
Signal size

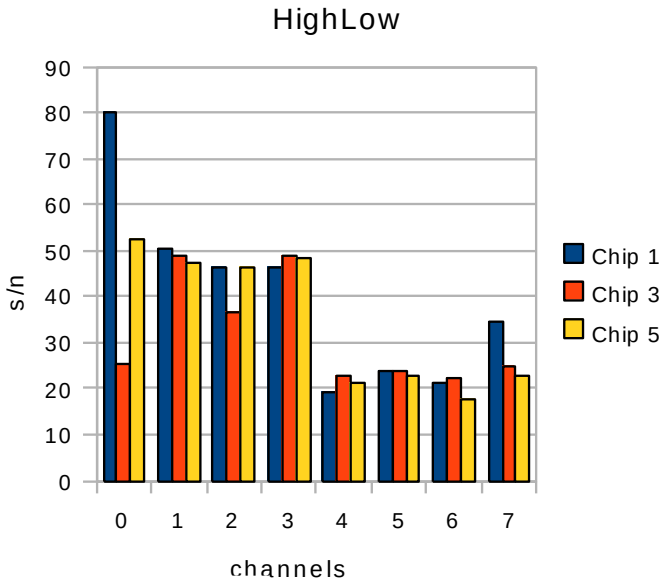

HighHigh
2000,0
1800,0
1600,0
1400,0
1200,0
1000,0
800,0
600,0
400,0
200,0
0,0
signal [ADC-channels]
0 1 2 3 4 5 6 7
channels
Chip 1
Chip 3
Chip 5

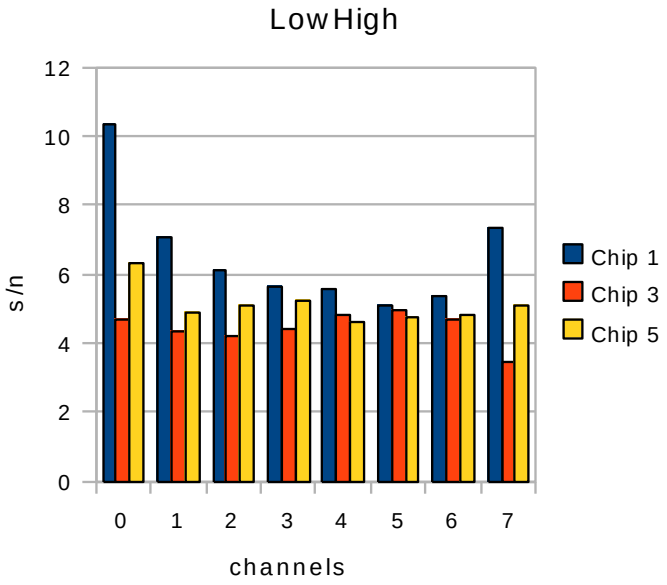

HighLow
350,0
300,0
250,0
200,0
150,0
100,0
50,0
0,0
signal [ADC-channels]
0 1 2 3 4 5 6 7
channels
Chip 1
Chip 3
Chip 5


LowHigh
45,0
40,0
35,0
30,0
25,0
20,0
15,0
10,0
5,0
0,0
signal [ADC-channels]
0 1 2 3 4 5 6 7
channels
Chip 1
Chip 3
Chip 5

Signal to noise







Calibration measurements

- idea was to have full calibration with:
  - linearity test on one channel for all gains
  - calibration factors for this channel
  - expect also linearity in all other channels
  - one signal size measurement at fixed input voltage for all channels in all chips
- but channel 0 in chip 1 showed much higher signals
- also different S/N-values for chip 3
- better to have linearity tests for all channels

Summery

- different measurements for test beam preparation were done
- IV-measurements for sensors:
  - comparison of the 5 sensors -> choice for test beam
  - check if pads are damaged
  - know dark current for each pad
- Capacitance measurement for Fanout
  - for cross talk estimation
- Tests for readout chips
  - linearity test and calibration measurement for one channel
  - comparison of signal size and signal to noise for all channels, all chips
  - estimation for calibration for all channels

Thank you