BLM Threshold Comparator Module

LHC BLM system audit – 08/11/2010

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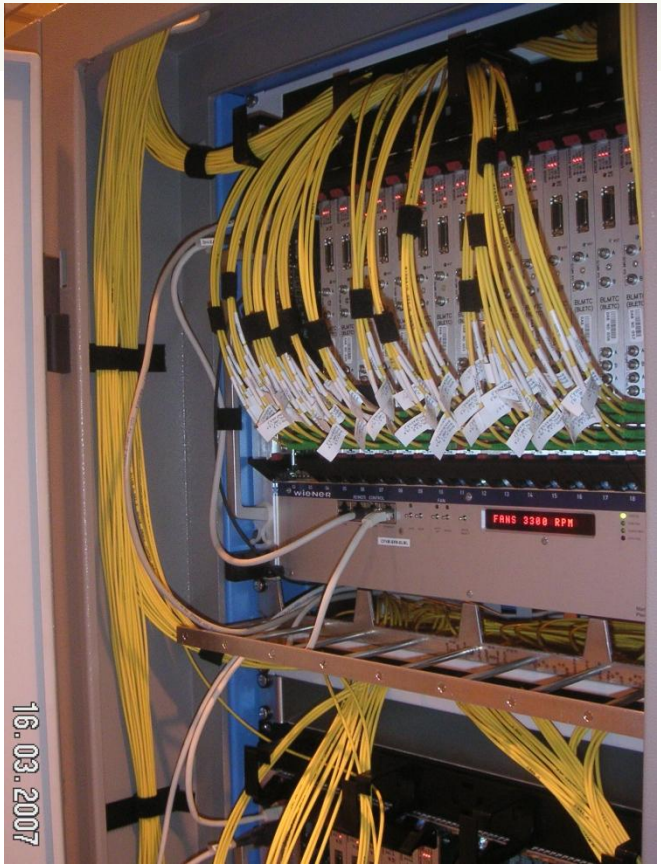
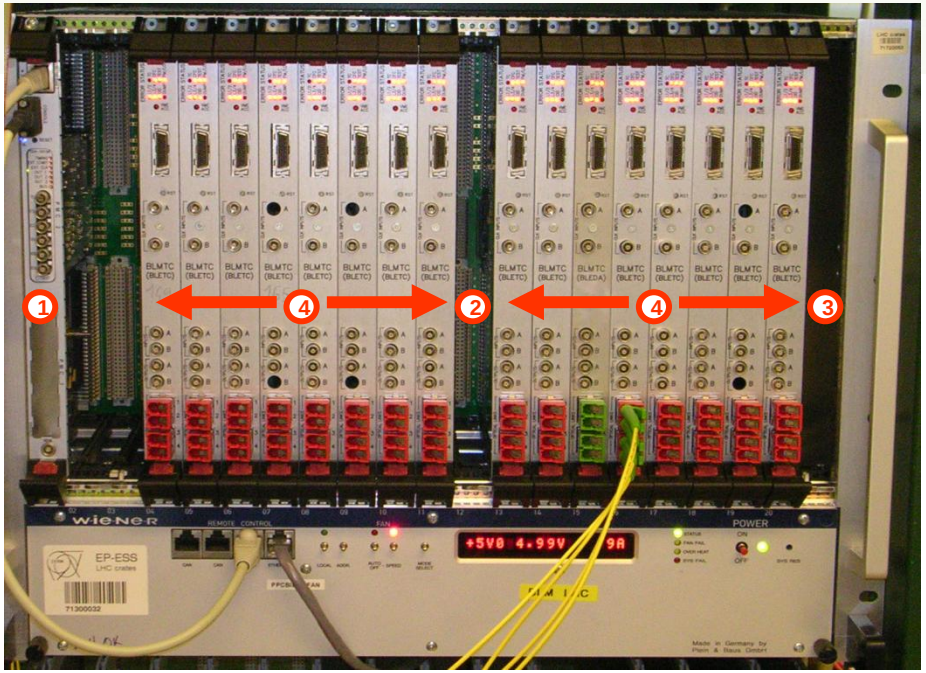
Outline

- Surface configuration
- Data Processing Overview
- Steps taken for a Failsafe System
- Verification techniques used
- Production and Installation
- Data Output
- Changes since last Audit

Surface configuration





1) FEC/CTRP – CPU / GMT timing
2) BOBR – BST timing
3) BLECS - Combiner & Survey
4) BLETC – Threshold Comparator

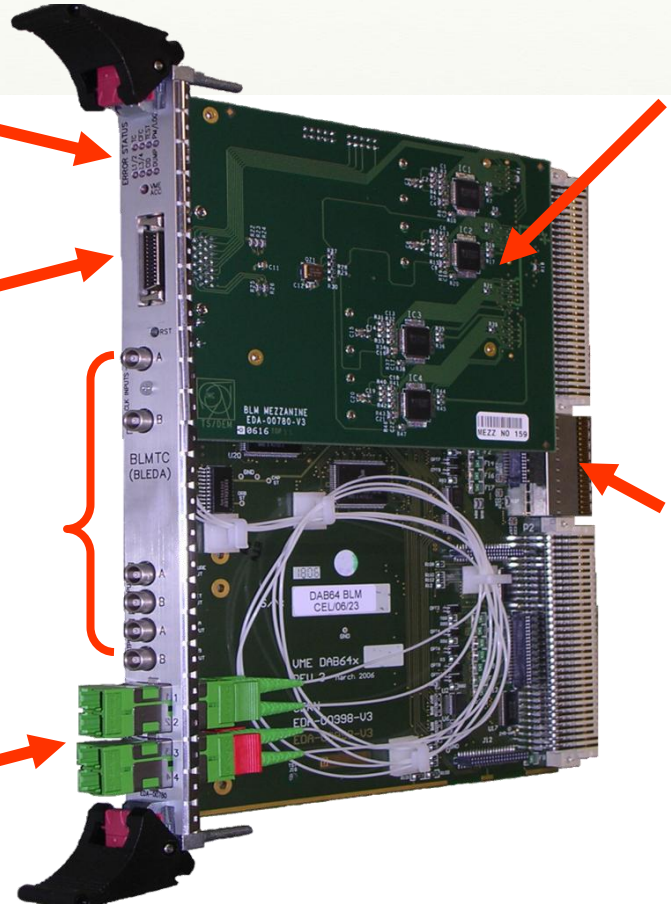
BLETC Module (1)

LEDs showing system and communication status

Connector to program the FPGA & Configuration device.

LEMO connectors for accessing some FPGA I/Os.

E2000-APC input connections to four optical fibres.

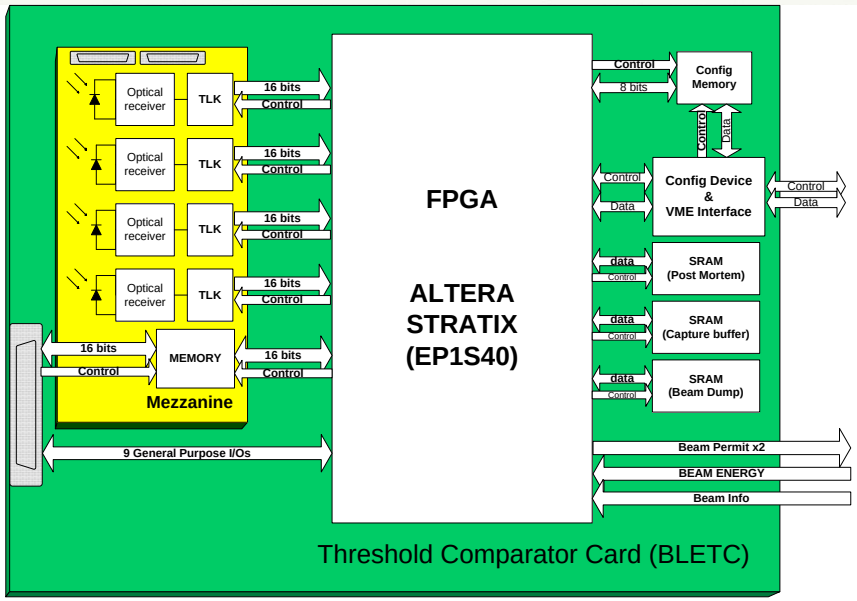


The **BLM Mezzanine** is hosting the receiver parts for four optical links. It handles the de-serialization and decoding of the optical gigabit data transmission lines in parallel and provides the received data to the DAB64x card's FPGA device for processing.

The **P0** connector is on a custom-made backplane.

It daisy-chains, the two beam permit lines and provide the beam energy data input.

BLETC Module (2)



DAB64x specifications

- Stratix FPGA
  - Vertical Migration to EP1S40
- SRAM memories (x3)
  - 512K x 32bit
- Connectors for Mezzanine
  - 2 x 64pin PMC connectors
  - Provide 3.3V, 5V, GND, and
  - Connection to 114 FPGA I/Os
- Communication bus
  - VME64x

	FPGA Device	
Feature	**EP1S20**	**EP1S40**
Logic Elements (LEs)	18,460	41,250
M512 RAM Blocks	194	384
M4K RAM Blocks	82	183
M-RAM Blocks	2	4
Total RAM bits	1,669,248	3,423,744
PLLs	6	12
Maximum User I/O Pins	586	615

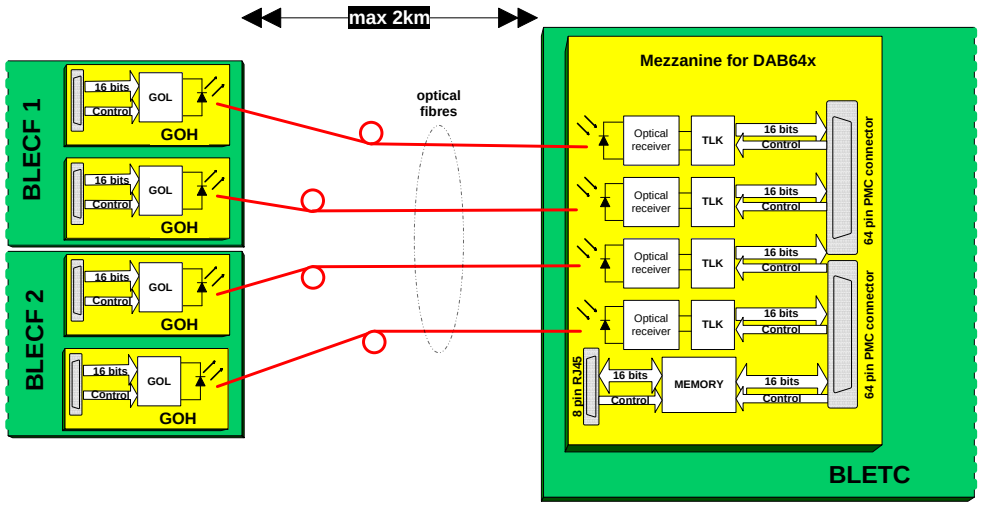
Mezzanine Cards

TUNNEL – GOH (x4)

- Redundant transmission
  - High radiation tolerance
  - > 3 KGray
- 800 Mbps
  - Data 640 Mbps
- 8bit/10bit encoding

SURFACE – BLM Mezzanine

- 4 optical diodes
  - 4 TLK (Texas Instruments) transceivers
- 8bit/10bit decoding
  - Synchronisation
  - Clock extraction
- 1MB non-volatile RAM
  - Programmable via FPGA or RJ45

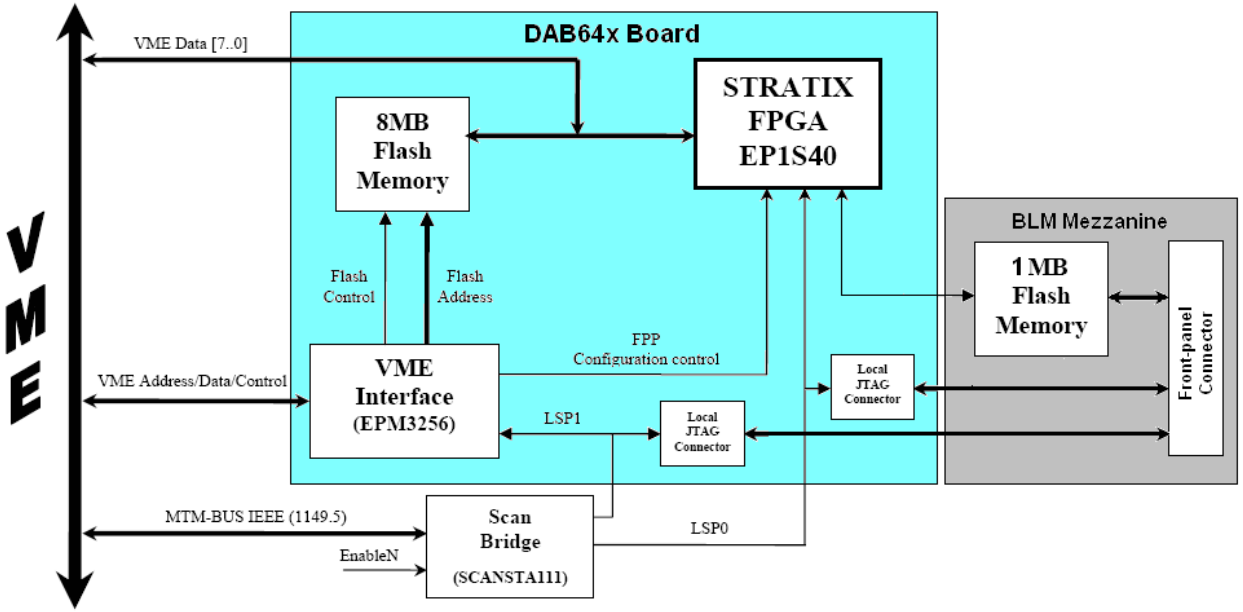


Supported FPGA Configuration modes

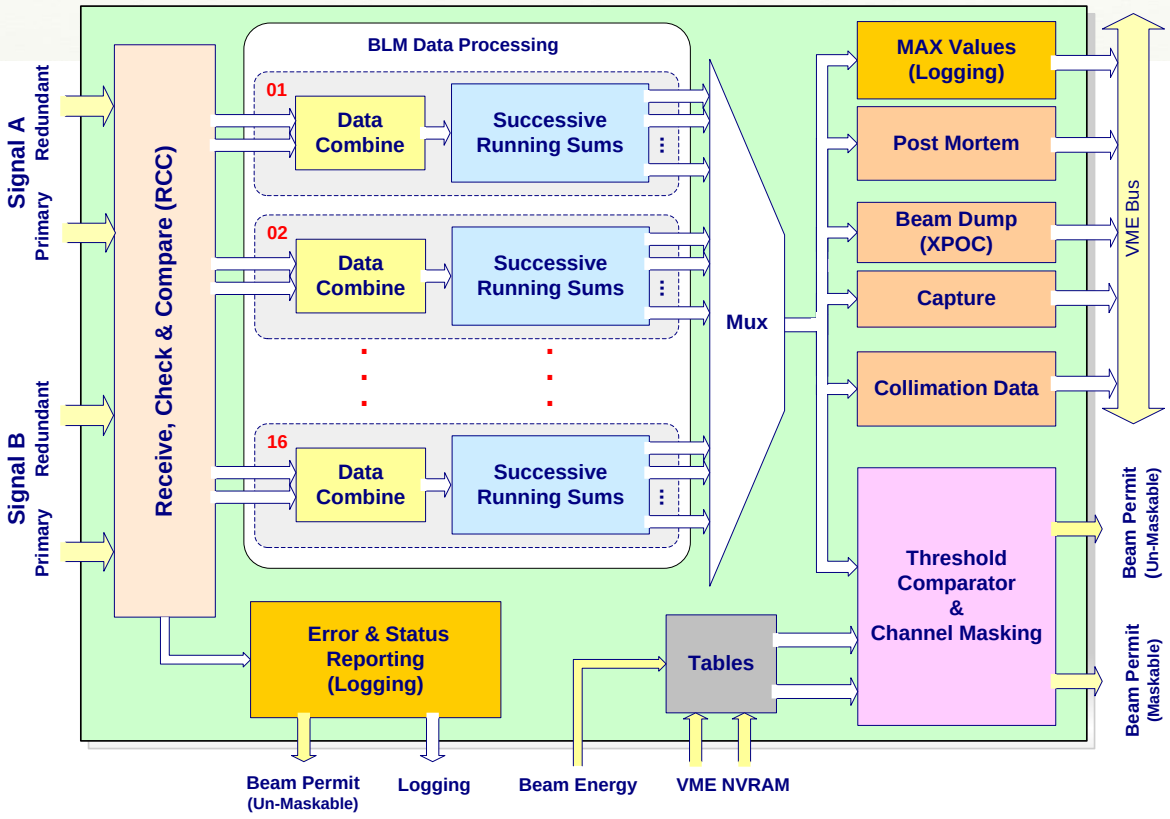
1. FEC
- Save on Flash
- Write to FPGA

2. Power-on
- Boot from Flash
- Script on FEC

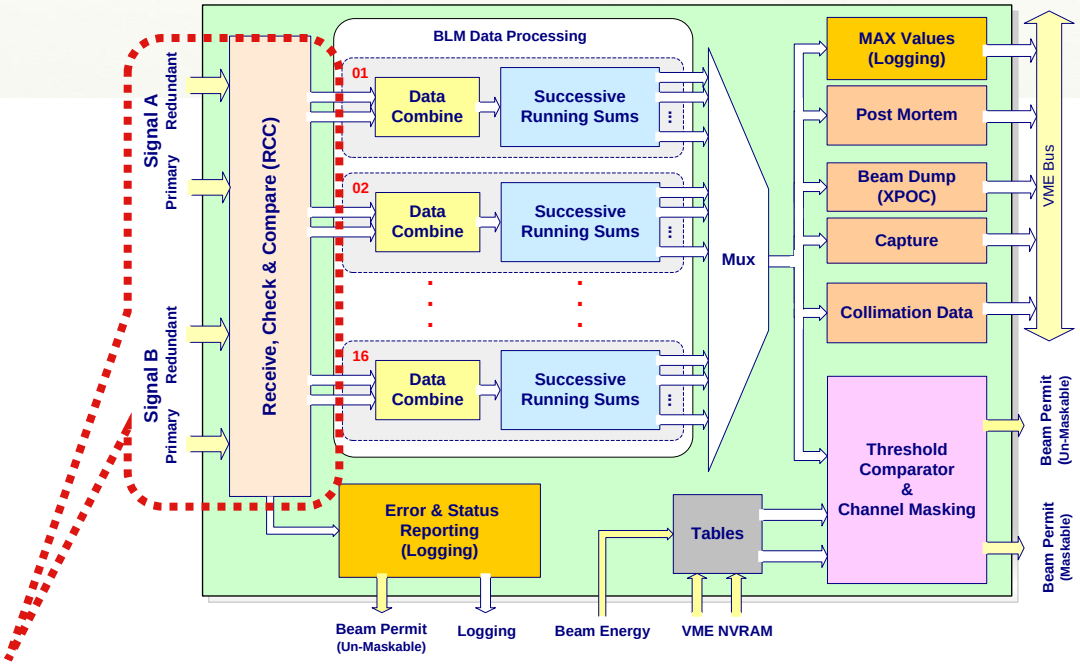
3. Front-panel
- Write to FPGA
- Write to CPLD



Data Processing Overview



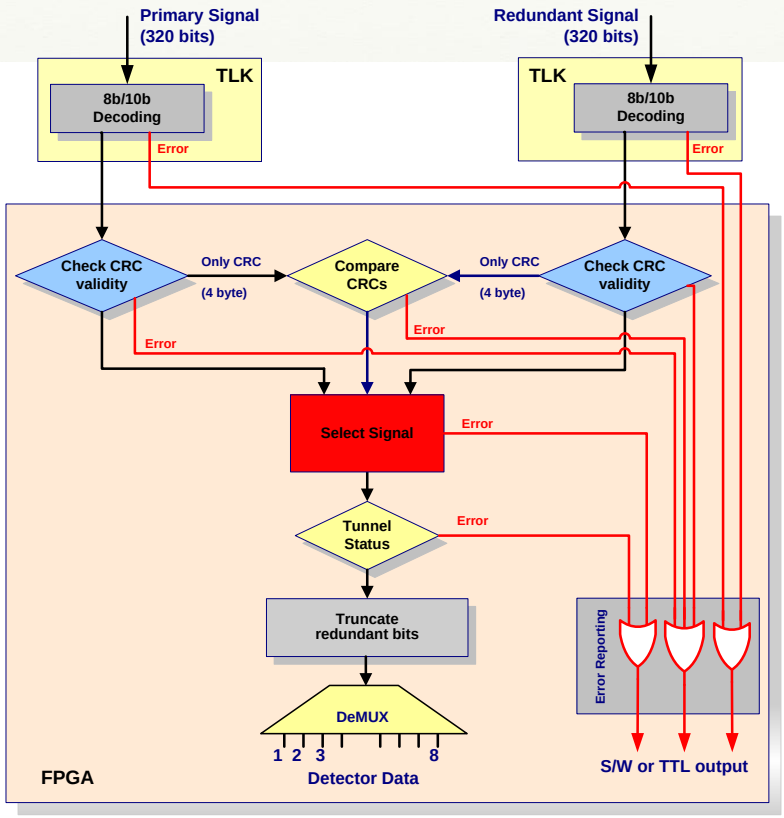
Receive, Check & Compare packets



Receive, Check & Compare (RCC)

- Receives, De-serialises and decodes the transmitted packets.
- Checks for errors using checksums (CRC-32 & 8b/10b).
- Compares the packets coming from the redundant transmission.
- Chooses error free data for further processing.

Transmission & Tunnel Status Check

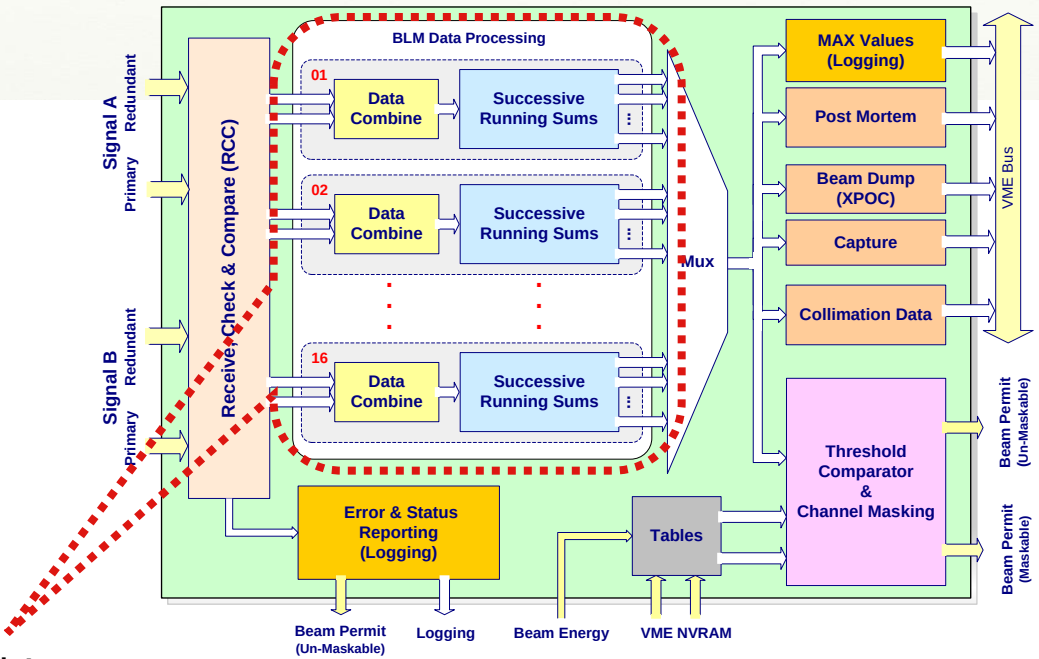


At the Surface FPGA:

- CRC-32
  - Error check / detection algorithm for each of the signals received.
- Comparison of the pair of signals.
- Signal Select block
  - Logic that chooses signal to be used
  - Identifies problematic areas.
  - Increases availability
- Tunnel's Status Check block
  - High Voltage, Power supplies
  - FPGA errors
  - Temperature
  - …

Signal Select Table				
CRC32 check		Comparison of 4Byte CRCs	Output	Remarks
A	B			
Error	Error	Error	Dump	Both signals have error
Error	Error	OK	Dump	S/W trigger (CRCgenerate or check wrong)
Error	OK	Error	Signal B	S/W trigger (error at CRC detected)
Error	OK	OK	Signal B	S/W trigger (error at data part)
OK	Error	Error	Signal A	S/W trigger (error at CRC detected)
OK	Error	OK	Signal A	S/W trigger (error at data part)
OK	OK	Error	Dump	S/W trigger (one of the counters has error)
OK	OK	OK	Signal A	By default (both signals are correct)

Real-Time Analysis of Data



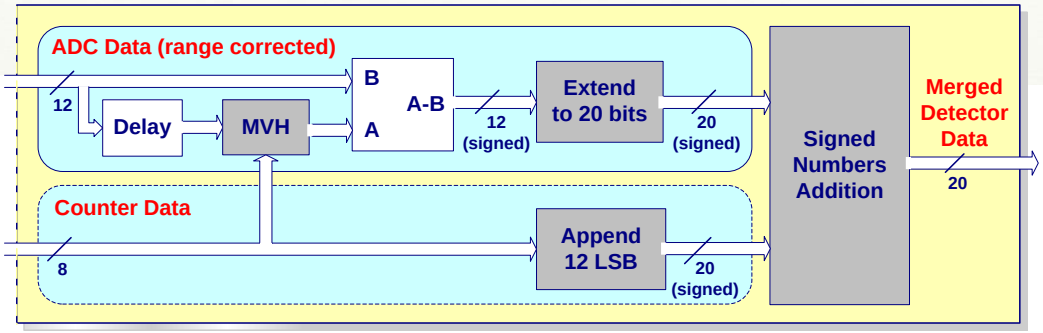
Data-Combine

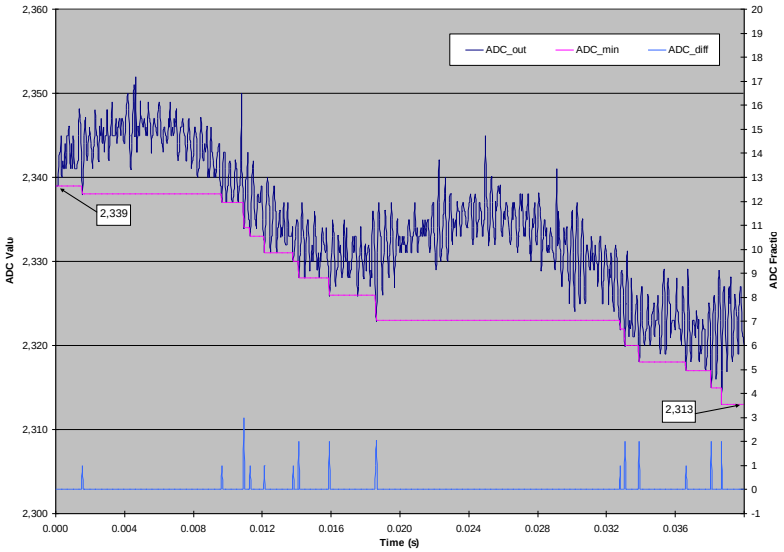
- Applies merging algorithm for the ADC and the CFC data.
- Filters noise.

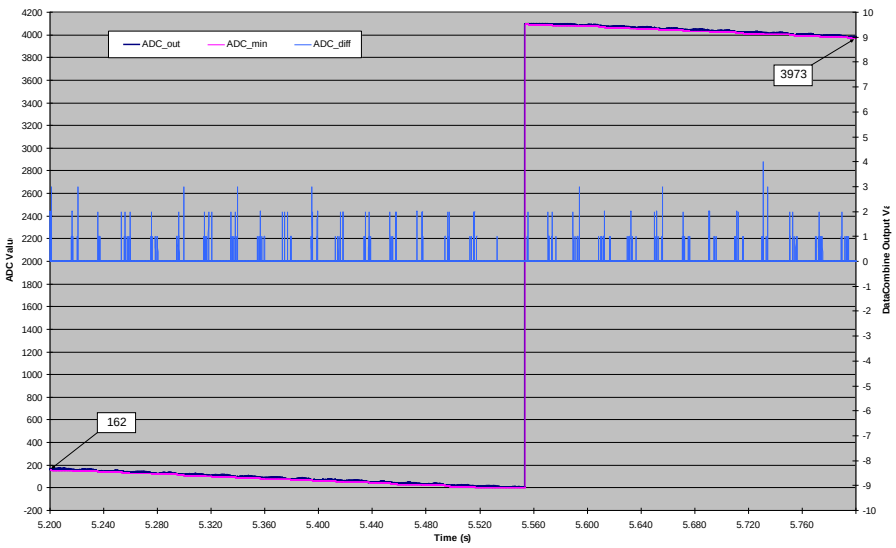
Successive Running Sums (SRS)

- Produces and maintains various histories of the received data in the form of Moving Sum Windows.
- 12 integration periods spanning from 40μs to 84s.

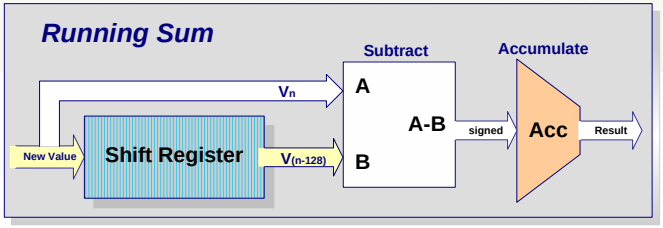
Merging ADC values with Counts







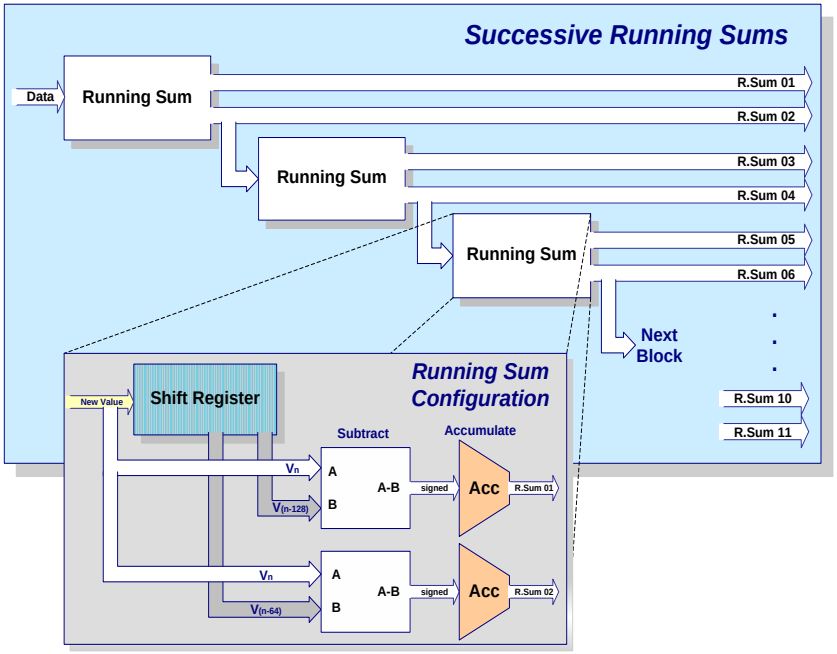
Successive Running Sums (SRS)



- Multi-point Shift Registers holds data
- Successive calculation of Running Sums
- Range 40µs - 84s (12 Running Sums)
- Maximum values of the last second are continuously calculated and kept.

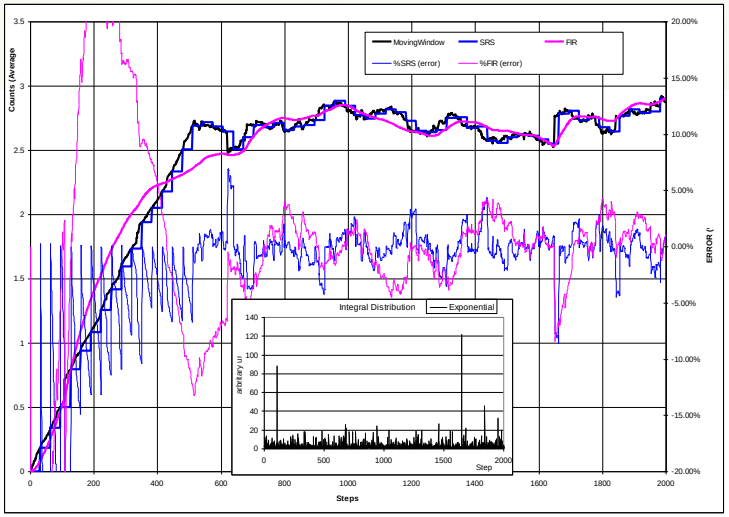
Successive Running Sums configuration

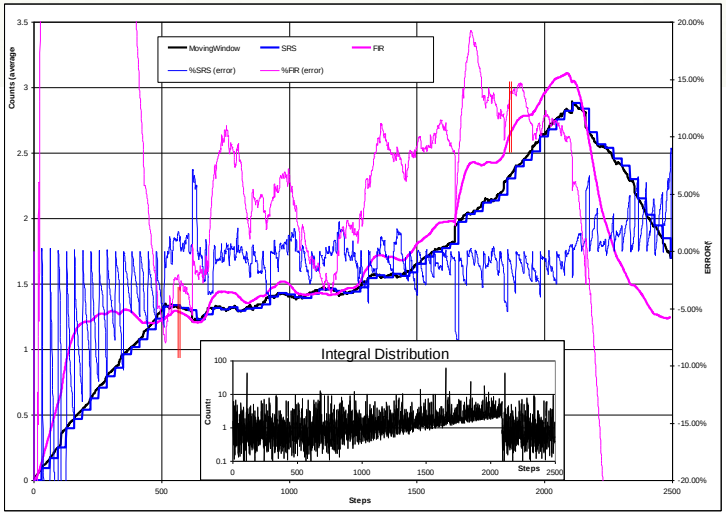
Running Sums		Refreshing		Shift Register Name	Signal Name	bits used
40 µs steps	ms	40 µs steps	ms			
1	0.04	1	0.04	SR0	RS 01	20
2	0.08	1	0.04		RS 02	22
8	0.32	1	0.04	SR1	RS 03	22
16	0.64	1	0.04		RS 04	22
64	2.56	2	0.08	SR2	RS 05	26
256	10.24	2	0.08		RS 06	26
2048	81.92	64	2.56	SR3	RS 07	32
16384	655.36	64	2.56		RS 08	32
32768	1310.72	2048	81.92	SR4	RS 09	36
131072	5242.88	2048	81.92		RS 10	36
524288	20971.5	16384	655.36	SR5	RS 11	40
2097152	83886.1	16384	655.36		RS 12	40



Processing techniques comparison

Study by G. Guaglio





The FIR (2nd order)

- crosses the error line more than once at the maximum 20% relative error allowed by the specifications
- exhibits long periods of over or under-estimation

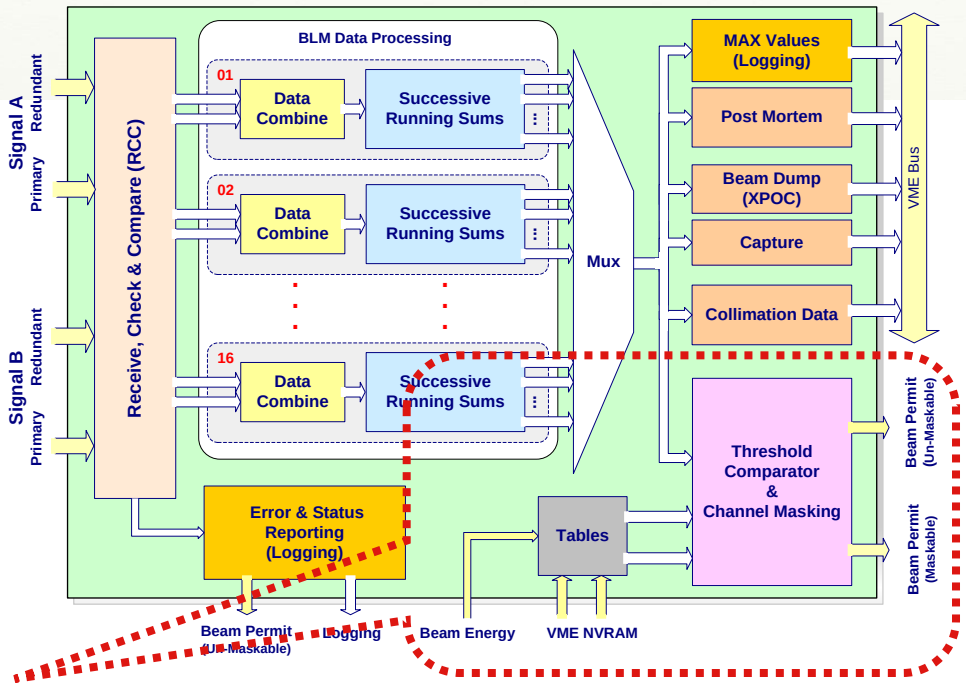
The SRS

- follows closely the losses
- recovers faster

SRS alternate future configurations

Time windows		Refreshing		Single channel width	Shift Register Name	Signal Name
40 µs steps	ms	40 µs steps	ms			
1	0.04	1	0.04	1	SR0	RS1
2	0.08	1	0.04	2		RS2
4	**0.16**	**1**	**0.04**	**4**	**SR1**	***N/C 1***
6	**0.24**	**1**	**0.04**	**6**		***N/C 2***
8	0.32	1	0.04	8		RS3
16	0.64	1	0.04	16		RS4
64	2.56	2	0.08	32	**SR2**	RS5
128	**5.12**	**2**	**0.08**	**64**		*N/C 3*
192	**7.68**	**2**	**0.08**	**96**		*N/C 4*
256	10.24	2	0.08	128		RS6
2048	81.92	64	2.56	32	**SR3**	RS7
4096	**163.84**	**64**	**2.56**	**64**		*N/C 5*
6144	**245.76**	**64**	**2.56**	**96**		*N/C 6*
8192	**327.68**	**64**	**2.56**	**128**		*N/C 7*
10240	**409.6**	**64**	**2.56**	**160**		*N/C 8*
12288	**491.52**	**64**	**2.56**	**192**		*N/C 9*
14336	**573.44**	**64**	**2.56**	**224**		*N/C 10*
16384	655.36	64	2.56	256		RS8
32768	1310.72	2048	81.92	16	**SR4**	RS9
65536	**2621.44**	**2048**	**81.92**	**32**		N/C 11
98304	**3932.16**	**2048**	**81.92**	**48**		N/C 12
131072	5242.88	2048	81.92	64		RS10
524288	20971.52	16384	655.36	32	**SR5**	RS11
1048576	**41943.04**	**16384**	**655.36**	**64**		*N/C 13*
1572864	**62914.56**	**16384**	**655.36**	**96**		*N/C 14*
2097152	83886.08	16384	655.36	128		RS12

To BeamDump on not to BeamDump?



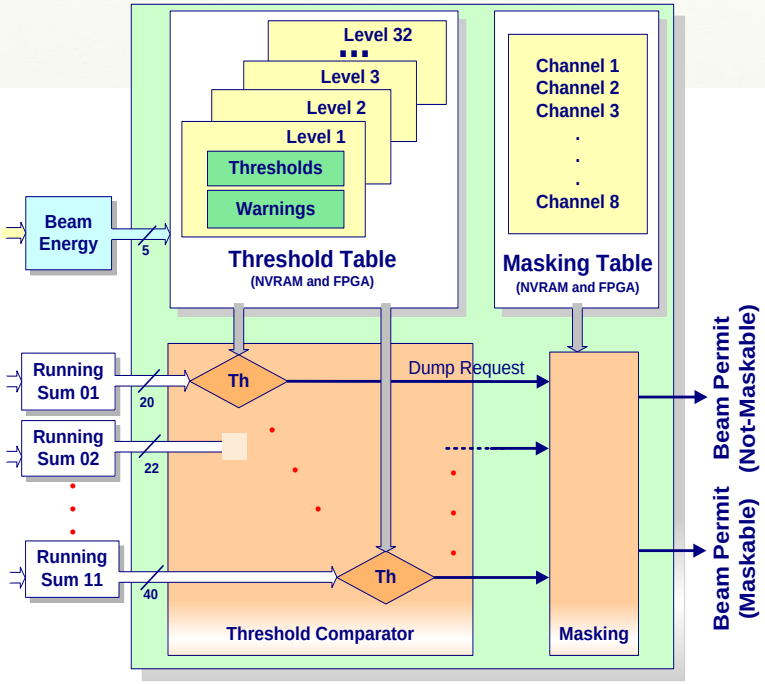
Threshold Comparator (TC)

- Compares continuously the calculated sums with their threshold limits.
- Chooses from energy and topology dependent threshold levels.

Channel Masking

- Inhibits unconnected channels and
- Discriminates channels into “Maskable” and “UnMaskable”.

Threshold Comparator & Masking



Threshold Table

- Threshold depends on energy and on integration.
- Unique thresholds for each detector.
- Read at power-on from an external NV-RAM.
- Update can be requested from the Combiner.
- Space required: 32 KB

Masking Table

- Unique masking for each detector.
- Read at power-on from the external NV-RAM.
- Masking is allowed only when safe beam.

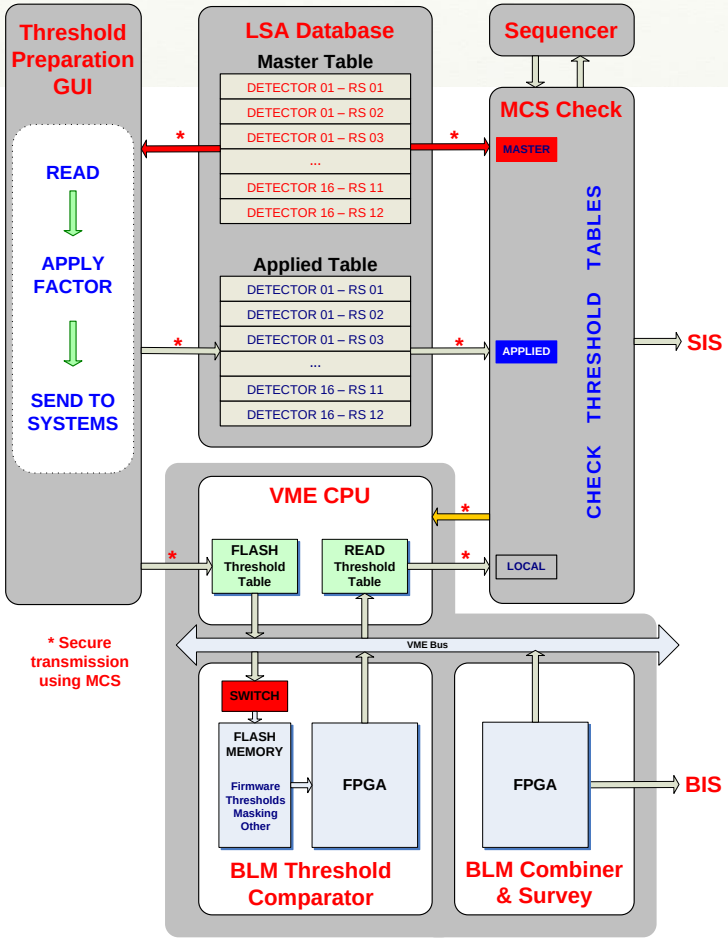
Table 1: Memory Utilisation by the Threshold Table

Width (Bits)	Detectors	Energy Levels	Running Sums	Values	Total (Bits)
32	16	32	8	4,096	131,072
64	16	32	4	2,048	131,072
		Total	12	6,144	262,144

Table 2: Information included in the Masking Table

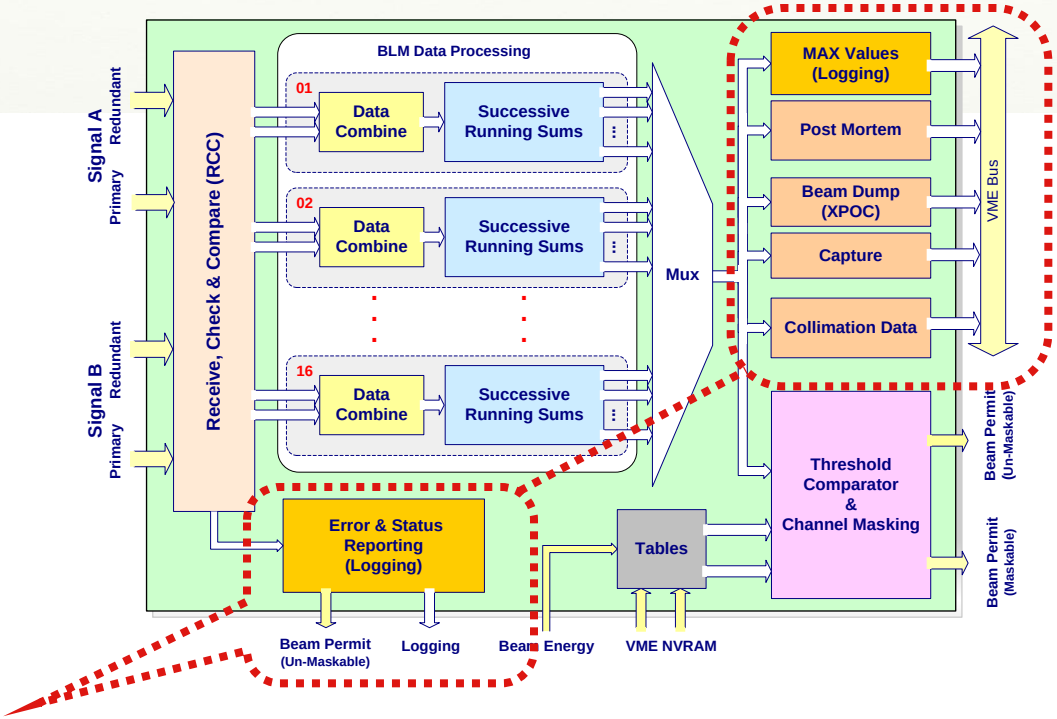
Detector	Connected	Maskable
1	No	Yes
2	No	Yes
3	Yes	No
...	...	...
15	Yes	No
16	Yes	Yes

Settings & Thresholds Management



- **Threshold GUI**
  - Reads the "master" table
  - Applies a factor (<1)
  - Saves new table to DB
  - Sends new table to CPU
- **CPU flashes table if allowed**
  - on-board switch
- Thresholds are loaded
  - at boot
  - on-demand
- **Combiner initiated test** allows CPU to read 'current' table.
- **MCS Check** receives all tables
  - Compares tables
  - Notifies SIS (if needed)
  - Replies to CPU/Combiner

Data Processing Overview



Preparation & Storage of data for external systems

- Produces an error and status report for the whole system.
- Calculates the max beam loss values for each channel.
- Keeps long buffers of acquired data.
- Keeps various buffers of integrated losses.

Steps taken for a Failsafe System

Error-free Communication

The steps taken to ensure a reliable communication link:

- Double (redundant) optical link
- CRC-32 error check algorithm
  - All single-bit errors.
  - All double-bit errors.
  - Any odd number of errors.
  - Any burst error with a length less than the length of CRC.
  - For longer bursts $Pr = 1.16415*10^{-10}$ probability of undetected error.
    - 224 bits of data plus 32 bits of CRC remainder = 256 bits
- 8b/10b encoding
  - Clock data recovery (CDR) - guarantees transition density.
  - DC-balanced serial stream - ones and zeros are equal/DC is zero.
  - Error detection – four times more characters.
  - Special characters used for control – sync, frame.
    - 256 bits of data are encoded in 320 bits = 64 extra bits

Avoiding Human Errors

To avoid misplacement of
- electronic cards or
- threshold and masking tables

- Tunnel Card ID
  - Unique number embedded in the FPGA (16bit)
  - Included in every transmitted frame
  - Compared with the one stored in the LSA DB
- Surface Card Serial number
  - Unique number embedded in a IC (64bit)
  - Compared with the one stored in the LSA DB

System Failures

To avoid loss of data

- Frame ID
  - Surface FPGA checks for missing frames
  - Incrementing number included at every transmission
- Optical link is always active
  - 8b/10b encoding sends "commas" when no data
  - Disconnection is detected in max 25ns

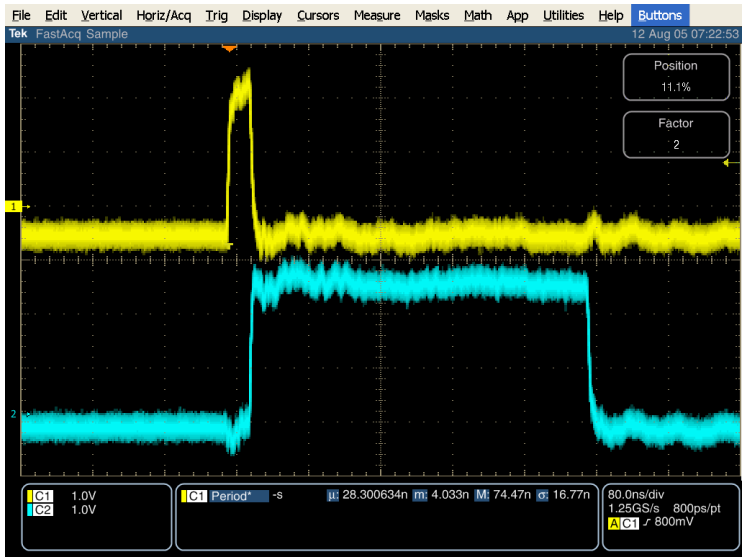
To ensure recognition of system failures and beam dump requests

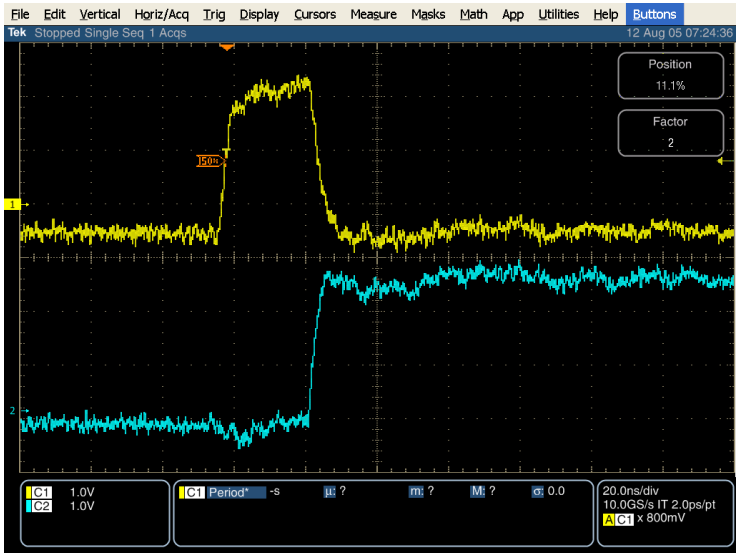
- FPGA Outputs (Beam Dump signals) as frequency
  - At a dump request, reset, or failure the transmitted frequency will be altered
- Beam Permit lines are daisy-chained between cards
  - Custom VME backplane
  - Dummy cards on empty slots to close circuit

Verification techniques used

Verification using the oscilloscope

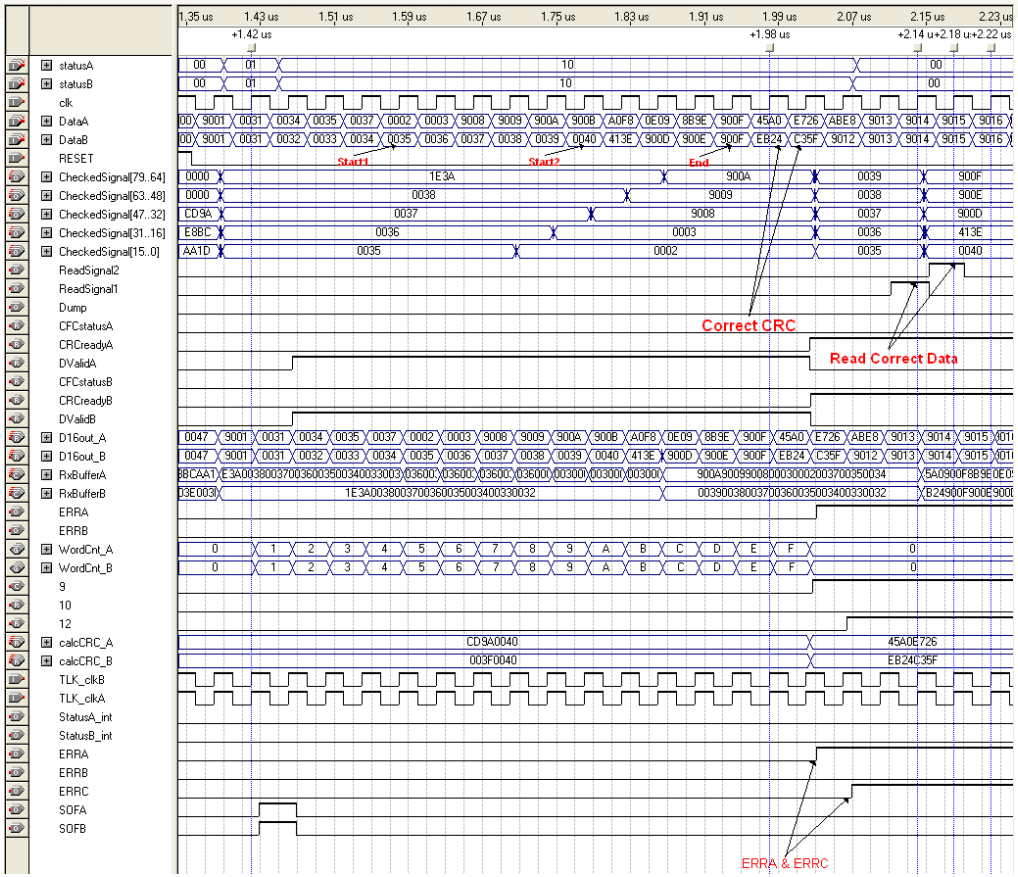
Example: Data reception control signals from the mezzanine.





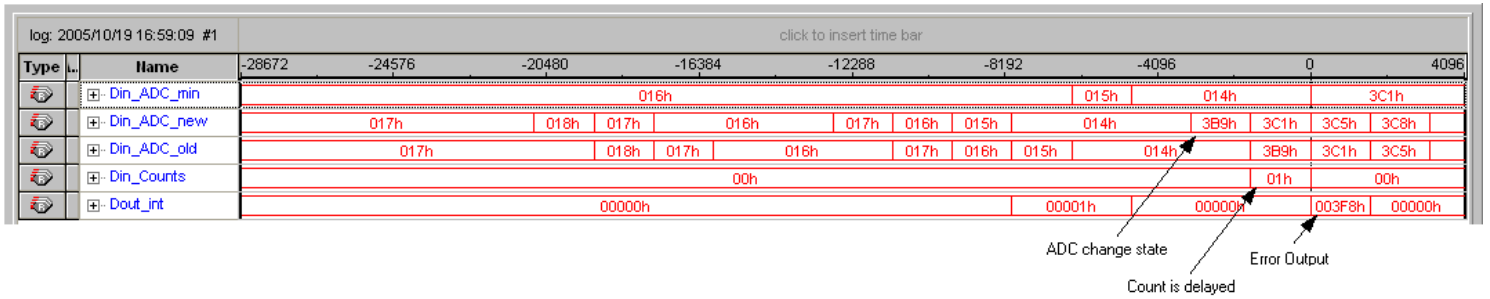
Verification using simulation

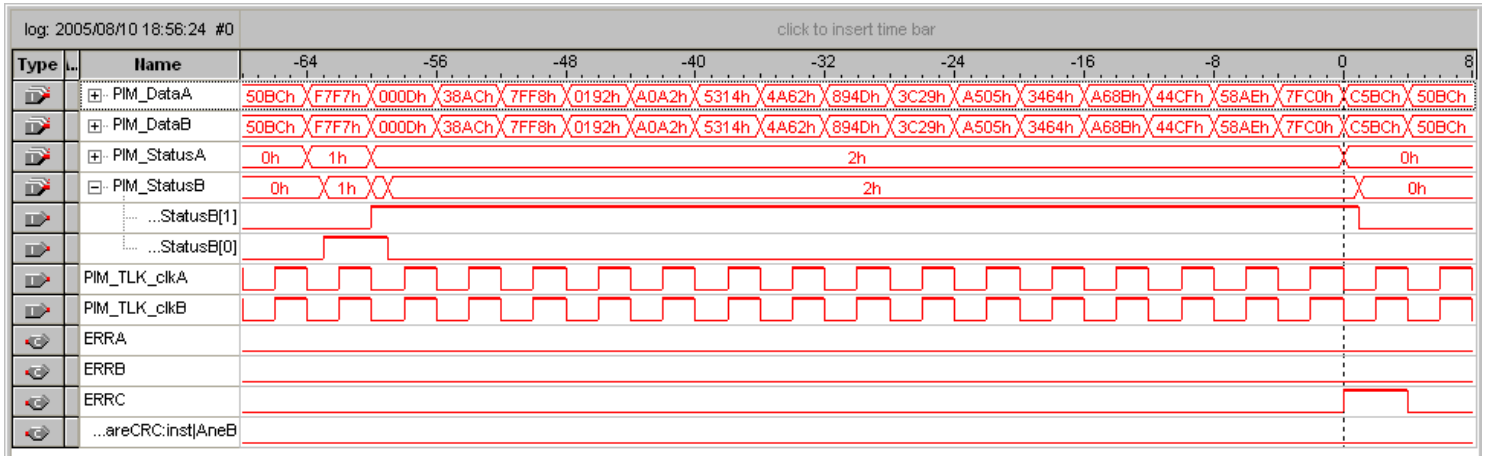
Example: Output of the RCC block. (Post P&R)



Verification using the SignalTap™

Example: Data acquisition triggered on transmission errors





Verification using custom firmware

Some examples:

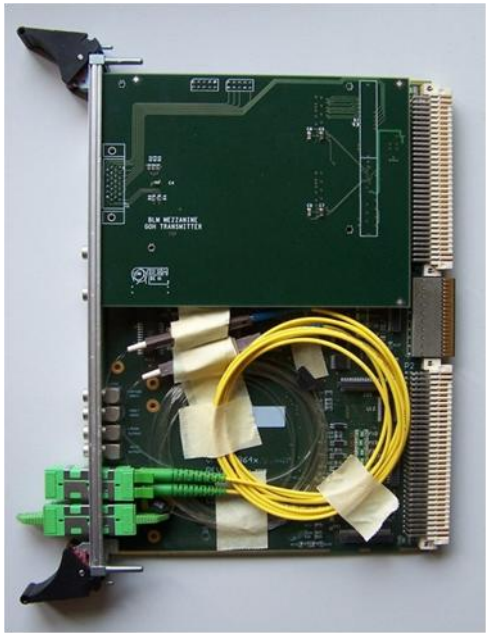
- Self-triggering mechanisms
  - Detecting differences in channels
  - Freezing of buffers on defined input levels
- Sending dummy data to check data paths
  - Input to threshold comparator
  - VME to databases

Verification Using ModelSim

- Functional simulation of critical parts
- "Black box" design methodology
  - Based only on specification
- Stimulus read from file
- Automatic checking of outputs
- Comparison of versions
  - Regression testing
  - Detection of new bugs

Verification using Emulator Module (I)

- In situ test of the TC in VME crate by emulation of output signals of CFC
  - New mezzanine for DAB64x card
  - Two standard GOH transmitters
  - Custom FPGA firmware



Verification using Emulator Module (II)

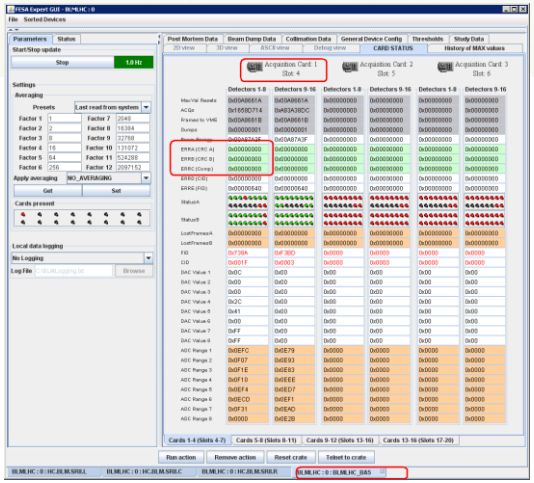
- Arbitrary Tx data
  - Comparison of different TC firmware versions
  - Playback of LHC capture data for analysis
- Tx errors
  - CRC, CID, FID
- Wrong configuration
- Errors in physical layer

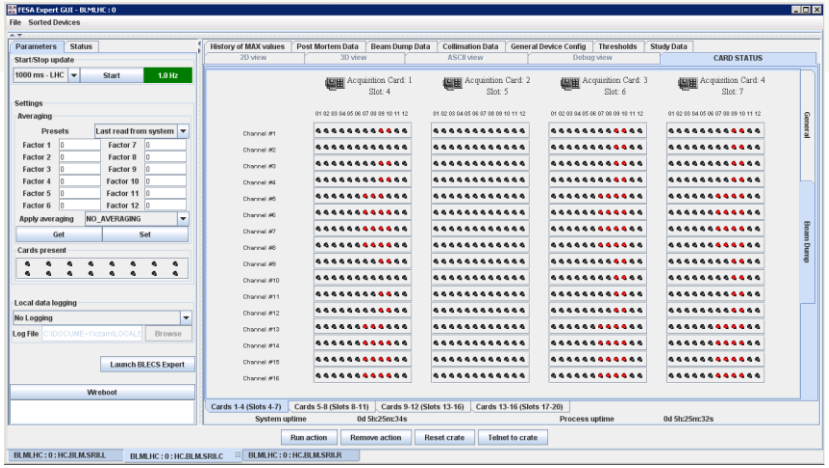
- Manual testing procedure
- Results read out in Expert application

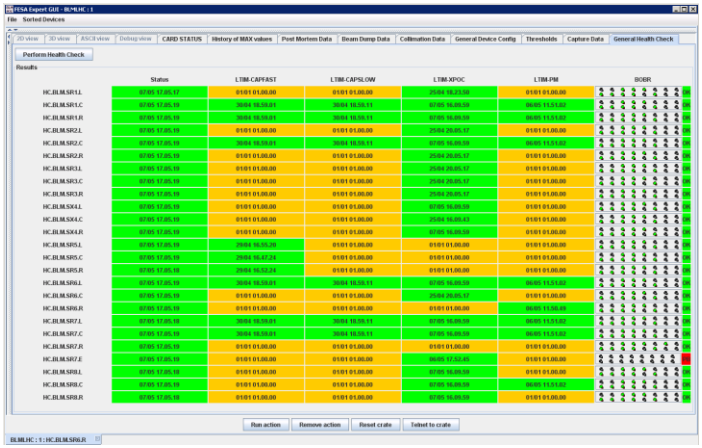
Verification using custom programs

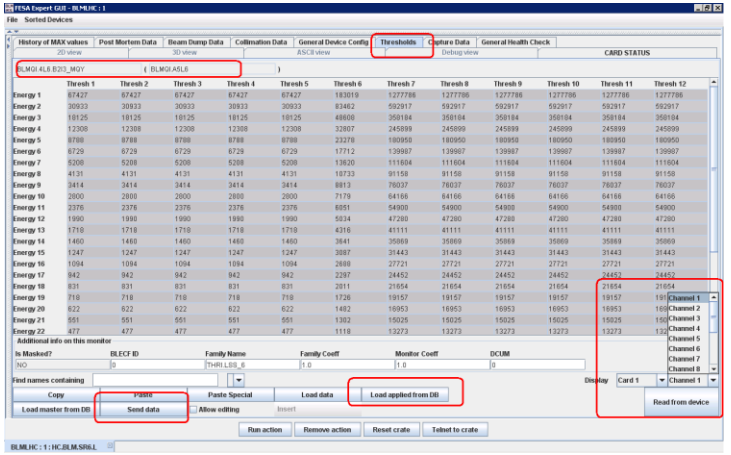
- Exhaustive verification of the behavior of the Threshold Comparator block
  - Check all permutations and their ability to trigger a beam dump request
  - Flash modified threshold table targeting one table field at each iteration.
    - 16 cards/crate
    - 16 detectors/TC card
    - 12 integration windows/detector
    - 32 beam energy levels
    - 98’304 testcases/crate
- VME readout check
  - The same testcase repeated 500’000 times

Verification using the Expert GUI (1)

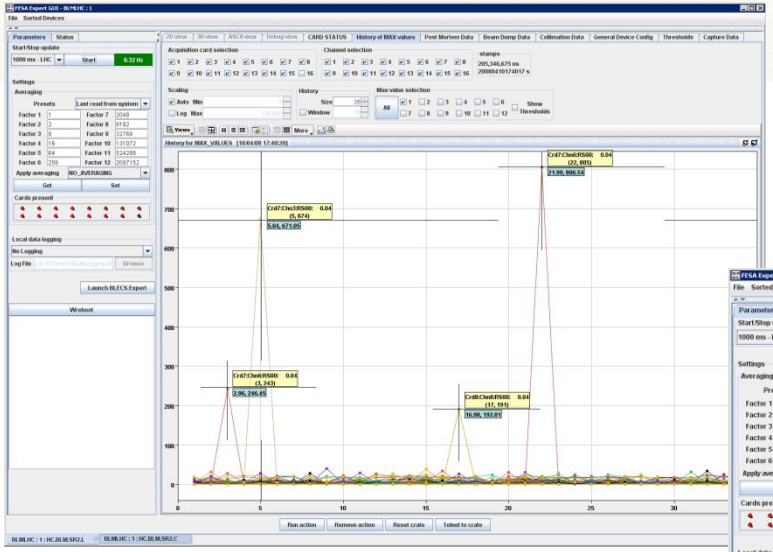


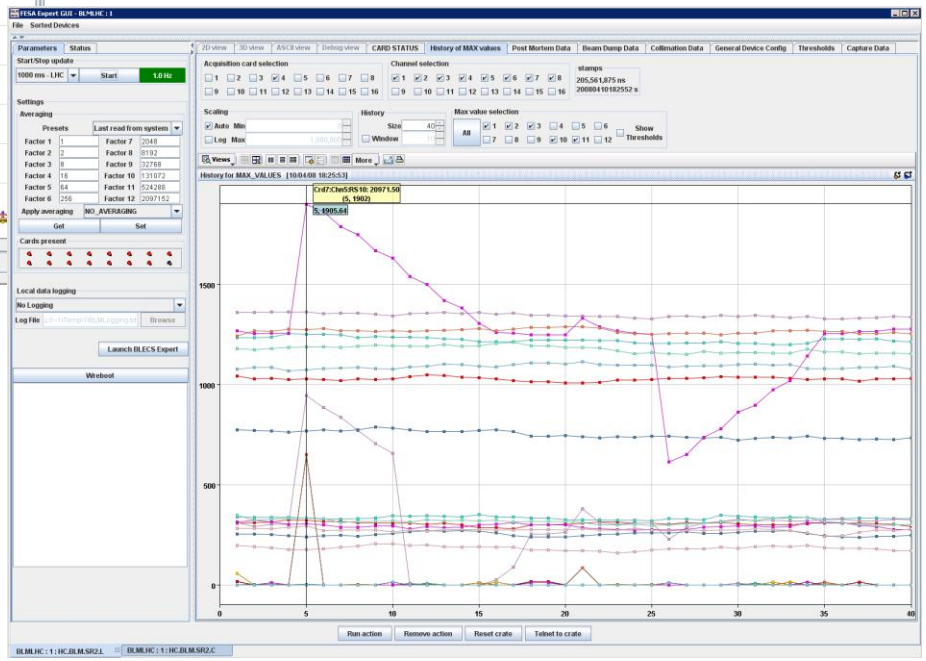






Verification using the Expert GUI (2)





Verification using other options..

- VME2USB module (CAEN)
  - Second VME master
- Scripts and programs
  - Written in Bash, C, Java – compiled in LynxOS
  - Direct access to memory addresses
- Many test systems (+ users)
  - DESY, SPS (x2), PS, CMS, LAB (x2)

Procedure for new firmware release

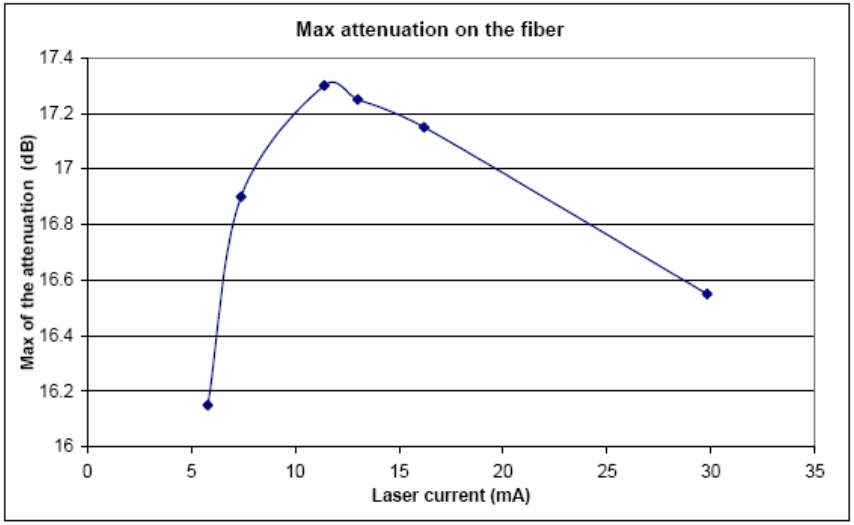
- A few hours of manual testing
  - Carry out simulation with testbenches all parts affected
- Perform hardware-based test
  - CRC errors
  - CID errors
  - FID errors
  - Lost frames
- 24 hours of automatic testing
  - Execute the software-based “Exhaustive testing”
  - All tests need to pass!
- Inspection of the code changes by the verification engineer
  - Independent review

Production and Installation

Laser Settings / Max attenuation

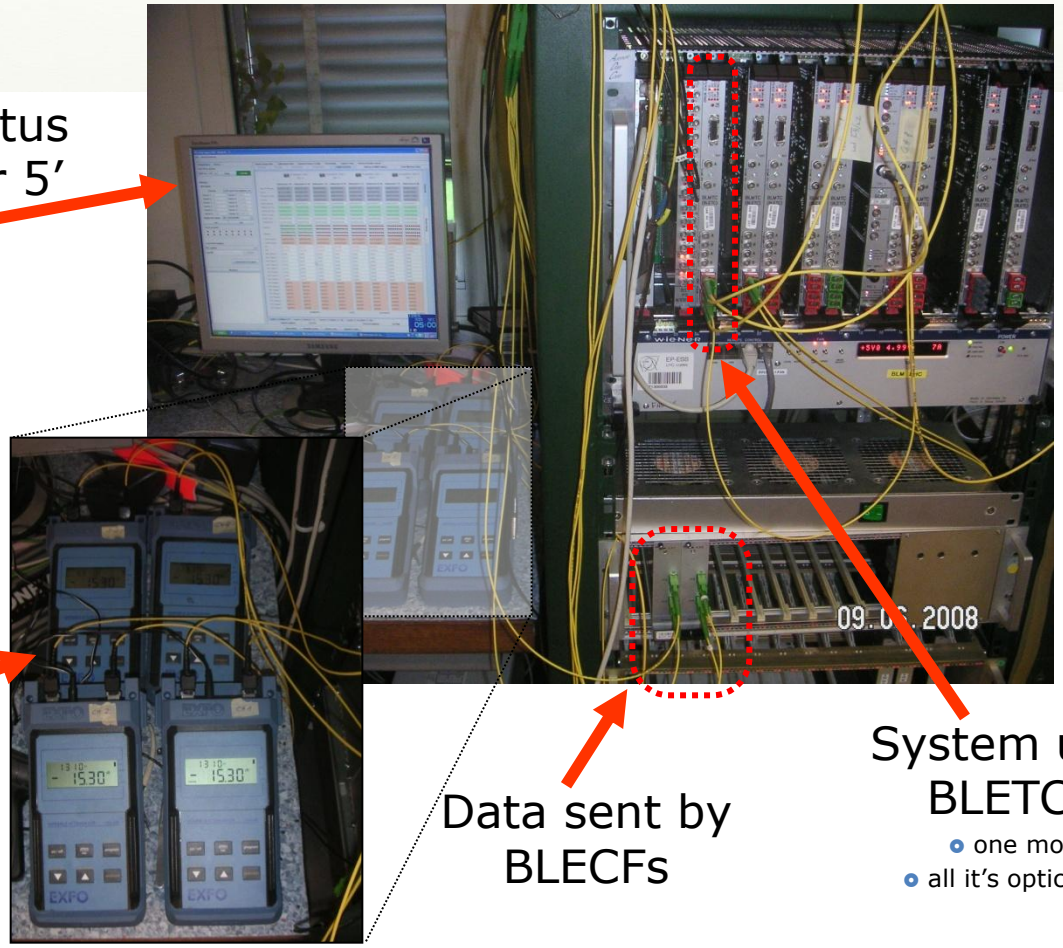
Measurements done (by J. Emery) to identify the optimal settings for the laser.

Laser Setting	Laser Current (mA)	Max Attenuation (dB)
12	5.8	16.15
16	7.4	16.9
26	11.4	17.3
30	13	17.25
38	16.2	17.15
72	29.8	16.55



Production testing

Record the status of the links for 5’ using the expertGUI



Attenuate the optical links by 15.3 dB

Data sent by BLECFs

System under test: BLETC module

- one module at a time
- all it’s optical links in parallel

Data Output

Table: BLM Noise and Offset

			minimum		10pA		10pA + Full DAC		DB Filter		maximum	
Name	**Time (µs)**	**Step (Time/40)**	**BLM_bits**	**Gy/s**	**BLM_bits**	**Gy/s**	**BLM_bits**	**Gy/s**	**BLM_bits**	**Gy/s**	**BLM_bits**	**Gy/s**
RS01	**40**	1	1	9.05E-05	2	1.81E-04	49	4.43E-03	60	5.43E-03	262144	2.37E+01
RS02	**80**	2	1	4.53E-05	2	9.05E-05	49	2.22E-03	65	2.96E-03	524288	2.37E+01
RS03	**320**	8	1	1.13E-05	2	2.26E-05	49	5.54E-04	78	8.80E-04	2097152	2.37E+01
RS04	**640**	16	1	5.66E-06	2	1.13E-05	49	2.77E-04	85	4.80E-04	4194304	2.37E+01
RS05	**2560**	64	1	1.41E-06	3	4.24E-06	58	8.20E-05	101	1.43E-04	16777216	2.37E+01
RS06	**10240**	256	1	3.54E-07	3	1.06E-06	71	2.51E-05	120	4.24E-05	67108864	2.37E+01
RS07	**81920**	2048	1	4.42E-08	8	3.54E-07	174	7.69E-06	156	6.88E-06	536870912	2.37E+01
RS08	**655360**	16384	1	5.52E-09	37	2.04E-07	990	5.47E-06	679	3.75E-06	4294967296	2.37E+01
RS09	**1310720**	32768	1	2.76E-09	65	1.80E-07	1947	5.38E-06	807	2.23E-06	8589934592	2.37E+01
RS10	**5242880**	131072	1	6.90E-10	261	1.80E-07	7742	5.35E-06	3048	2.10E-06	34359738368	2.37E+01
RS11	**20971520**	524288	1	1.73E-10	956	1.65E-07	30820	5.32E-06	11641	2.01E-06	137438953472	2.37E+01
RS12	**83886080**	2097152	1	4.32E-11	3891	1.68E-07	123087	5.31E-06	33627	1.45E-06	549755813888	2.37E+01

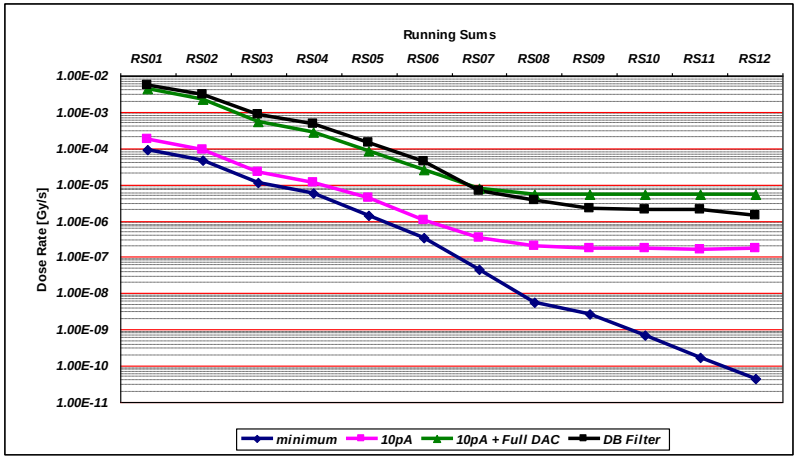
BLM Dose rate & Offset

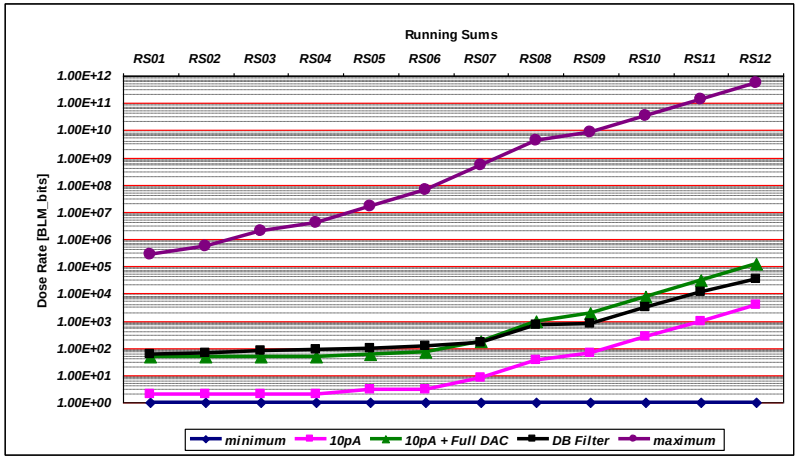
Signal present but not related to particle flux

- 10pA – Constant offset
- 0 to 255pA – Aging Compensation

Logging DB filters chosen for all integrals (RS)

- ~ 1 order higher from the 10pA
- Fixed logging interval to 1 minute





Figures: Dose rates expected in BLM_bits (left) and Gy/s (right) for each integration period

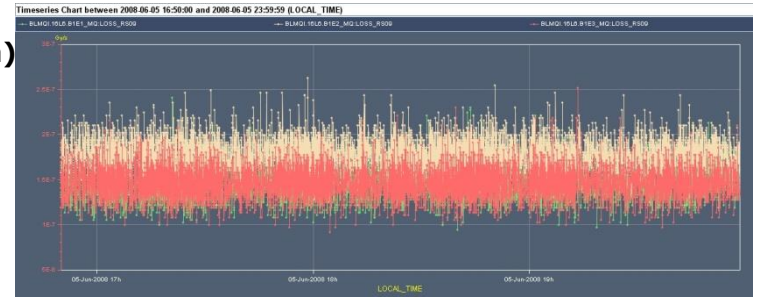
Measurement/Logging DB

Constant 10pA input of 3 ch.

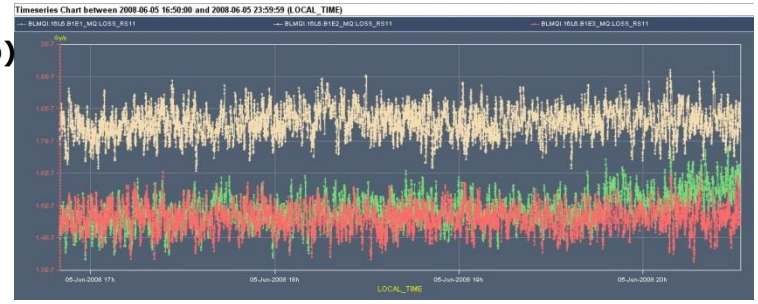
a) 1.3 sec integral

b) 84 sec integral

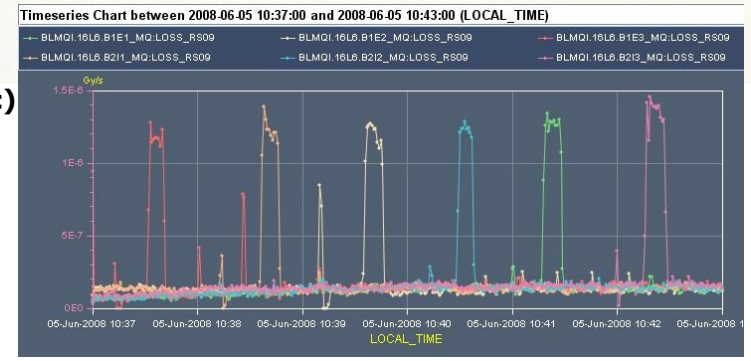
a)



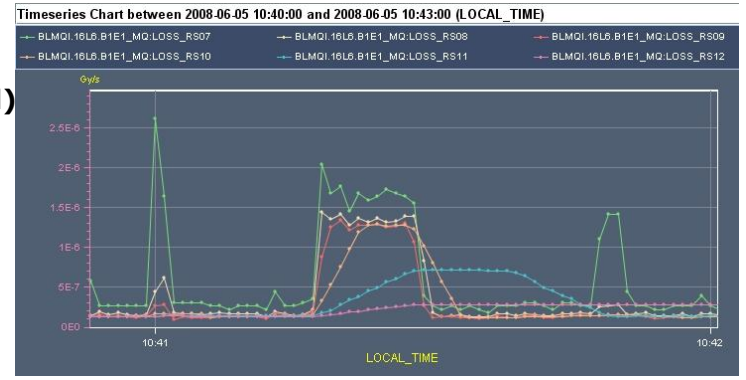
b)



c)



d)



Radiation Source Test

c) 1.3 sec integral of 6ch. – Complete magnet

d) 82 ms - 84 sec integrals of one channel

Major changes since last audit (2008)

Operational:

- Resolved instabilities in the TH table readout
- Implemented connections with Combiner for tests
- Implemented & connected detection of failures of the tunnel system to the beam dump requests
- Automatic checks to test the complete chain to BIS
- Implemented warnings to be displayed in the ALARMS server at the CCC

Verification:

- Produced test-benches for verifying (before deployment) firmware/software revisions
- Deployment of Vertical Slice Test system.