The LHC beam loss monitoring system's data acquisition card

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Abstract

The beam loss monitoring (BLM) system [1] of the LHC is one of the most critical elements for the protection of the LHC. It must prevent the super conducting magnets from quenches and the machine components from damages, caused by beam losses. Ionization chambers and secondary emission based beam loss detectors are used on several locations around the ring. The sensors are producing a signal current, which is related to the losses. This current will be measured by a tunnel electronic, which acquires, digitizes and transmits the data via an optical link to the surface electronic. The so called threshold comparator (TC) [2] collects, analyzes and compares the data with threshold table. It also gives a dump signal through the combiner card to the beam inter lock system (BIC).

The usage of the system, for protection and tuning of the LHC and the scale of the LHC, imposed exceptional specification of the dynamic range and radiation tolerance. The input current dynamic range should allow measurements between 10pA and 1mA and it should also be protected to very high pulse of 1.5kV and its corresponding current. To cover this range, a current to frequency converter (CFC) is used in the tunnel card, which produces an output frequency of 0.05Hz at 10pA, and 5MHz at 1mA. In addition to the output frequency, the integrator output voltage is measured with a 12bit ADC to improve the resolution.

The location of the CFC card next to the detector imposes the placement of the card in the LHC tunnel, exposing the card to radiation. The radiation tolerance was defined by assuming a 20 year operation period corresponding to 400Gy. A mixture of radiation tolerant Asics from the microelectronic group at CERN, and standard component was chosen to cope with these requirements.

I. INTRODUCTION

There will be several systems installed for the protection of the LHC, but one of the most critical is the beam loss monitoring system. The system consists of around 4000 detectors, ionisation chambers and secondary emission monitors. A total of 650 data acquisition cards will be installed in the LHC arcs and side tunnels next to the straight sections of the ring. In the arc, the CFC card will be placed in small racks located below each quadrupole magnet. Due to the high radiation in the straight sections, the CFC cards are concentrated at two locations at each LHC interaction region. The CFC data will be transmitted via an optical link to the surface electronics. It consist of 340 TCs with optical receiver mezzanine, situated in 25 VME creates, distributed in the surface buildings around the LHC. The VME creates will also host the PowerPC, a combiner card, and two timing-cards. The PowerPC collects the running sum values of the TC, and sends it to a database. The combiner card has a hardwired link to the BIC, which transmits the beam dump signal to kicker magnets.

A. *Specification of the data acquisition card*

The exposition to radiation leads to the requirement of a tolerance of a maximum of 400Gy integrated dose for 20 years LHC life-time. For the system and the performed tests a maximum value of 500Gy was chosen to ensure a safety margin.

The employment of the system for the LHC protection requires a high reliability of the CFC card. To achieve a reliability level SIL3 [3] (10^{-7} to 10^{-8} failure/h) of the system, several different test modes, status information, protection circuits and a redundant data transmission are implemented. For the verification, different tests have been performed, like irradiation, temperature and burn-in test. An additional test in magnetic field was included.

Table 1: Specifications requirements

Current measuring range	2.5pA	1mA
Error down to 10pA	-50%	+100%
Error down to 1nA	-25%	+25%
Maximal input current	561mA	
Input voltage peak	1500V @ 100us	
Radiation	500Gy in 20yr	
Digital supply	+ 2.5V	
Analogue supply	+/- 5V	
HV monitor input	0V	+5V

B. *The data acquisition card*

To measure a current over this high dynamic range, a CFC (figure 1) has been chosen, which is based on the balanced charge integrating techniques. In comparison with other switching techniques, the CFC advantage is given by no dead times and no losses of charges [4]. Since the output frequency depends on the input current (small current correspond to a very low frequency), an addition analogue to digital converter (ADC) is added to measure the output voltage of the integrator and to calculate partial counts in the TC. This measure decreases the response time and increases the dynamic range. The counting time window of the system is 40µs. The data including the counted CFC pulses and the integrator output voltage are transmitted every 40µs to the TC. The requirements of a small leakage current and a fast charge/discharge led to the choice of the OPA637 as the

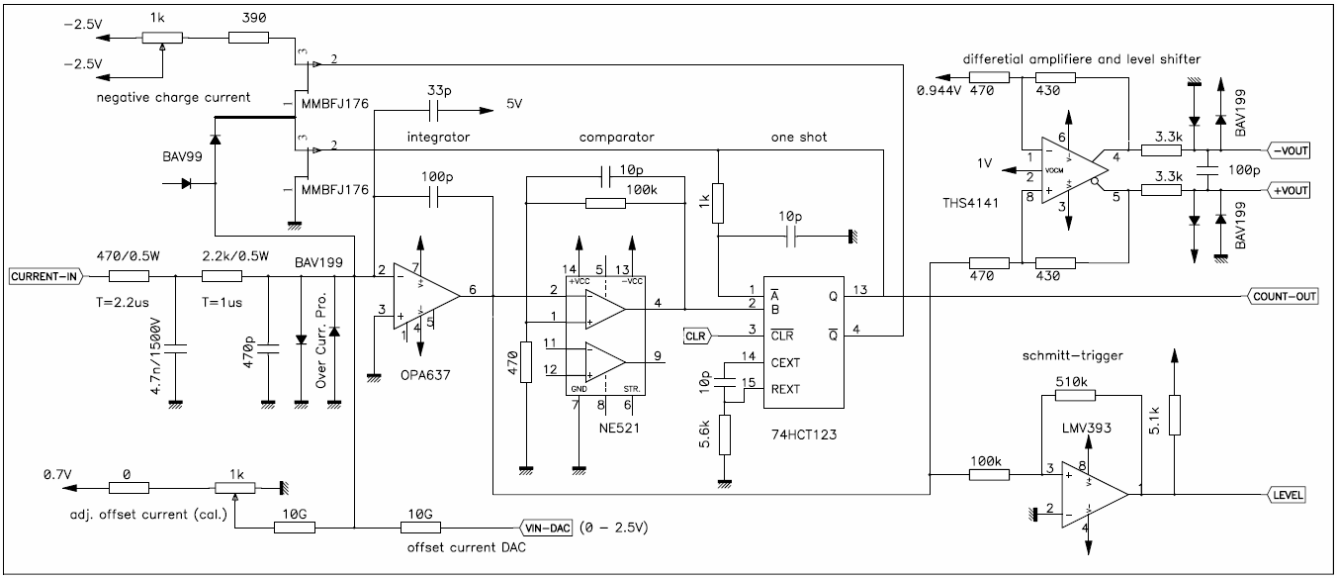

Figure 2: Circuit diagram of the CFC for one current input

operational amplifier in the integration circuit. The radiation tests showed that the chosen amplifier OPA637 did resist the irradiation. But the input offset current increased from typically 2pA to -50pA to -80pA with an integrated dose of 500Gy. Conversely, the amplifier maintained its functionality even with a dose of up to 1500Gy. The JFET J176 used for the switch discharge circuit was adding a positive leakage current of +150pA under radiation, but this current could be removed with the insertion of a diode BAV99 into the current path. The irradiation of the comparator NE521 and the one shot 74HCT123 produced an error of less than 0.5%. Standard ADCs have been irradiated and failed already with a small dose. The radiation tolerant ADC AD41240 [5] produced by MIC showed no decrease in functionality under radiation. The AD41240 is used together with the deferential line-driver CRT933 (from MIC), which is needed as level shifter between the ADC and FPGA. To connect differential analogue input of the ADC to the single ended output of the integrator, a THS4141 is used.

For the data conditioning, a FPGA has been chosen. To achieve a higher radiation tolerance, an antifuse type is used instead of a flash based FPGA. Actel provides a standard type A54SX72A and a radiation hard type RT54SX72A, but the RT54SX72A are far too expensive for such a system, which requires 750 pieces. The FPGA did withstand a total dose of 480Gy to 790Gy.

For the data transmission, an optical link is chosen instead of a copper based one, because the distance between the transmitter and the receiver, can be up to 2km. Several standard systems from the market have been tested but all of them failed while irradiation. Here again, the MIC provided the solution. For the CMS experiment, they produced a gigabit optical link (GOL) [6], which is utilised in the gigabit optical hybrid (GOH). For the BLM system a special GOH with an E2000-APC optical connector was produced.

To survey the specified function of the CFC card several status bits are constantly checked and transmitted together with the data frame. All the voltage supplies, including the external high voltage, are monitored with a comparator circuit using a LMV393. Two independent monitoring systems are used for the CFC. A Schmitt trigger circuit, using a LMV393, monitors the integrator output level and sends a flag if it exceeds 2.4V. The second survey technique for the CFC introduces a constant input current of 10pA, which corresponds to one count every 20s. The counts are monitored, and in case of 120s without a count, an error flag is generated and transmitted.

Due to increasing negative leakage current of the OPA637 with the radiation dose, an active compensation has been added to ensure a constant 10pA input current. The compensation current is produced using an 8 bit digital to analogue converter AD5346 with a 10G resistor connected to the input of the CFC.

The complete CFC card has been irradiated up to a total dose of 500Gy. To detect SEU, the redundant CRCs had been verified and compared at the receiver part. No SEU was detected up to $1x10^{12}$ p/cm^2.

C. Functional description of the FPGA

The functionality is shown in figure 2. All input signals are registered with 40MHz, due to some malfunctions of finite state machines (FSM) and other logical parts of the FPGA. For example, the counter input, which was connected directly to the input buffer, produced random values at the counter output with a well defined input frequency. Adding a register solved the malfunctioning of the input buffers. Due to the limited FPGA size (an overall of 6036 cells), only the CFC counters, which are most critical, have been tripled. The ADC values are insignificant for the threshold value comparisons. Tripling will decrease the probability of a fault beam dump provoked by a SEU. The system reset is also tripled but all the remaining logic is not tripled. The two GOH interfaces are redundant blocks, which are connected to the GOHs. The 40MHz system clock is connected to the hardwired HCLK and to the 4 quadrant QCLK. This opens the possibility to distribute the 40MHz internally in accordance to the importance of the blocks. The HCLK is used for the GOH interfaces, because of speed considerations, and for the counter block, because it is less sensitive to SEU.

The entire clock, timing, enable and other control signals, which are used in the FPGA, are produced in the clock divider. This includes several counters to produce enable signals of 200ns, 40µs and 1s. With these counters all control signals are produced. There is also a 16 bit counter that produces the frame identity number (FID) which increments every sent frame and is checked at the receiver part.

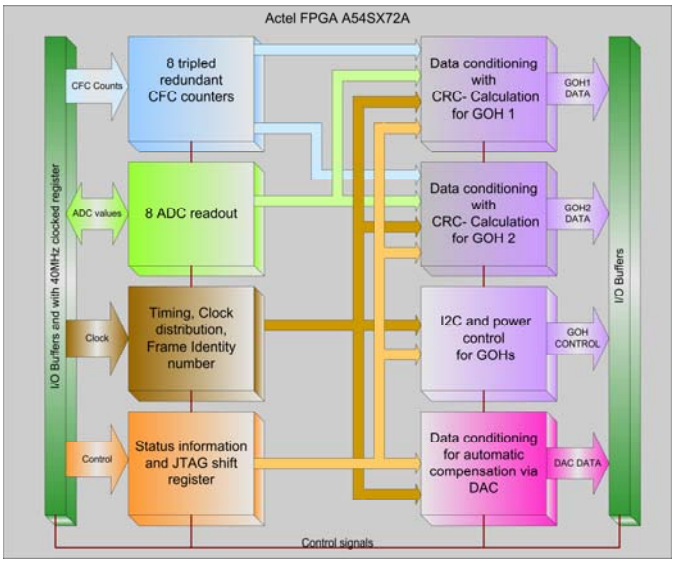

Figure 2: Block diagram for FPGA

In the status block, all the status bits coming from the pins and produced internally are registered every 40µs. A shift register is introduced to read out the card identity number (CID), which is stored as the silicon signature of the FPGA. The signature is programmed into each single chip and readout via the JTAG. This CID is read and checked for every frame in the TC.

As there are 8 similar current inputs and CFCs, the block shown in figure 3 exists 8 times. The count signals coming from the one shot are physically connected to 3 I/O pins and all the logic is tripled inside this block.

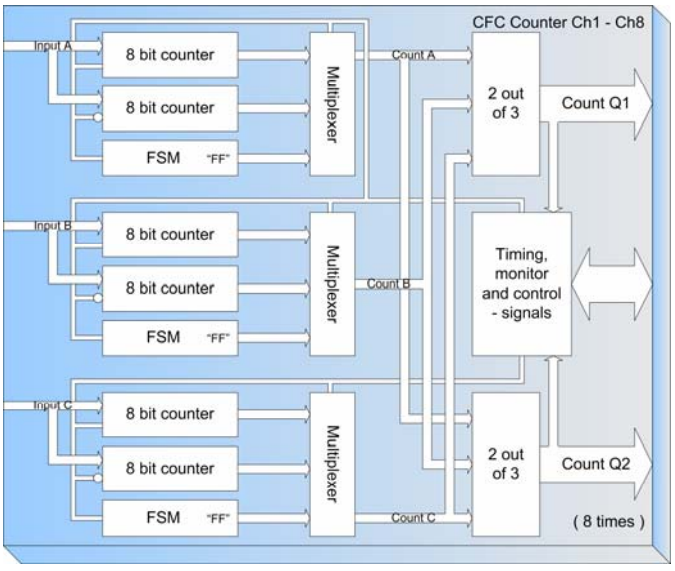

Figure 3: Block diagram for CFC counter (1 channel)

This counter signals are connected to two similar 8 bit counters. The counter used is a fast balanced counter produced by the Actel SmartGen macro builder. The enable signal is gated with a 40µs signal. One of the enable signals is inverted, therefore the counters work in chopper mode. This design has been chosen in order to have one less time critical part, as there is 40µs gap available instead of 25ns to read out the information. Since the selection in the SmartGen is poor concerning the types of counters and In and Output configurations, the addition of a FSM was necessary to ensure that in case of overflow the output would stay 255. The counter outputs are connected to a multiplexer, which switches between the two counters every 40µs, except in case of overflow when the third input is selected. This counter value is produced 3 times per CFC channel. These 3 values are sent to two 2-out-of-3 voters, each of them feeding one GOH interface.

The ADC is connected via two 12 bit data lines (figure 4), the information of two channels is multiplexed and changes with the rising or falling edge. Rising edge corresponds to ch0 and ch2; falling edge to ch1 and ch3. The sampling frequency of the ADC is 5MHz but the readout of the system is every 40µs.

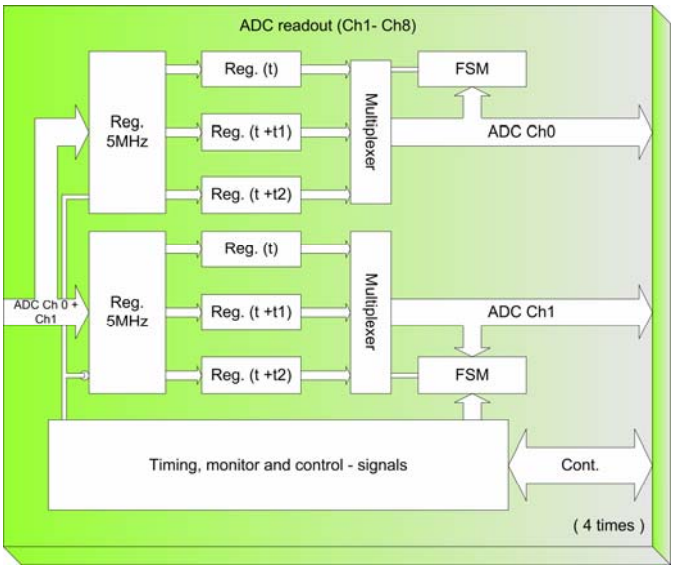

Figure 4: Block diagram for ADC readout

To separate the multiplexed ADC values the readout of the two channels is shifted by half a period of the clock frequency. A special logic has been implemented in case the CFC pulse is close to the readout of the ADC. It was observed that the CFC plus was counted in the specified 40µs window, but the ADC value was near zero instead of the maximum value. The delay between the positive edge of the CFC pulse and the integrator output causes this effect. A FSM was introduced to check if there is a count in a defined time window of 100ns, and a second FSM checks the ADC value. In case a pulse appears in this 100ns time window, the next readout value will be chosen. Due to the rise time of the integrator signal, a wrong ADC value can still appear. Therefore, a second FSM compares the value with a threshold and if necessary, it uses the 2nd ADC readout. The 3 readouts are always registered and connected to a multiplexer. The two FSMs select the correct value.

There are two redundant GOH interfaces. To increase the reliability of the data transmission, both interfaces calculate a 32 cycle redundancy check (CRC), which is transmitted together with the data. The incoming data are combined to 16 bit words and then connected to a 20 * 16 bit multiplexer.

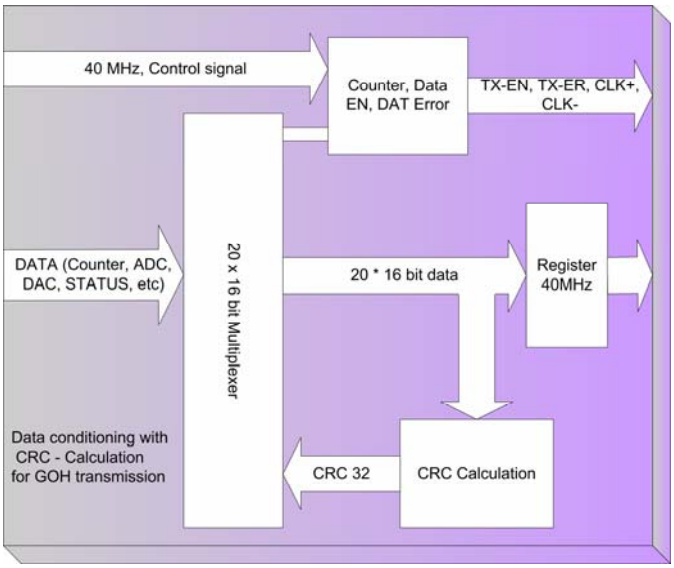

Figure 5: Block diagram GOH interface

The last two input ports are connected to the output of the CRC calculator. The output of the multiplexer is connected to the input of the CRC calculator block and to a register clocked with 40MHz, which connects to I/O buffer. A data enable and data error signal, which are produced in this block, are needed to control the GOH transmission. The transmitted data frame is shown in table 2.

Table 2: Data frame

CID (card identity number)	
STATUS 1	
STATUS 2	
Count 1	ADC 1
ADC 1	Count 2 / ADC 2
ADC 2	Count 3
ADC 3	Count 4
Count 4	ADC 4
Count 5	ADC 5
ADC 5	Count 6 / ADC 6
ADC 6	Count 7
ADC 7	Count 8
Count 8	ADC8
FID (frame identity number)	
DAC1	DAC2
DAC3	DAC4
DAC5	DAC6
DAC7	DAC8
CRC	
CRC	

The GOH includes the possibility to receive commands via the I2C. While carrying out a temperature test, some CRC errors have been observed while transmitting data. This has been improved by changing the laser diode current. The two temperature signals coming from two sensors placed on the PCB are used to switch from nominal current 11.4mA to 16.2mA, via the I^2C bus. In addition, the GOH-reset and the two GOH-flag signals allow switch off and restart the GOH. This is useful in case of the GOH malfunction.

There is an active compensation using a parallel interfaced 8 bit DAC. The DAC is controlled by the DAC interface shown in figure 6. Each counter value from both 2-out-of-3 voters are connected to the first stage, which is producing a reset signal for each arriving count. This reset pulse is used to reset the 20 second timer. If there is no reset, the following 8 bit counter will receive an enable signal and increase the counter by 1. This process is repeated till a count appears every 20s at their outputs. These 8 values are multiplexed and sent to the data input of the DAC. Together with the control signal and the address, it will set the currents on the different input channels. The same enable signal is connected to a 3 bit counter and increased also by 1. In case this value reaches 6 an error flag is set, which indicates a problem with one of the CFC input circuits. The counter will be also reset when a count will arrive.

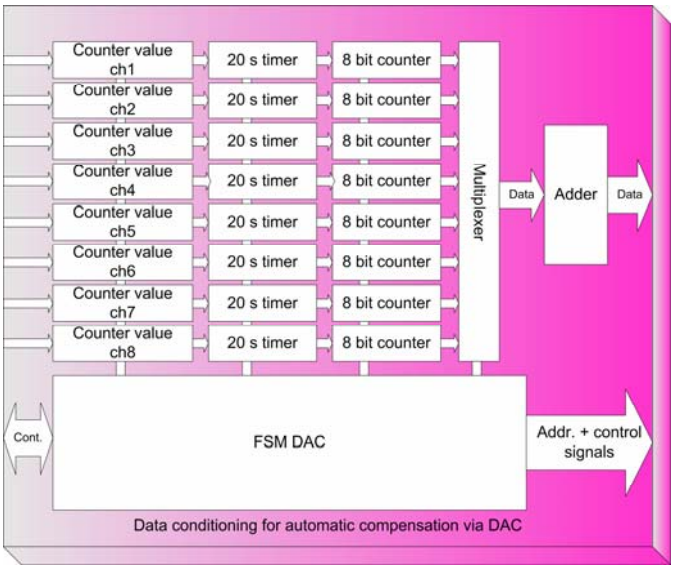

Figure 6: Block diagram DAC interface

Since the optical link is unidirectional for communication between surface and tunnel equipment (TC to CFC), the high voltage (HV) supply connection is used (bias voltage for all the ionisation chambers). All tunnel cards are connected to the HV because its level is part of the status checks. Four comparators circuits with increasing HV thresholds are connected to the FPGA. The Status_HV is used as HV monitor. The CFC_TEST, RST_DAC, GOH_RST and the LEVEL1-8 are the inputs for the FSM (figure 7). If the 3 pins are at '0', the FSM is in the default state "wait_for_cfc_test". If the CFC_TEST = '1', a counter is started. If the input is constantly '1' for 120s, then the state changes to "CFC_TEST_ON". In this state an adder in the data path of the DAC is increasing the DAC value by 100 corresponding to an input bias current increase of 100pA. The state will remain till the pin CFC_TEST changes to '0' (HV_{nom} = 1500V) and the LEVEL1-8 are at '1' (integrator voltage <1.8V). The LEVELs are included to ensure the CFCs are working correctly. For the DAC_RST and GOH_RST the same sequence needs to be followed and also 100pA is added.

The difference is an additional state which, is just before entering into the default state. As a consequence of this procedure, all the CFCs will work as defined, before the DAC is being reset or the GOH is being restarted. The active compensation is blocked as soon the FSM enters to a test or reset state.

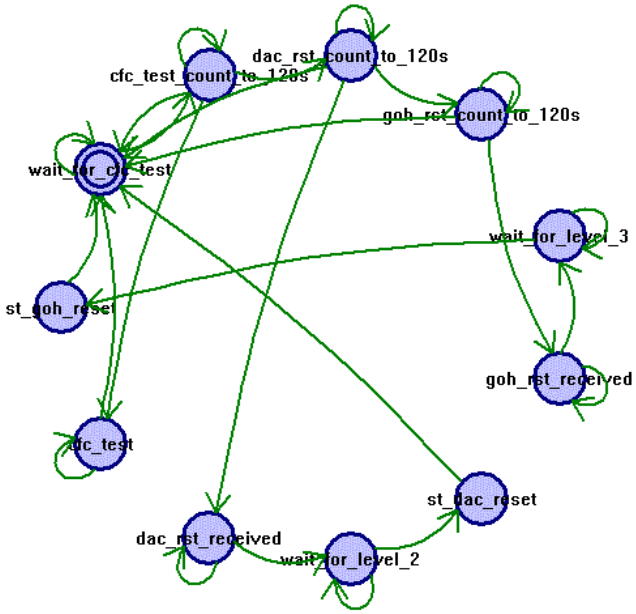

Figure 7: FSM DAC

D. Tests, test-modes and error detection

To ensure the system is working properly and to increase the reliability, several tests, test modes and error detection system have been added.

Before the installation, a calibration and an initial test are performed using a BLECFT [7] USB card, which performs an automatically generated functional test pattern. This system will also be used for additional tests after tunnel installation.

The constantly performed test using 10pA offset current, provides a count every 20s. After absence of the count for more than 120s, an error bit is activated.

For the data transmission a CRC is added, which will be verified at the TC. Due to the redundant link, even if one transmission is corrupted, data are still available.

The CID is sent and checked every transmission to ensure the used threshold table belongs to the correct chamber. Lost data transmission will be detected by the check of the FID at each data transmission.

With the CFC_TEST activated (HV ≥ 1655V for 240s), 100pA are added on the input of the CFC, to test the corresponding response of the acquisition chain. It is foreseen that this test will be carried out before each beam fill.

A HV modulation test uses capacitive current injection via chamber electrodes to detect the degradation of the complete acquisition chain. This test will be carried out before each beam fill.

There is also 32 status bit (table 3) which are sent and readout every transmission. Depending on the indicated malfunction a beam-dump is initiated.

Table 3: Status bits (E =error, W=warning, I=information)

Status 1			Status 2		
Status_P5V	E	<4.73V	CFC-ERR1	E	>120s
Status_M5V	E	>-4,72V	CFC-ERR2	E	>120s
Status_P2V	E	<2.25V	CFC-ERR3	E	>120s
Status_HV	E	≥ 3.183V	CFC-ERR4	E	>120s
TEST_CFC	I	≥ 3.633V	CFC-ERR5	E	>120s
TEST_ON	I	(≥ 1655V)	CFC-ERR6	E	>120s
RST_DAC	I	≥ 4.006V	CFC-ERR7	E	>120s
DAC_RST_R	I	(≥ 1825V)	CFC-ERR8	E	>120s
RST_GOH	I	≥ 4.390V	LEVEL 1	W	>2.4V
GOH_RST_R	I	(≥ 2000V)	LEVEL 2	W	>2.4V
TEMP 1	W	>35ºC	LEVEL 3	W	>2.4V
TEMP 2	W	>60ºC	LEVEL 4	W	>2.4V
GOH 1 ready	W	"0"	LEVEL 5	W	>2.4V
GOH 2 ready	W	"0"	LEVEL 6	W	>2.4V
DAC_155	W	>155	LEVEL 7	W	>2.4V
DAC_OVER	W	255	LEVEL 8	W	>2.4V

E. Conclusion

An acquisition system to measure current in the range of 2.5pA to 1mA has been constructed and tested. An error smaller than the +96% down to 10pA and +6.5% down to 1nA has been measured and can still be improved by a more accurate calibration. A radiation tolerance of 500Gy has been achieved for all components except two components. The one shot 74HCT123 showed some malfunction at 340Gy but it recovered after stopping the irradiation. The antifuse FPGA form Actel did withstand radiation between 480Gy to 790Gy, no SEU was detected up to $1x10^{12}$ p/cm^2. Several protection and supervision circuits are build in and were tested successfully. The optical link is radiation tolerant due to its design and in a test setup installed in HERA no CRC occurred for several months. The system passed a temperature test (0 to 70°C) which caused some CRC errors while data transmission. The complete system was also tested in a magnetic field up to 1000Gauss with a small offset current change.

II. References

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