Audit of the BLM LHC system

The Beam Loss Combiner and Survey card (BLECS)

Jonathan Emery
8 November 2010

Outline

- BLECS in the BLM system
- BLECS overview
- Beam permit
- Beam energy
- BLM checks
- Supplies monitoring

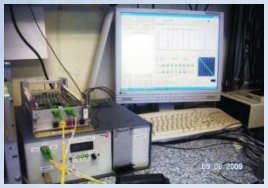
Combiner card inside the LHC BLM system

Beam Loss Monitors (4000)

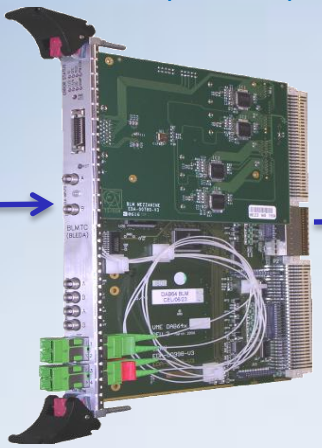
around the LHC ring

Tunnel Cards (700)

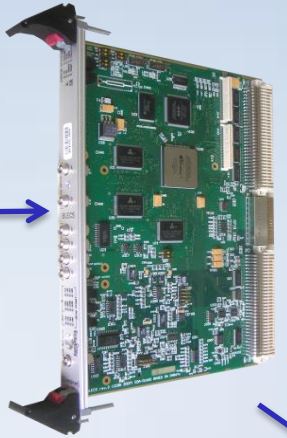
Tunnel Card test benches (5)



Threshold Comparators (350)

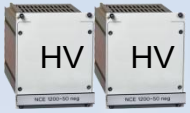


Combiner and Survey (25)

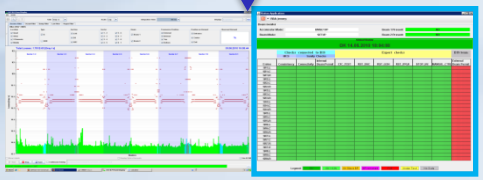


Beam Energy Receivers (8)
[CISV]
Hardware:
BE-CO-HT (P. Alvarez)
Responsible:
TE-MPE-MI (B. Puccio)
Energy measurements:
TE-ABT (N. Voumard)

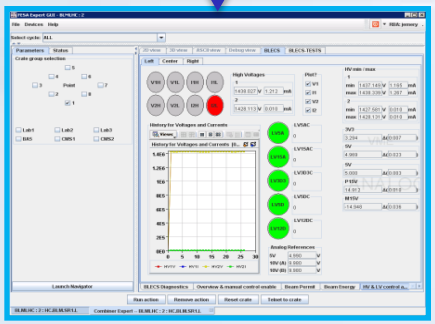
Interlock Interfaces (16)
[CIBUS] TE-MPE-MI
(B. Puccio, B. Todd)



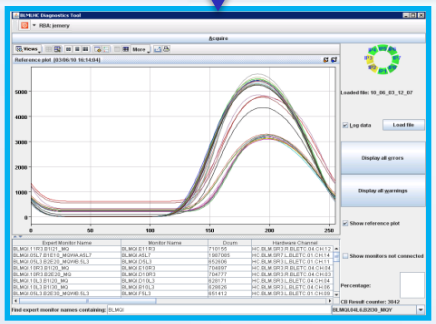
BLM HV supplies



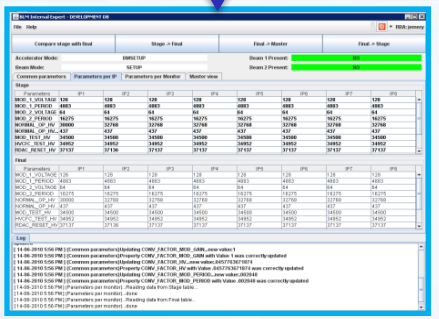
Operational applications (2)
(BE-OP)



Expert applications (2)
(BE-BI-SW)

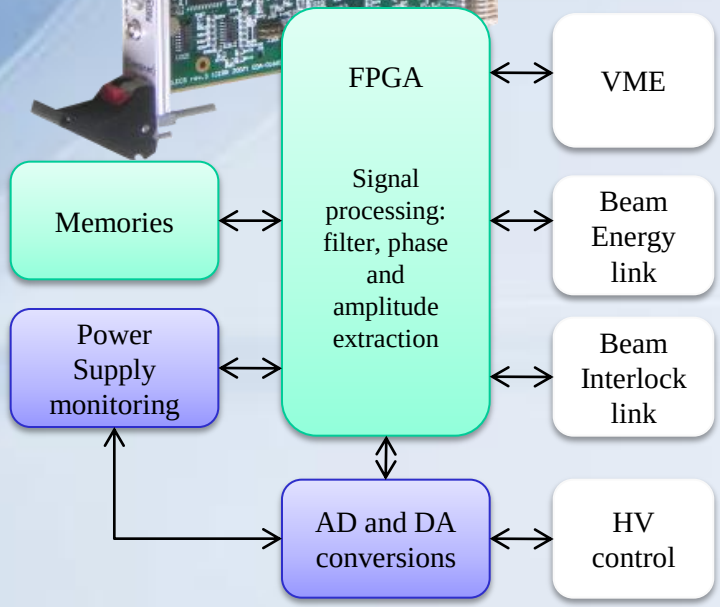


Diagnostics application,
phase and amplitude
for the connectivity check



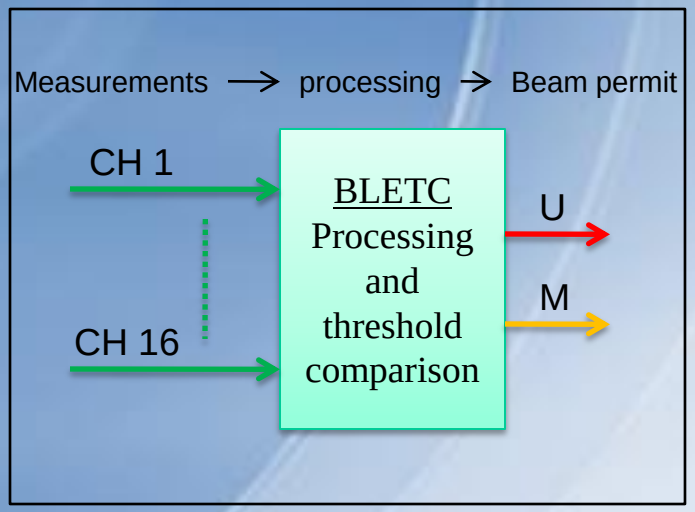
Settings applications (2)
(BE-BI-SW)

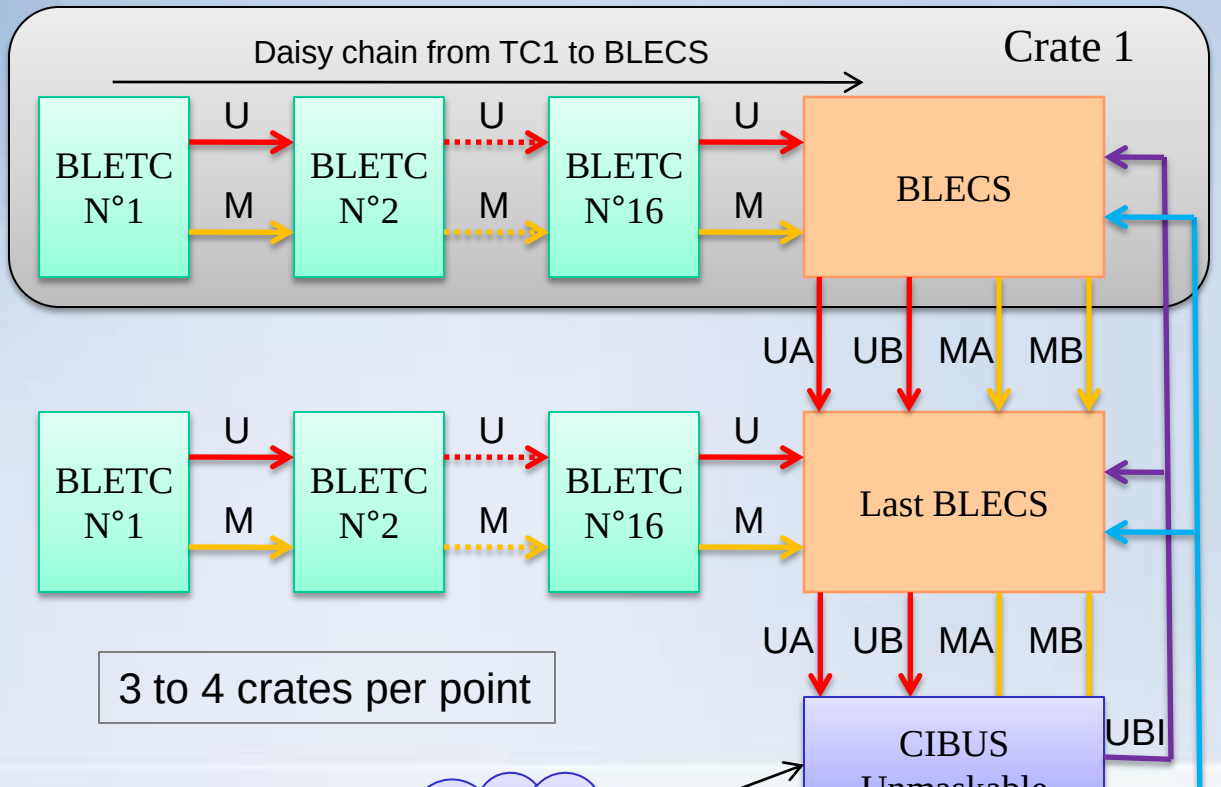
LHC BLM Combiner and Survey Card

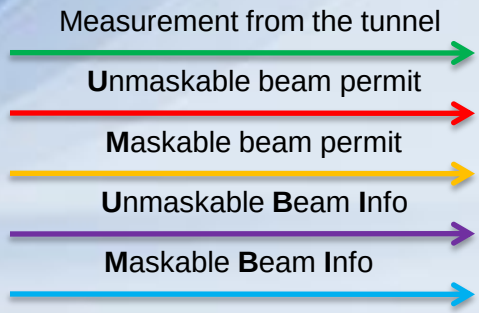


- Based on DAB card
  => VME 64x
  => Stratix 40k
  => SRAM memory
  => One site code update
  => Specific BI signals on P0
- Beam permit
  Daisy chain between crates and link to interlock
- Beam energy reception and broadcast
- Automatic checks and decisions
- Control of the BLM supplies
  Interface to high voltage power supplies
  Set and monitoring from the FPGA
- Monitoring VME PS
  for specific behavior (ripples)
- Crate interconnections for
  automatic check of the system

Beam Permit (BP) signals combination, Beam Info (BI) and link to the Beam Interlock System (BIS)

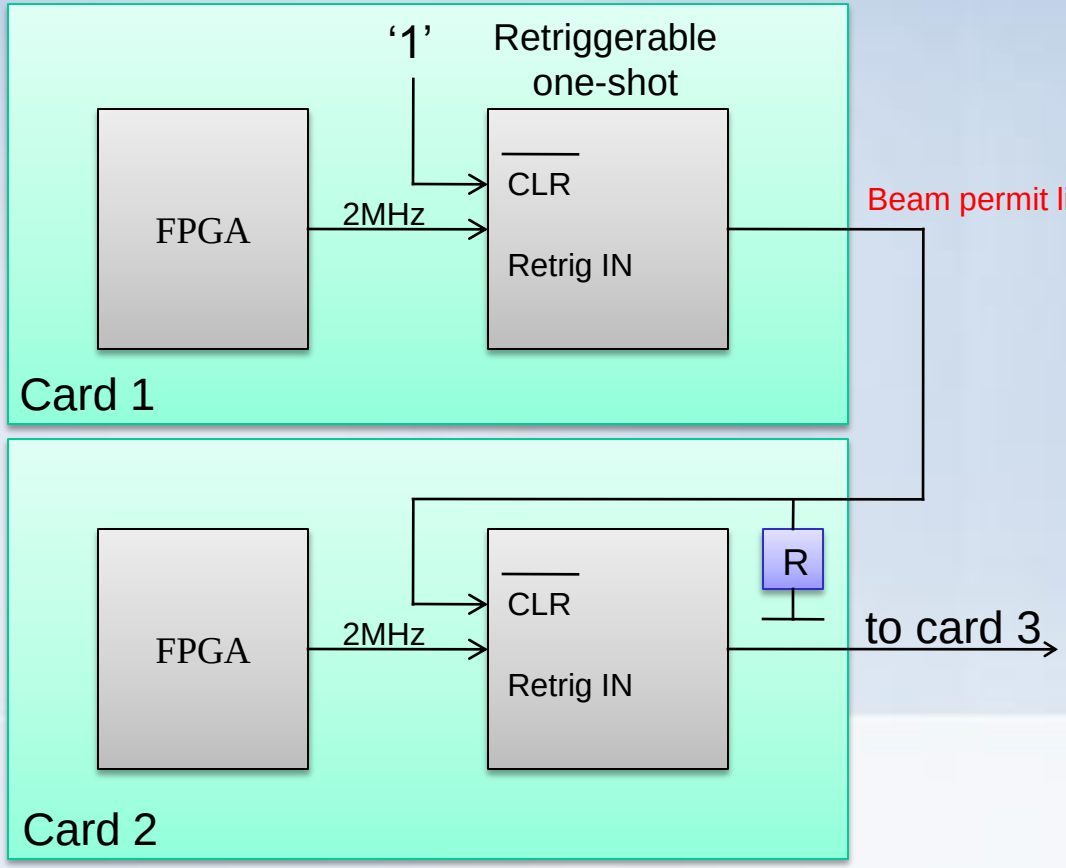






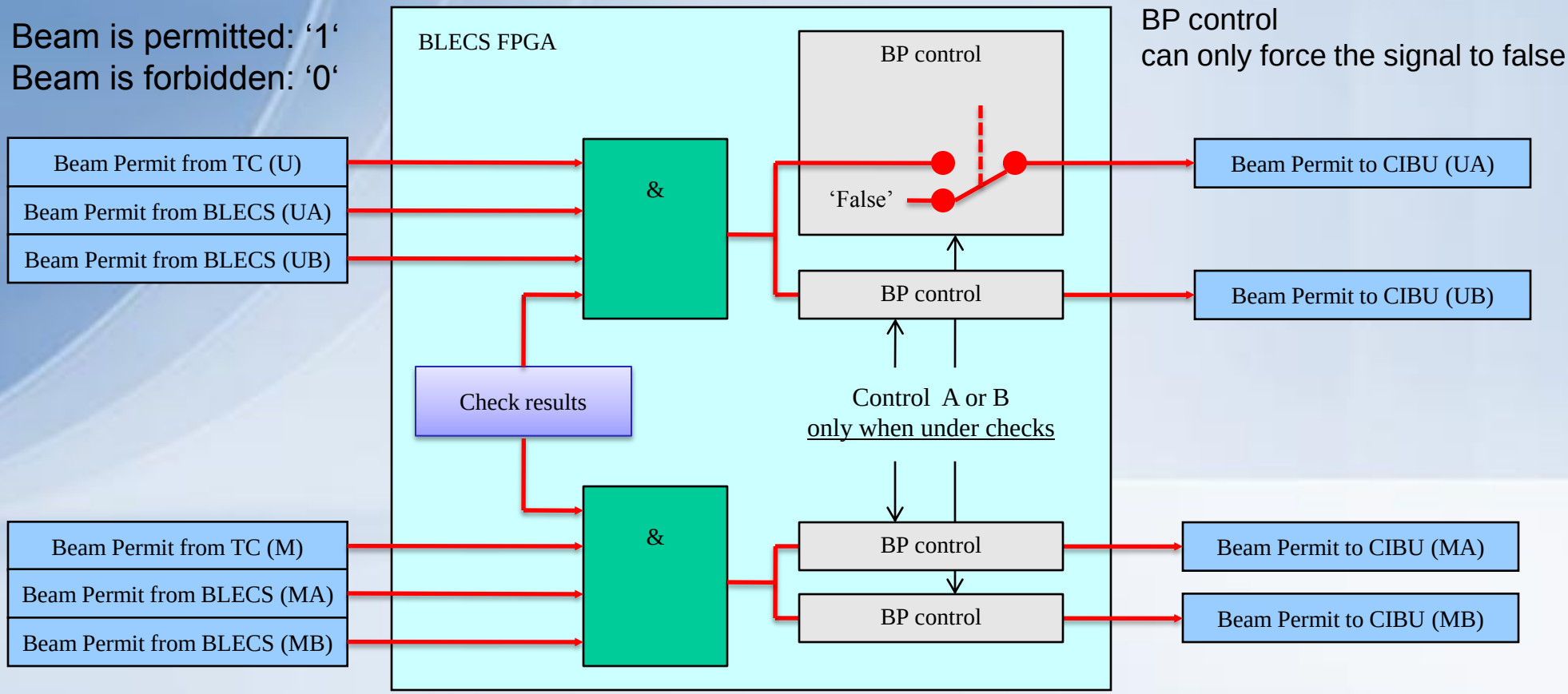
Daisy chaining principle for the beam permit signals

- The FPGA provide a clock line to the one-shot chip
- The CLR input is used to combine the signal from the previous card
- A pull-down resistor is used in case of a broken wire or a unwanted board removal
- Same principle for the 2 links
  Inside the crate (BLETC to BLETC)
  Between the crates (BLECS to BLECS)

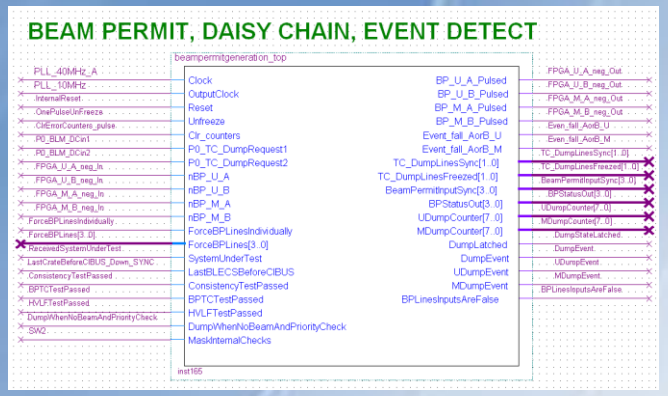


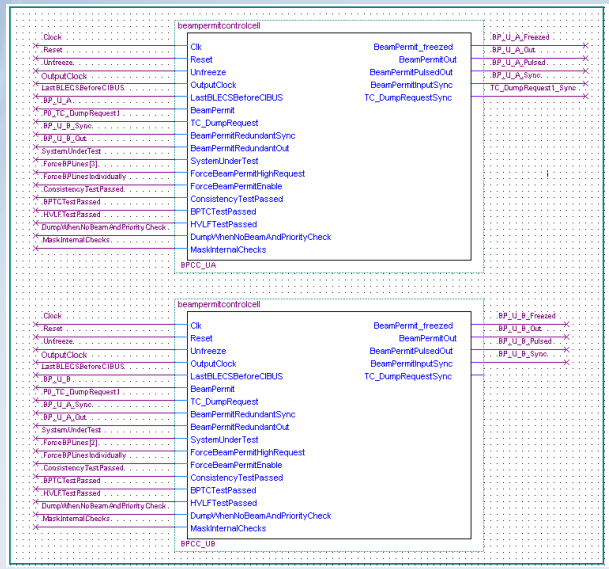
Beam permit combination implementation

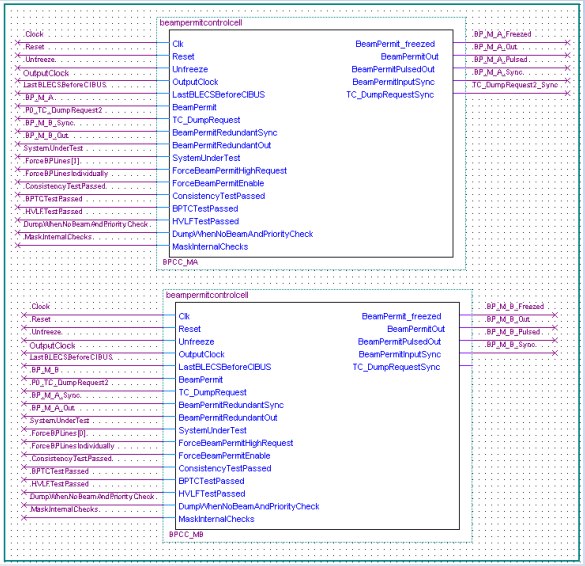
The beam permit signal is travelling on the VME P0 connector from the first BLETC (1) to the last BLETC (16) and then to the BLECS with a daisy chain link.
One for the unmaskable and one for the maskable

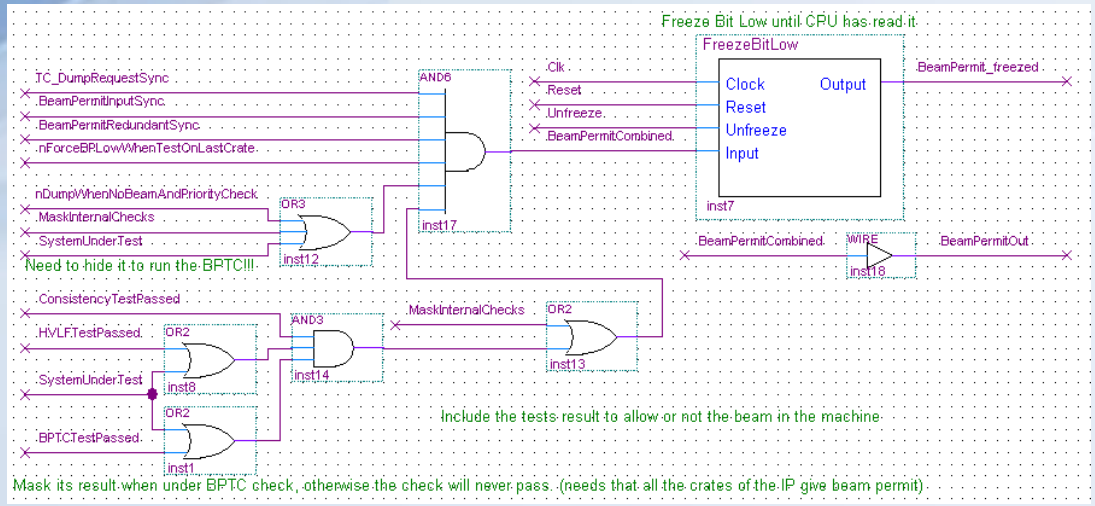


Link to the Beam Interlock System (BIS) Implementation









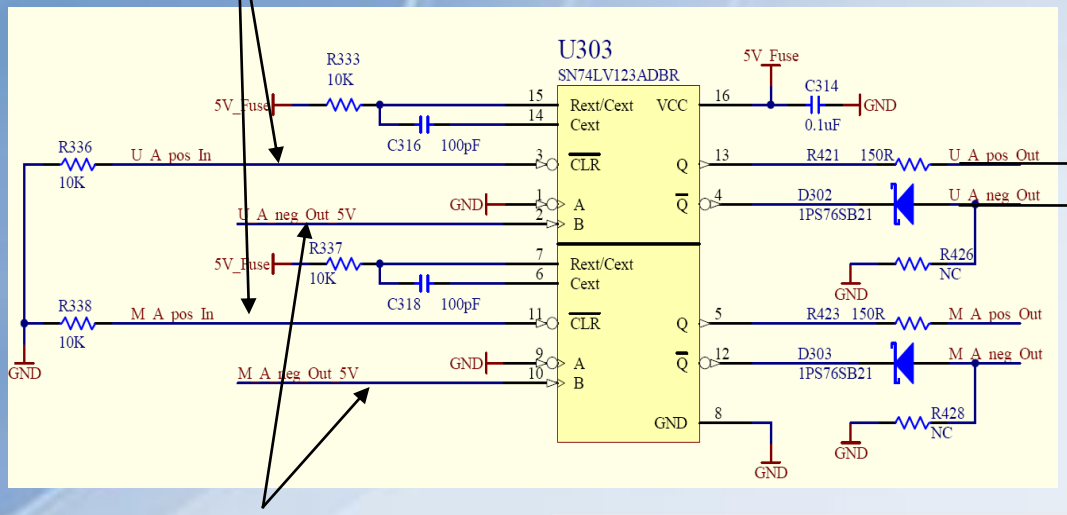
Time stamping of the BLM beam dump request

- A counter (25ns accuracy) starts in the BLECS when the BP falls
- It stops when the PM freeze event occurs (one P0 line)
- Accurate time stamp is known for the PM freeze
- Time stamp BLM dump = time stamp PM freeze - counter

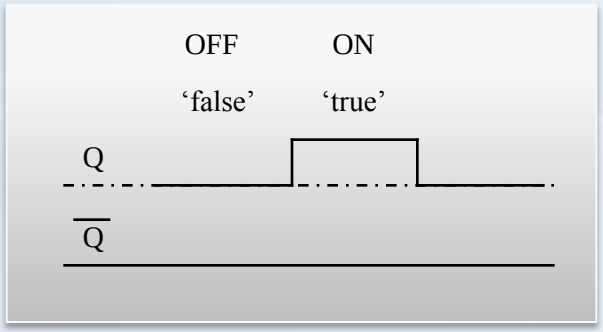
Link to the Beam Interlock System (BIS)
Electrical connections

Combiner outputs

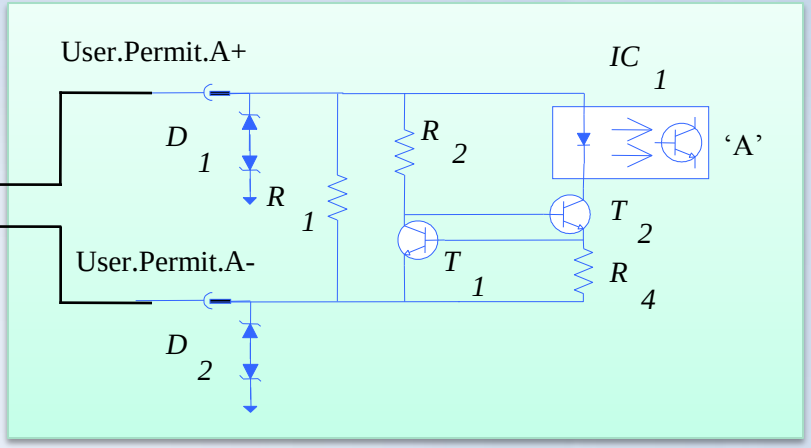
Lines from BLECS (Up)



Lines from FPGA (frequency > 1MHz)



CIBUS interface

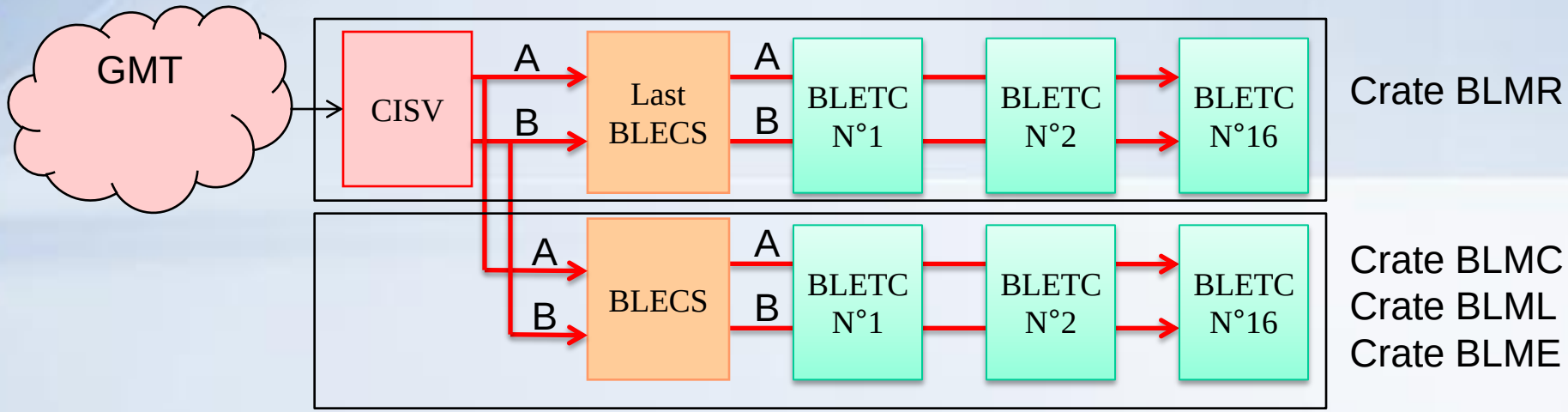


You need both lines (Q and !Q)
to be correctly connected.

http://ab-div-bdi-bl-blm.web.cern.ch/ab-div-bdi-bl-blm/Electronics/BLECS_Combiner/BLECS-Schematics/Rev3/BLECS_Combiner_Rev3.pdf

Beam energy reception and conversion

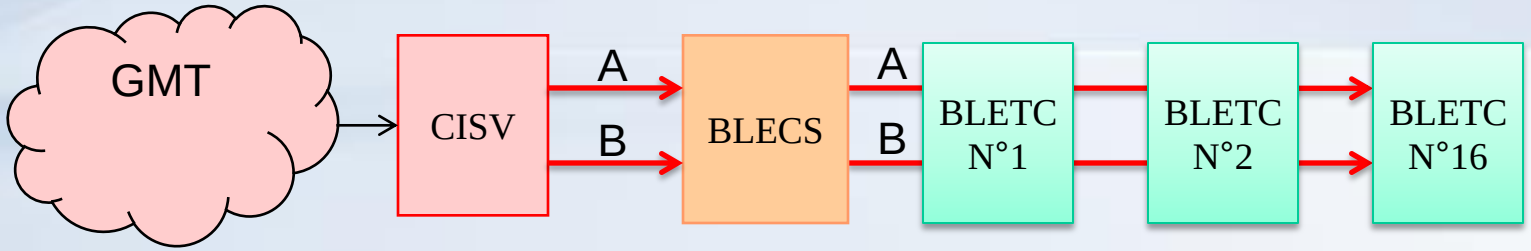
- Generated by the Beam Energy Tracking system (BETS)
- Send in the whole LHC machine through the General Machine Timing (GMT) link.
- One receiver per point (CISV), all 4 BLECS receives in parallel through 2 serial links.
- Conversion from 16bits to 5bits levels (32 levels of the BLM system).
  hardcoded inside the FPGA of the BLECS
- BLECS broadcast on 2 serial links to the 16 BLETC



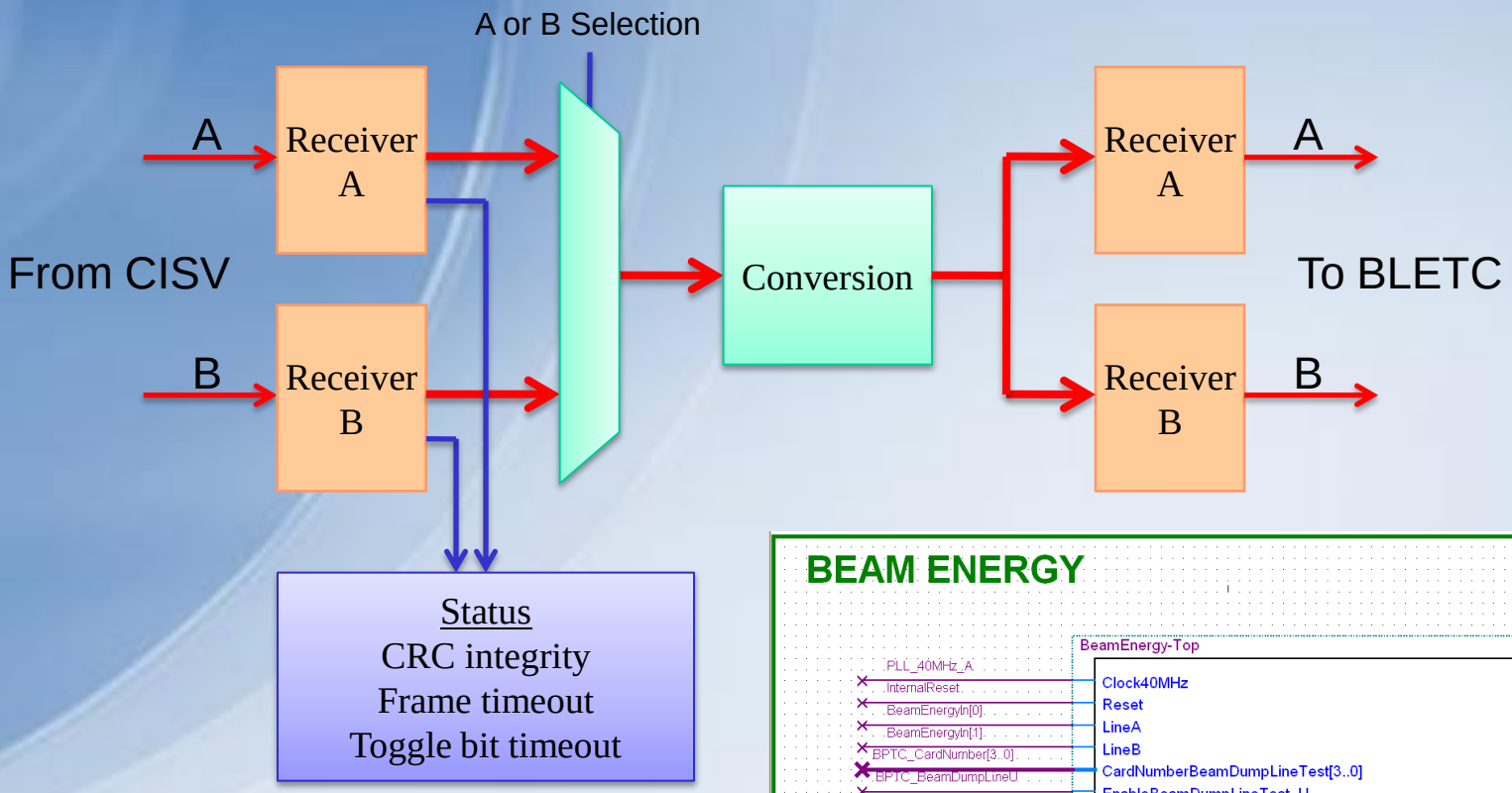
Beam energy link

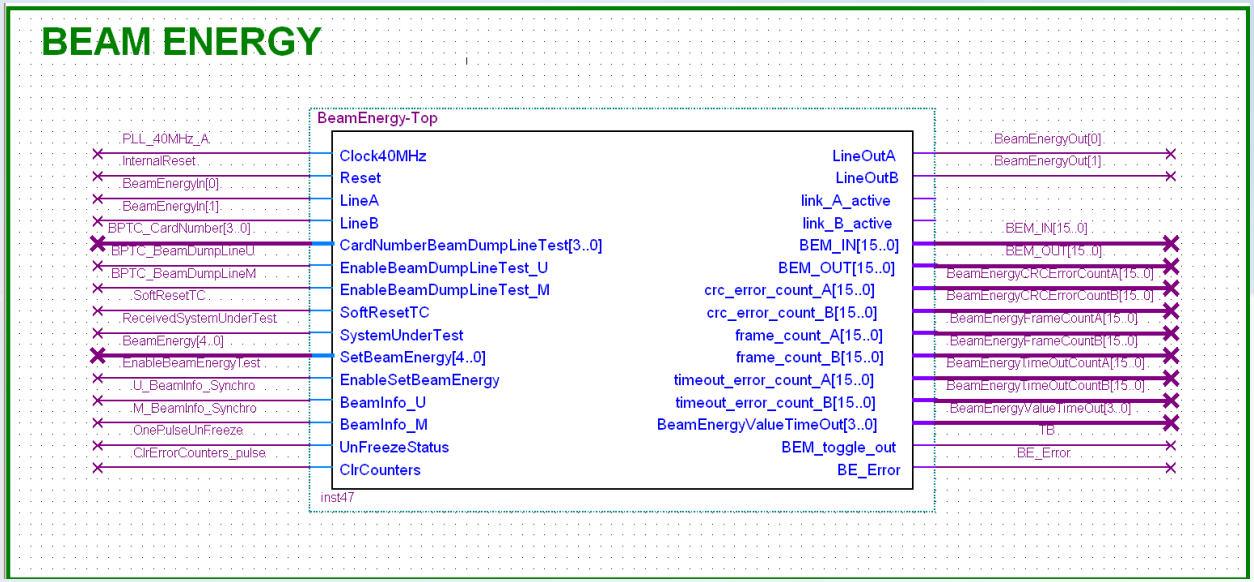
- New energy value every 100ms (one bit toggle when update)
- The energy frames are transmitted every ms
  (the energy value is repeated between new values)
- Uses a serial link, 1MHz bit rate, Manchester encoding
- The frame is 32 bits long and content:
  LHC energy header (“1001“)
  Spare bits (”000”)
  Toggle bit expected to have a transition every 100ms
  Energy value (16 bits)
  CRC (8 bits)

Error counters to the DB



Beam energy conversion implementation in the BLECS





Additional information in the link to the BLETC

CISV transmission specification
1. LHC energy header => "1001“
2. ”000”
3. Toggle bit → Toggle bit time out check (errors counter)
4. Energy value (16 bits) → Energy value (16 bits)
5. CRC (8 bits) → CRC check (errors counter)

Conversion + additional information & control

	Beam Energy (0 to 31) [5 bits]	Error bit [1 bit]	SofResetTC [1bit]	System under Test	Unmaskable Beam Info [1 bits]	Maskable Beam Info [1 bits]	BPL Unmaskable test activation [1 bit]	BPL Maskable test activation [1 bit]	Beam Permit Line test TC Card Number [4 bits]
Bit position	[15..11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3..0]
Broken link state*	31 (highest)	1	0	0	1	1	0	0	0

* Applied when both transmission are broken.

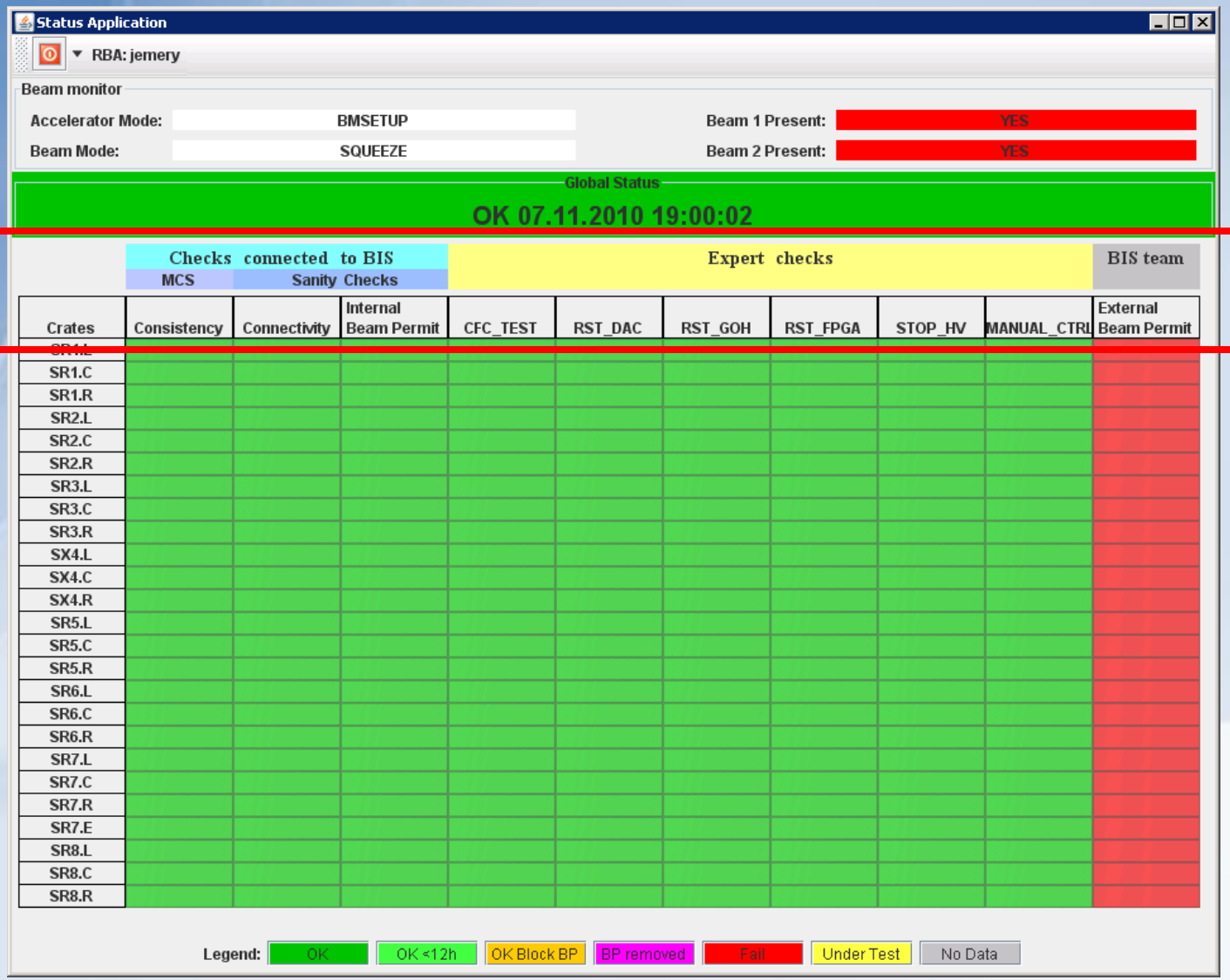
Information from the CIBUS

Used to provoke beam dump to TC individually (during Internal beam permit check)

To 16 BLETC in parallel

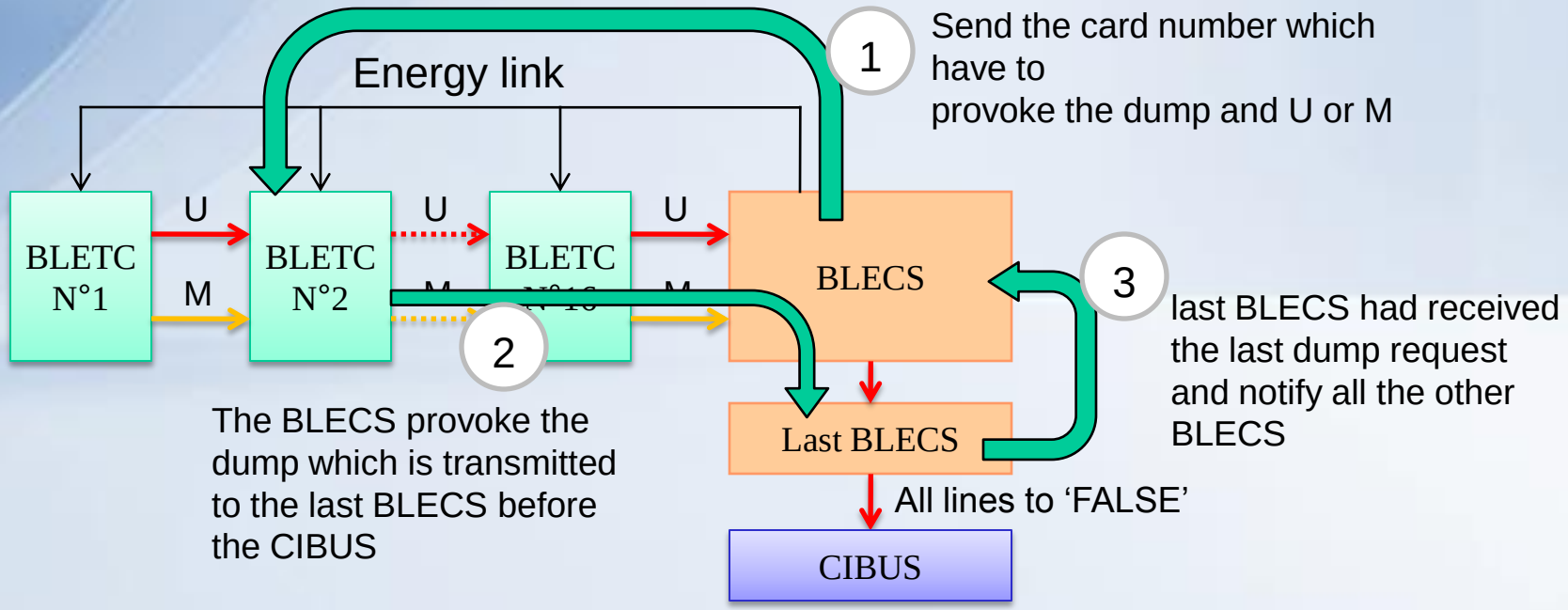
BLECS transmission specification
1. ”10010000” header (8 bits)
2. Composite data (16 bits)
3. Toggle bit + ”000” (4 bits)
4. CRC (4 bits)

BLM checks overview



Internal beam permit check

- Check the beam permit lines (BPL) inside the crate
- Check the BPL between the crates (on the same IP)
- Check results are saved in the database



External beam permit check

Verifies the link BLM to BIS

BLM system provides a software interface to modify the lines state (A or B)

Check manage by BIS team

Regular check are foreseen

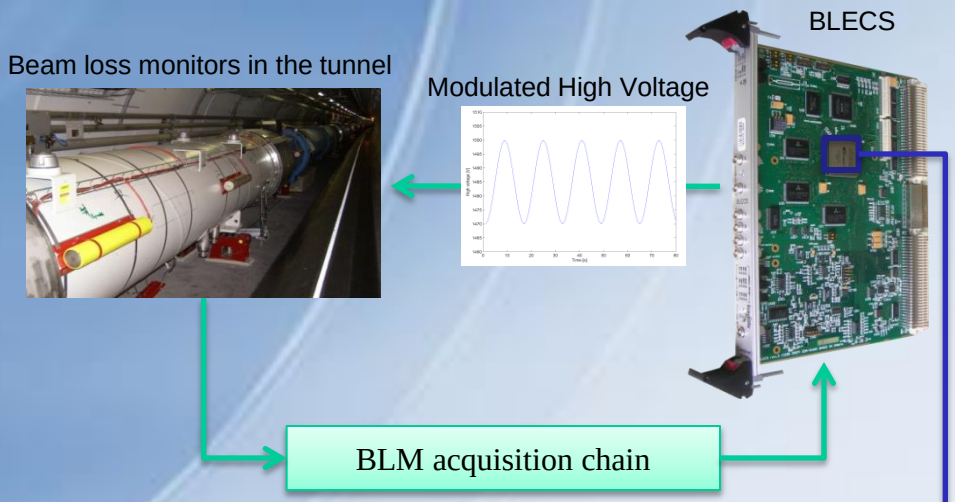
Daisy chained BLM crates

U

M

Interlock Interfaces
[CIBUS] TE-MPE-MI

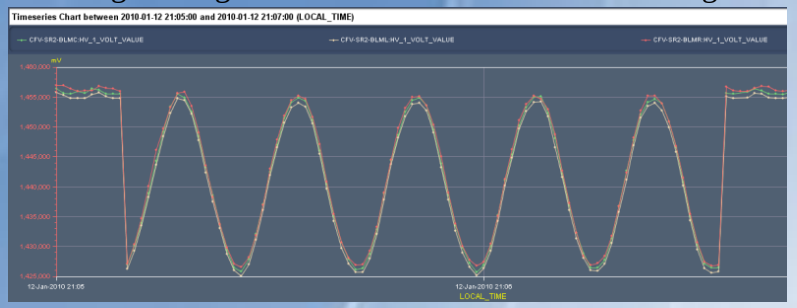
Connectivity check



- Novel technique of system integrity check (modulation of bias voltage; amplitude and phase analysis)
- Functional specification given by PhD thesis of G. Guaglio
- Last processing improvement in winter 2009
- Connected to the BIS in spring 2010
- Mandatory execution every 24h, beam injection blocked if non-conformities are found

Connectivity check

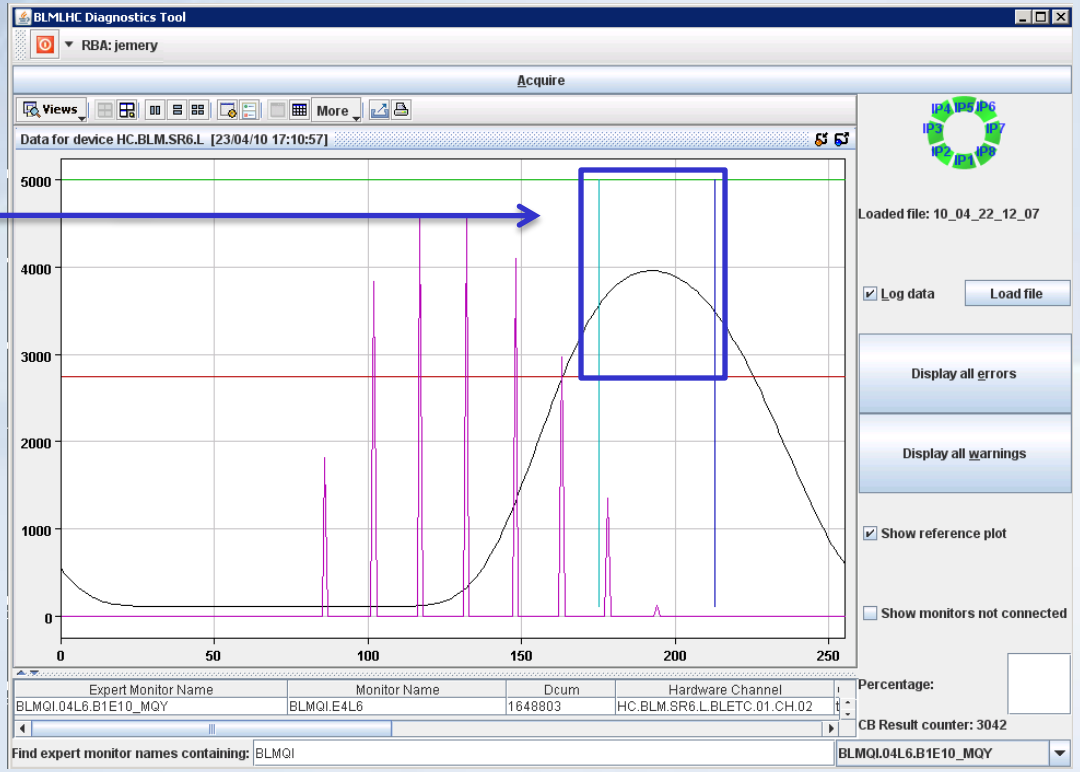
The high voltage is modulated with a 30V/60mHz signal



A current is induced in the monitors and measured by the system

Last full period in saved in the SRAM and processed

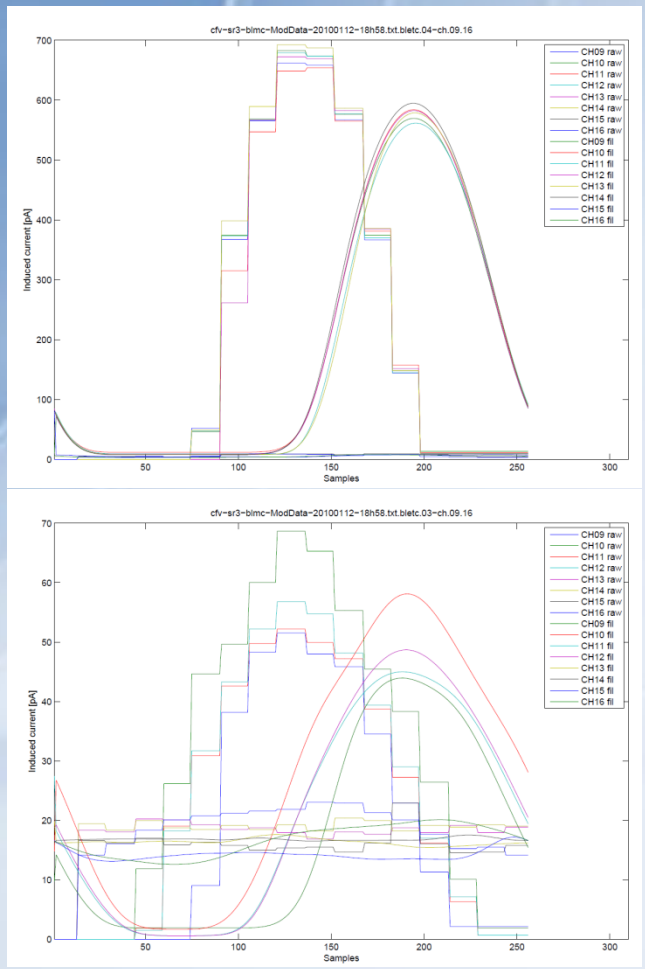
Internal thresholds settings overview in the diagnostic tool.
(unique for each monitor)



The phase and amplitude are calculated and compared to predefined thresholds in the BLECS card.

The raw and filtered data is kept into the SRAM and can be retrieve with the Diagnostic application

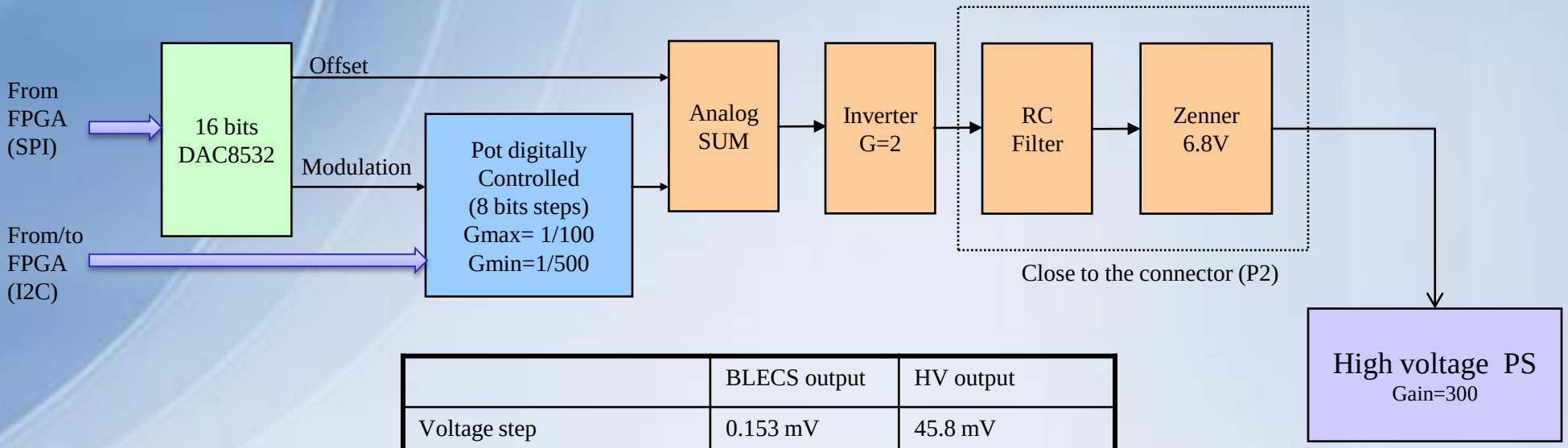
Connectivity check procedure



- A full signal period is saved inside the SRAM
- A Low pass filter is applied
- The peak to peak amplitude is calculated
- The phase difference with the HV control is extracted
- The results are compared against thresholds to take decision

Measurements and system non-conformities will be presented Tuesday morning

Control of the HV supplies



	BLECS output	HV output
Voltage step	0.153 mV	45.8 mV
Voltage range	6.8 V	2040 V
Modulation range peak-peak (theoretical values)	78nV to 100mV	23V to 30V

Ionization chambers high voltage controlled by 0-10V signal
Analog sum between the working voltage 5V-6.8V and a small modulation (16mV)

Experts checks: Commands through the HV

- Control of the BLECF test mode through the HV
- 4 different levels (one operational and 3 tests)
  Normal operation, test_cfc, reset_dac, reset_goh
- Additional one added “FPGA reset”, reset_goh level for 10min.
- Theses levels are different for each point
- Values are stored in secure database (LSA) and in NV memory
- Stop HV: Procedure to stop easily the monitors supply (not implemented yet)

Hardware timers

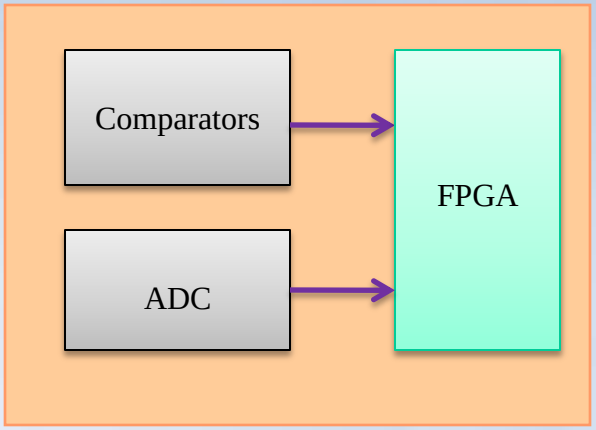
- Implementation of the checks result validity expiration
- 1) MCS Consistency 2) Sanity Checks
- Rearmed when the check runs successfully
- 2 level of priority: Normal after 12h and High after 24h
- If High, next injection inside the LHC not possible (BP kept by BLECS low)

VME voltages monitoring

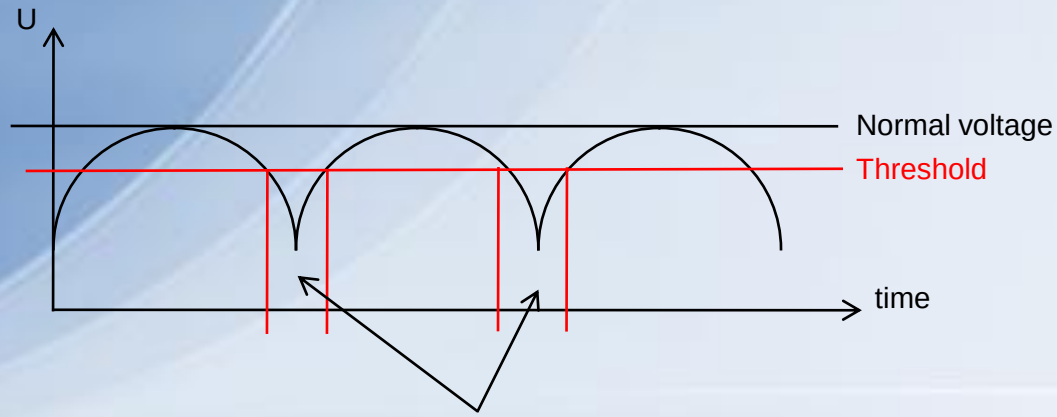
The voltages on the combiner are monitored since some ripples due to ageing were observed on previous BLM system.

<u>There are 2 ways to observe it:</u>

- With the comparators connected to counters
- With ADC values (~5kHz), the FPGA calculate the delta (max – min) when this value increase, its means there is ripples.



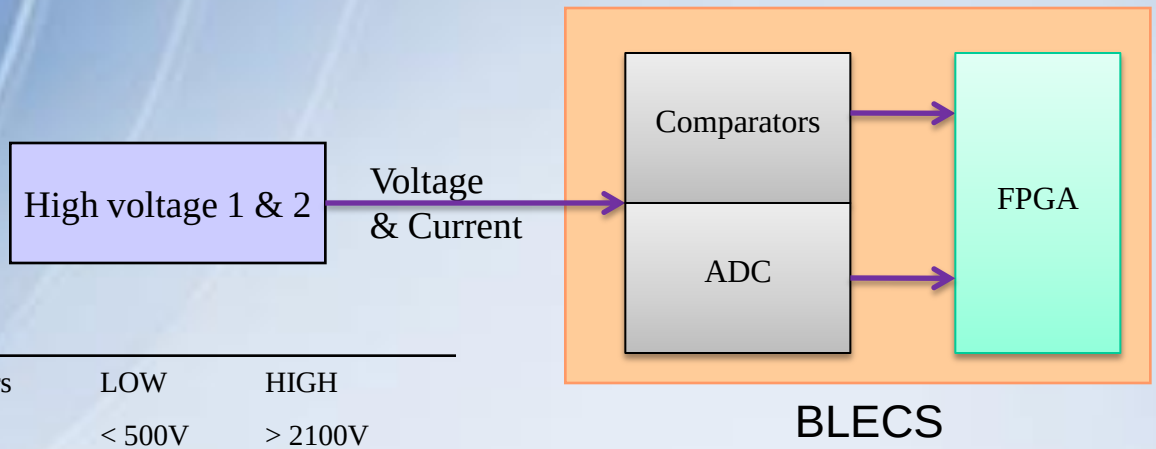
BLECS



Under the threshold value:
the comparator notify it, the counter is increasing by one
<u>OR t</u>he counter is measuring the time below

	Digitalization	comparator
5V (VME)		
3V3 (VME)		
±12V (VME) not used on the board		
5V (P0 Analog)		
15V (P0 Analog)		
-15V (P0 Analog)		
5V (Reference of the DAC)		
10V (HV comparator ref 2x)		

High voltage supplies monitoring



Comparators	LOW	HIGH
Voltage	< 500V	> 2100V
Current	< 0.5mA	> 18mA

	BLECS input	@ the HV [V]	@ the HV [I]
ADC maximum resolution (DC) 24 bits	0.6 mV	0.18 mV	1.2 nA
Measured noise (over 10h)	1.61 mV	0.5V @ 1505V	40A @ 1.3mA

The high voltage power supplies have analog output monitors to view the voltage and current levels, these signals are digitalized with an ADC. There are also comparators checking the levels.

BLECS overview

- Links the BLM system to the BIS system
- Receives, converts and send the beam energy
- Request periodic checks
- Checks the system integrity and takes decision
- Blocks the BP if a non-conformity is found
- Controls the monitors' HV
- Monitor the voltages supplies

Audit of the BLM LHC system

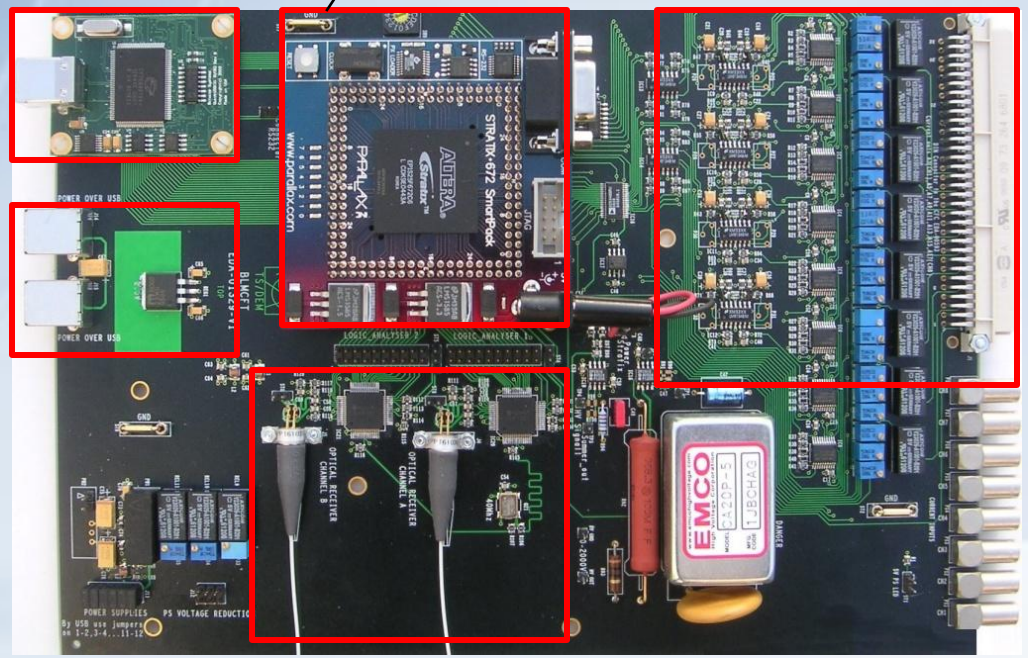
BLECF mobile tester
BLECS test bench

BLECF mobile tester

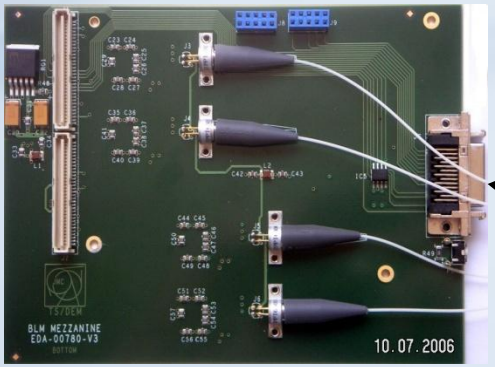
FPGA module (parallax) with custom code including the BLETC processing

USB module "Quick USB"

Power the board from the USB



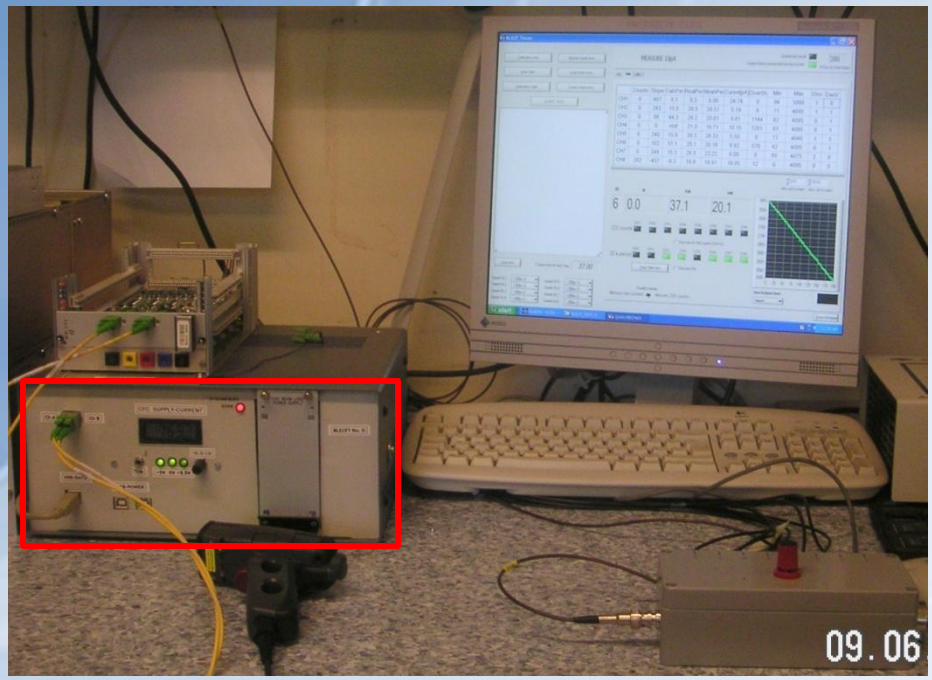
Current source circuits to feed the BLECF 10pA to 1mA on 8 channels



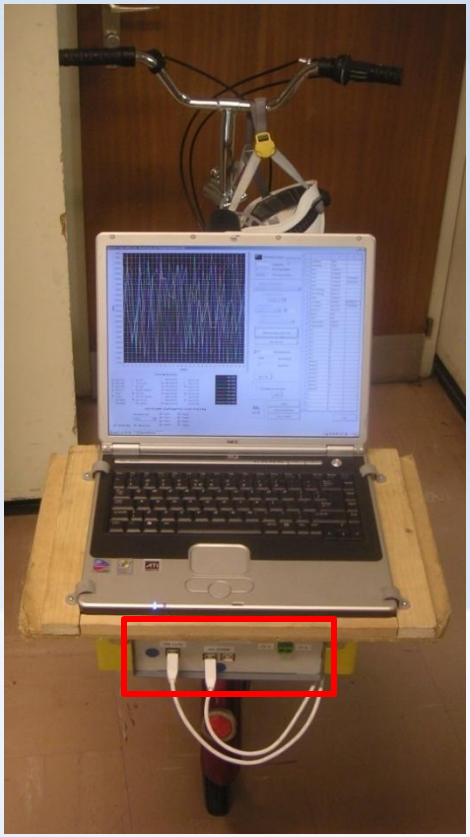
Optical receiver bloc from the BLM mezzanine

BLECF mobile tester

Lab version



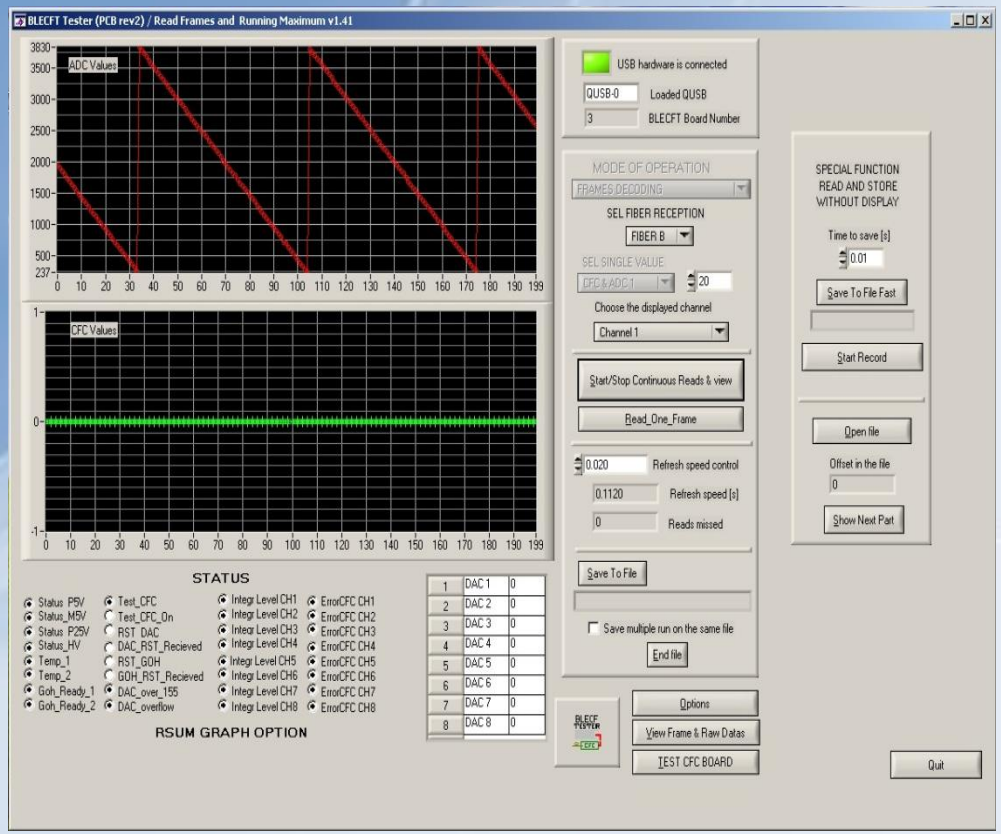
Tunnel version



BLECF mobile tester software

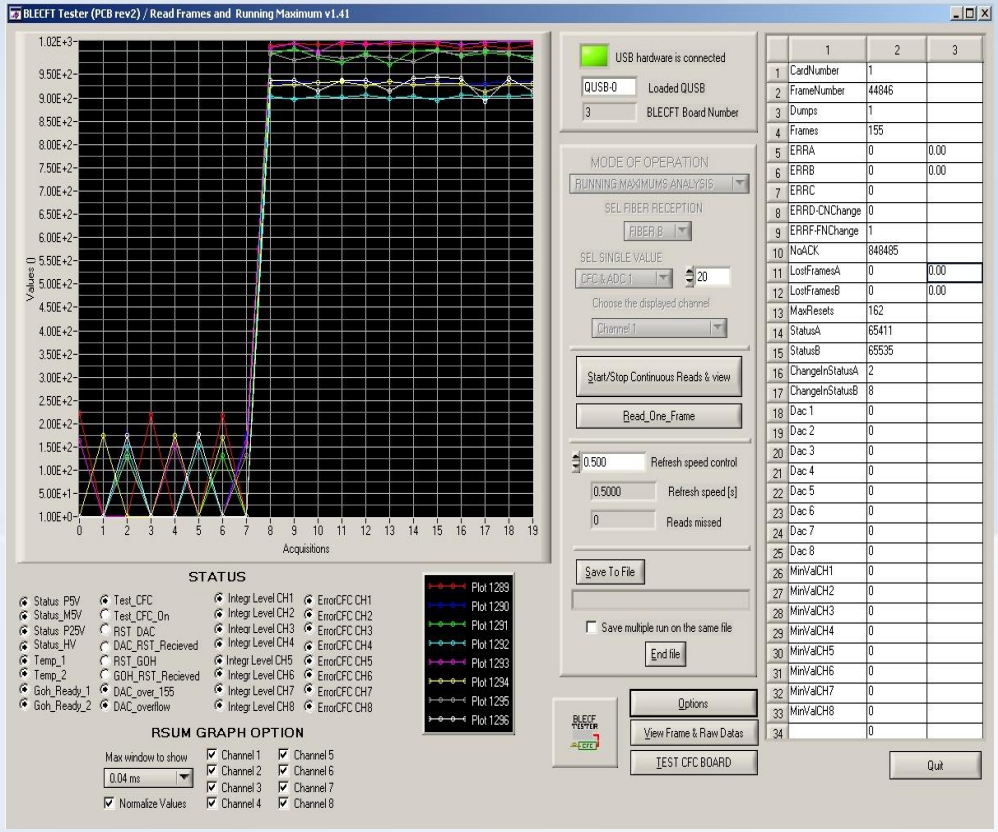
Frame mode

The software takes the complete frames from the BLECF , analyze it and show it.



Running sums mode

The core processing of the BLM system holds inside the FPGA taken from the BLETC. The software takes the result of it and show it.



BLECF mobile tester software

- Developed in C with Labwindows/CVI (NI)
- Can read and decode the frames send from the BLECF at 100Hz, show it and save it inside a file
- Can show and save the result of the BLM processing (same as BLETC)
- Full functional test (in the lab)
- Testing and validation of the installed cards (in the tunnel)

BLECF mobile tester software

1. <u>10pA calibration</u>
   Look at the ADC readings
   Calculate the exact current
   The operator correct it on the board
   Check if there are discontinuity
   Check if the signal is saturated
   Save the final value inside a file

2. <u>1mA calibration</u>
   Done with a external current source (keithley)
   The operator correct it on the board
   Save the final value inside a file

3. <u>Complete test</u>
   Check the integrity of the optical fiber link
   Check if the status are working
   Check the HV level thresholds
   Check the linearity with internal sources
   Save everything inside a file

REPORT_CFCBoard_NormalT__DN_67_0.txt - Notepad

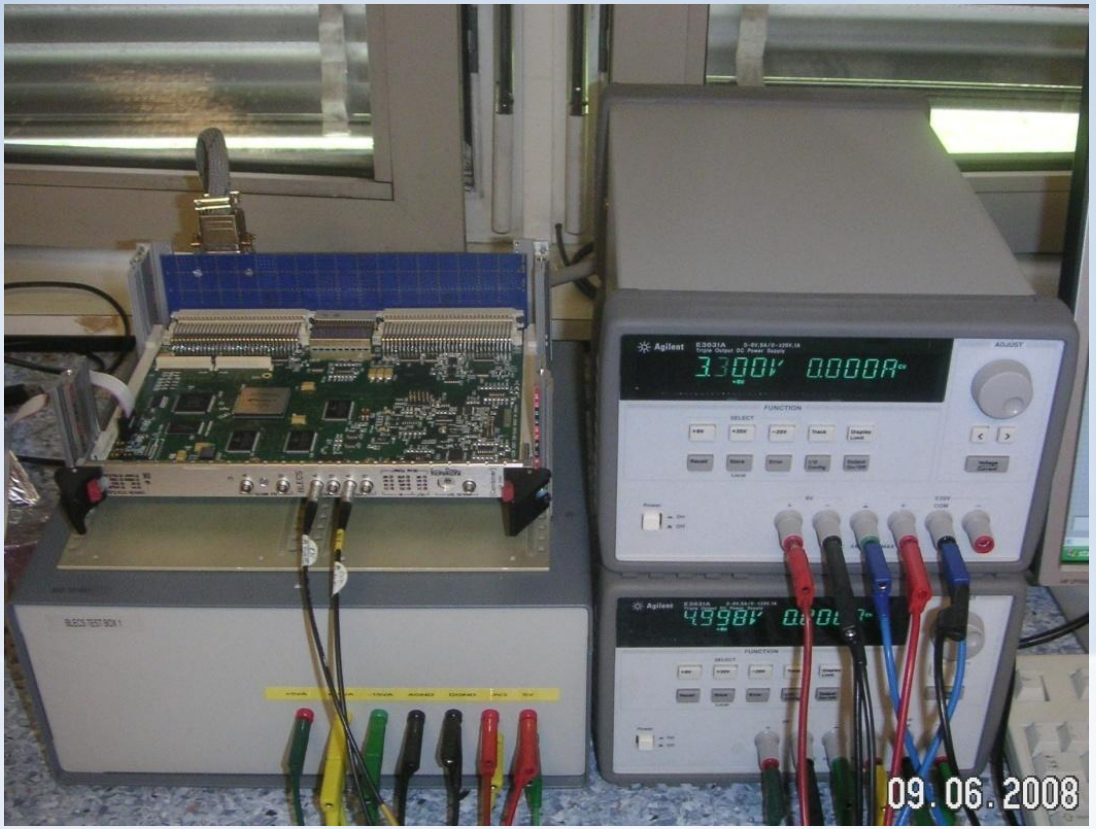
File Edit Format View Help

```
G:\\Divisions\\sl\\DIV_SL\\BI\\PM\\BLM_BLECF\\BLECF_TEST_REPORT\\REPORT_CFCBoar

FUNCTIONAL TEST OF THE TUNNEL ACQUISITION BOARD FOR THE LHC

Mon Oct 15 14:10:53 2007

------------------------------------------------------------

Device number send through the fiber : 67

PCB version : EDA-00593-V6

Comments :
Type your comments that will appear in the report file

------------------------------------------------------------

IDENTIFICATION BARCODES
------------------------------------------------------------
-- DONE -- (FPGA barcode number, FPGA internal number, Board number)    passed
------------------------------------------------------------
BLECF_0067
FPGA  NO.067
- 0006222348proto005
30201010069242
30201010056165


MEASURE 10PA => Start at 256908.18 [s]  (12.50 - 25.00)
------------------------------------------------------------
CALIBRATION Offset current CH1 : 19.66 [s]   (12.50 - 25.00)            passed
CALIBRATION Offset current CH2 : 18.97 [s]   (12.50 - 25.00)            passed
CALIBRATION Offset current CH3 : 19.78 [s]   (12.50 - 25.00)            passed
CALIBRATION Offset current CH4 : 19.66 [s]   (12.50 - 25.00)            passed
CALIBRATION Offset current CH5 : 20.67 [s]   (12.50 - 25.00)            passed
CALIBRATION Offset current CH6 : 19.58 [s]   (12.50 - 25.00)            passed
CALIBRATION Offset current CH7 : 19.23 [s]   (12.50 - 25.00)            passed
CALIBRATION Offset current CH8 : 17.98 [s]   (12.50 - 25.00)            passed
Offset current calc CH1 : 10.17 [pA]   (16.00 - 8.00)                   passed
Offset current calc CH2 : 10.55 [pA]   (16.00 - 8.00)                   passed
Offset current calc CH3 : 10.11 [pA]   (16.00 - 8.00)                   passed
Offset current calc CH4 : 10.17 [pA]   (16.00 - 8.00)                   passed
Offset current calc CH5 : 9.68 [pA]   (16.00 - 8.00)                    passed
Offset current calc CH6 : 10.22 [pA]   (16.00 - 8.00)                   passed
Offset current calc CH7 : 10.40 [pA]   (16.00 - 8.00)                   passed
Offset current calc CH8 : 11.12 [pA]   (16.00 - 8.00)                   passed
Overshot      CH1 : 0   (Max 20)                                        passed
Overshot      CH2 : 0   (Max 20)                                        passed
Overshot      CH3 : 0   (Max 20)                                        passed
Overshot      CH4 : 0   (Max 20)                                        passed
```

BLECS test bench

Test bench 1

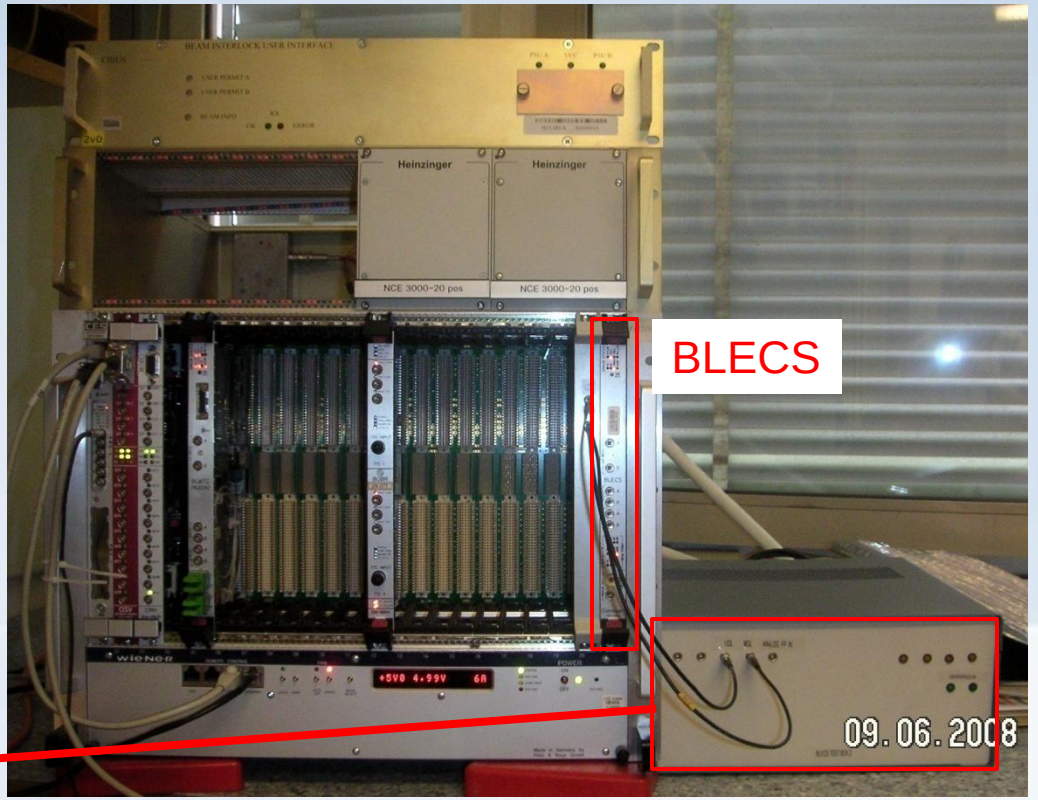
- Current measurements at all programming stages
- Automation of the 2 PS with Labview: lowering each voltages, look at the status when it changes (comparators thresholds check) and save the result inside a file



BLECS test bench

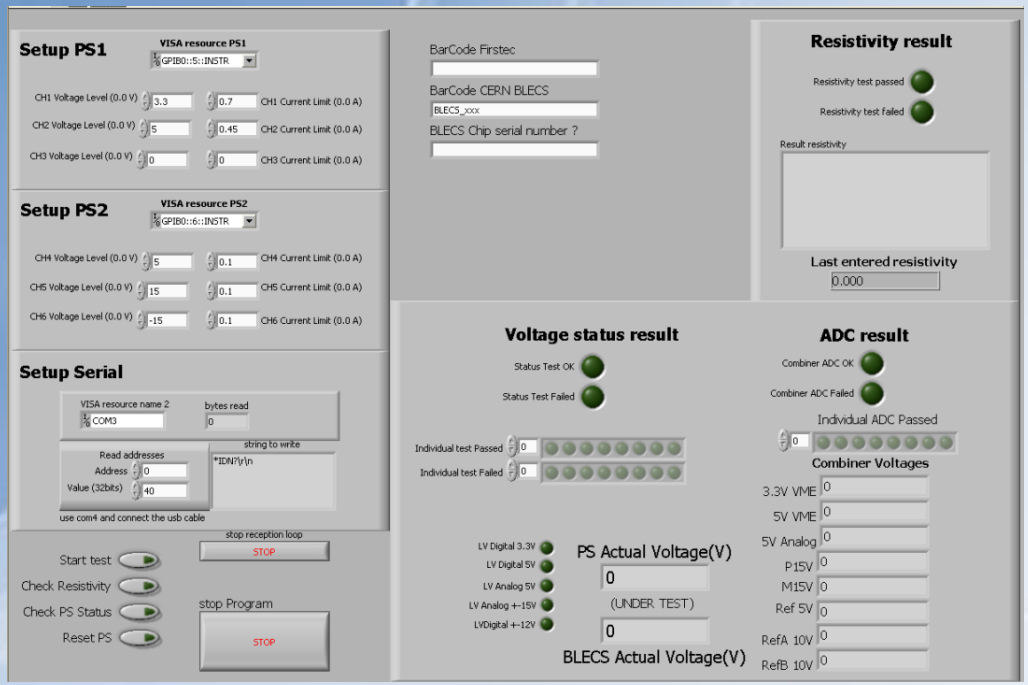
Test bench 2

- Use a standard BLM LHC crate
- Use 2 I/O modules from NI to drive the BLECS inputs and check the outputs.
- Gets data from the BLECS with the CMW wrapper (AB-CO-MA)

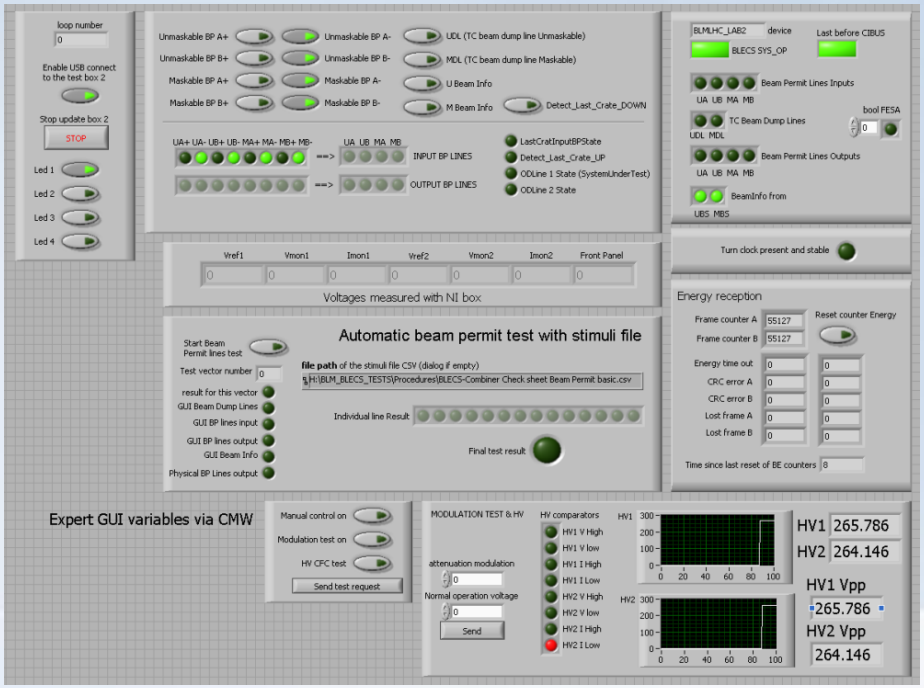


BLECS test bench

Test bench 1



Test bench 2



BLECF mobile tester

- Aim to be used to test 750 boards in the lab and in the tunnel
- Ability to test FPGA code functions
- Custom test board using commercial modules
- Software in Labwindows/CVI
- Calibration assistance
- Full automated functional test
- Saves full measurement into multiples files

BLECS test bench

- Aim to test 45 boards
- Ability to test FPGA code functions
- Use commercial input/outputs modules (analog and digital)
- Software in Labview
- Partial automation for complex logic (all beam permit lines states)
- Uses status of the FPGA continuous check for the energy reception, turn clock.
- Test report on a excel file