UNIVERSITAT DE BARCELONA

Institut de Ciències del Cosmos

Progress on ICECAL chip test

Upgrade of the front end electronics of the LHCb calorimeter

D. Gascón, E. Picatoste, A. Sanuy,

Universitat de Barcelona

Institut de Ciències del Cosmos ICC-UB

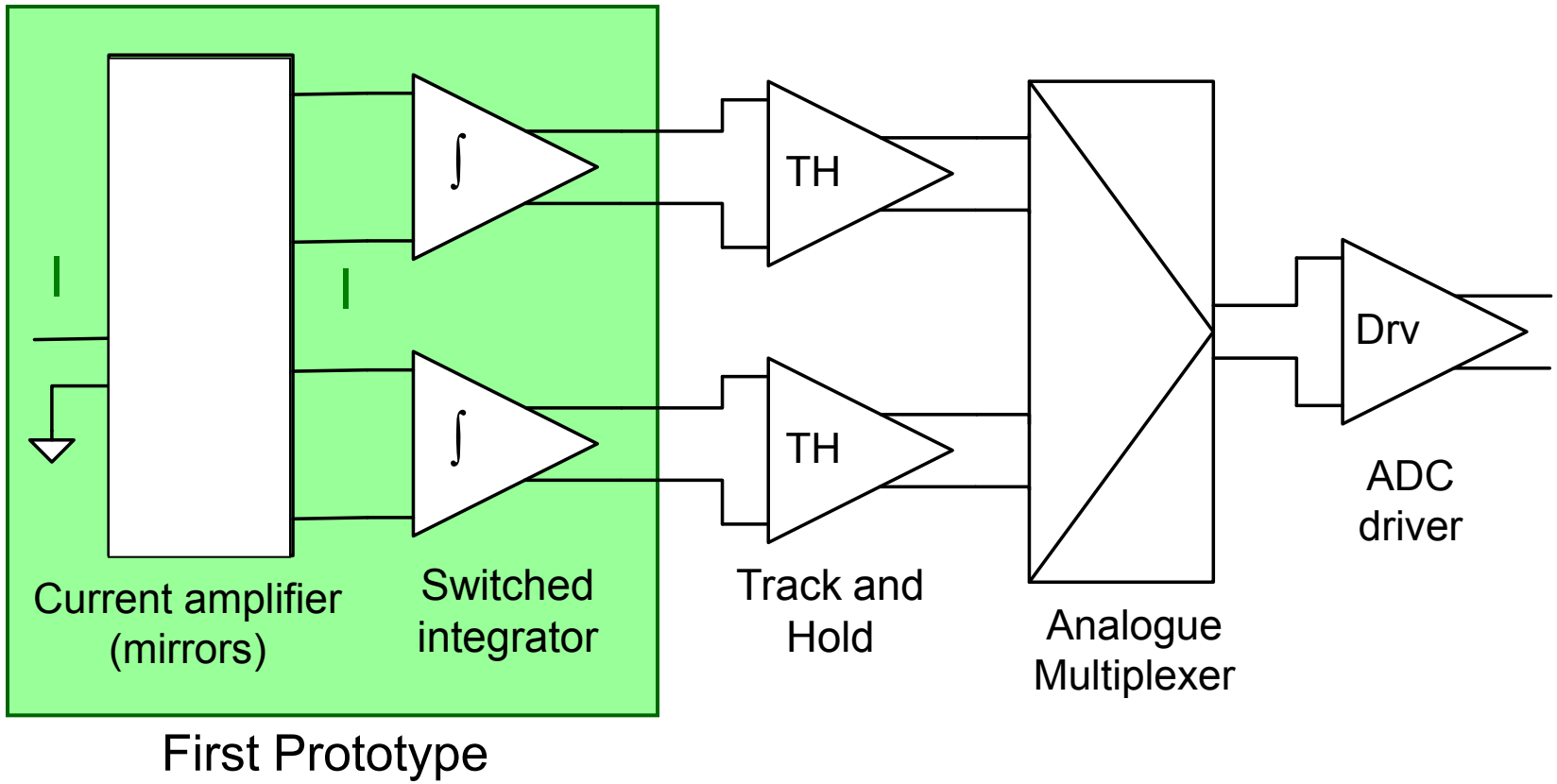
Calorimeter upgrade meeting – CERN – February 11th 2011

Outline

I. Introduction
II. Key tests on the first prototype
III. Test set-up
IV. Offset
V. Noise
VI. Input impedance
VII. Linearity
VIII. Flatness: jitter of clock vs input signal
IX. Characterization of preamp
X. Summary & news

Introduction

- ECAL analogue FE IC: channel architecture

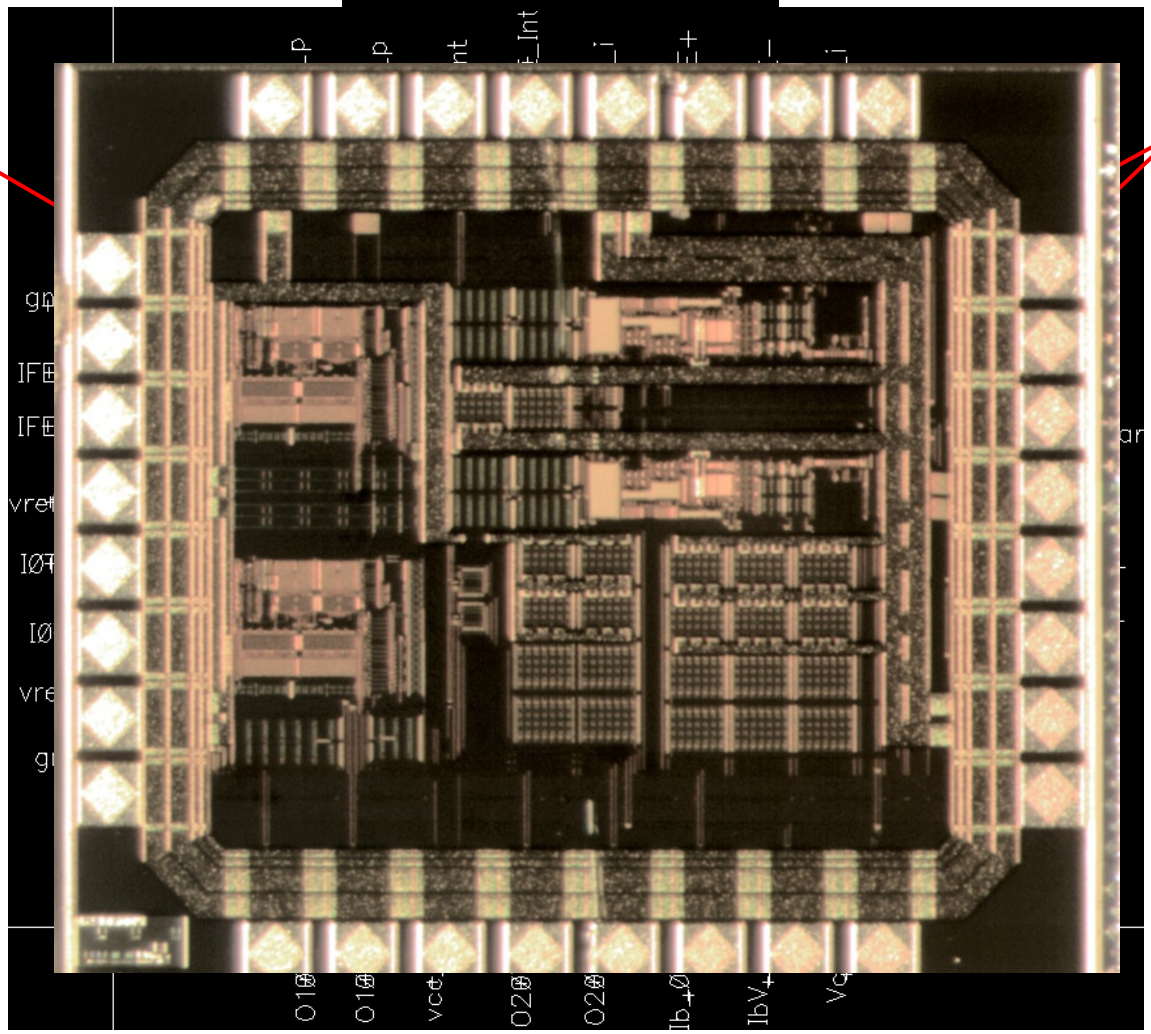


Introduction

- ICECAL chip

SiGe BiCMOS 0.35um
AMS 2 mm²
Received: October 2010

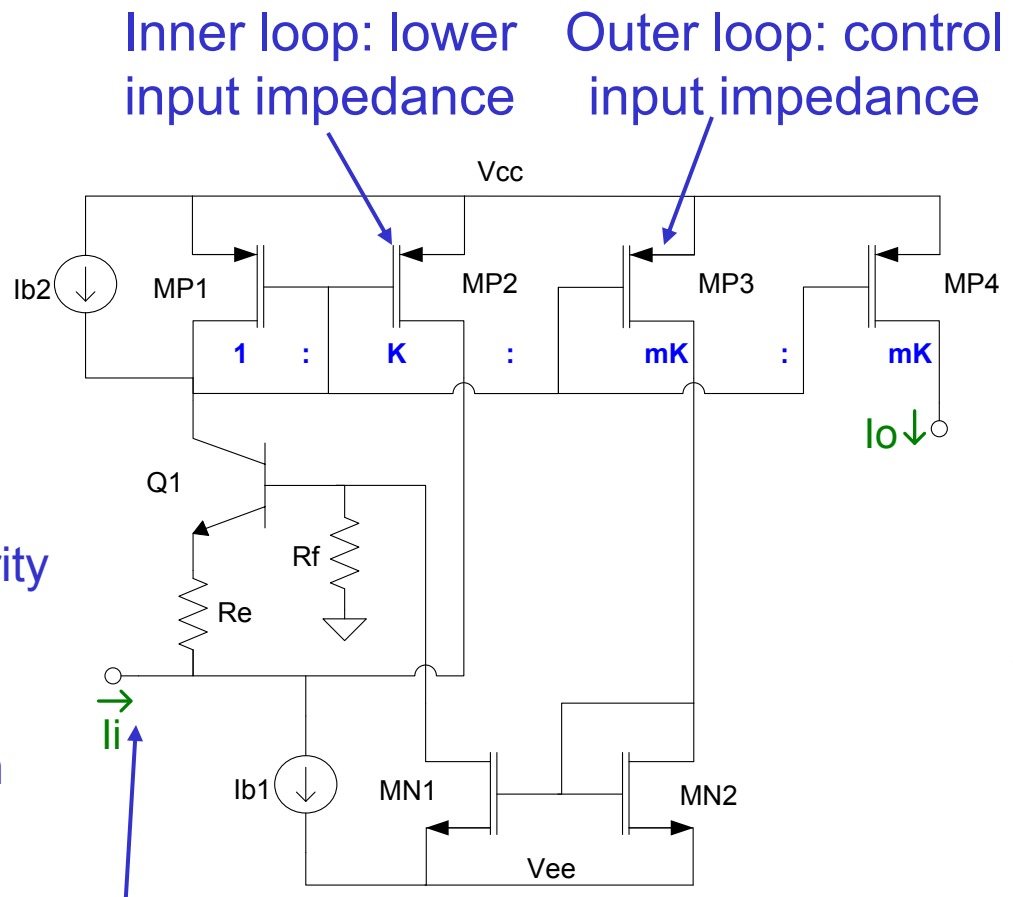
Current preamp



Integrators

Introduction: Current mode preamplifier

- Pros:
  - "Natural" current processing
  - Lower supply voltage
  - All low impedance nodes:
    - Pickup rejection
  - No external components
  - No extra pad
- Cons:
  - Trade-off in current mirrors: linearity vs bandwidth
- Low voltage
  - Only 1 Vbe for the super common base input stage
- Better in terms of ESD:
  - No input pad connected to any transistor gate or base

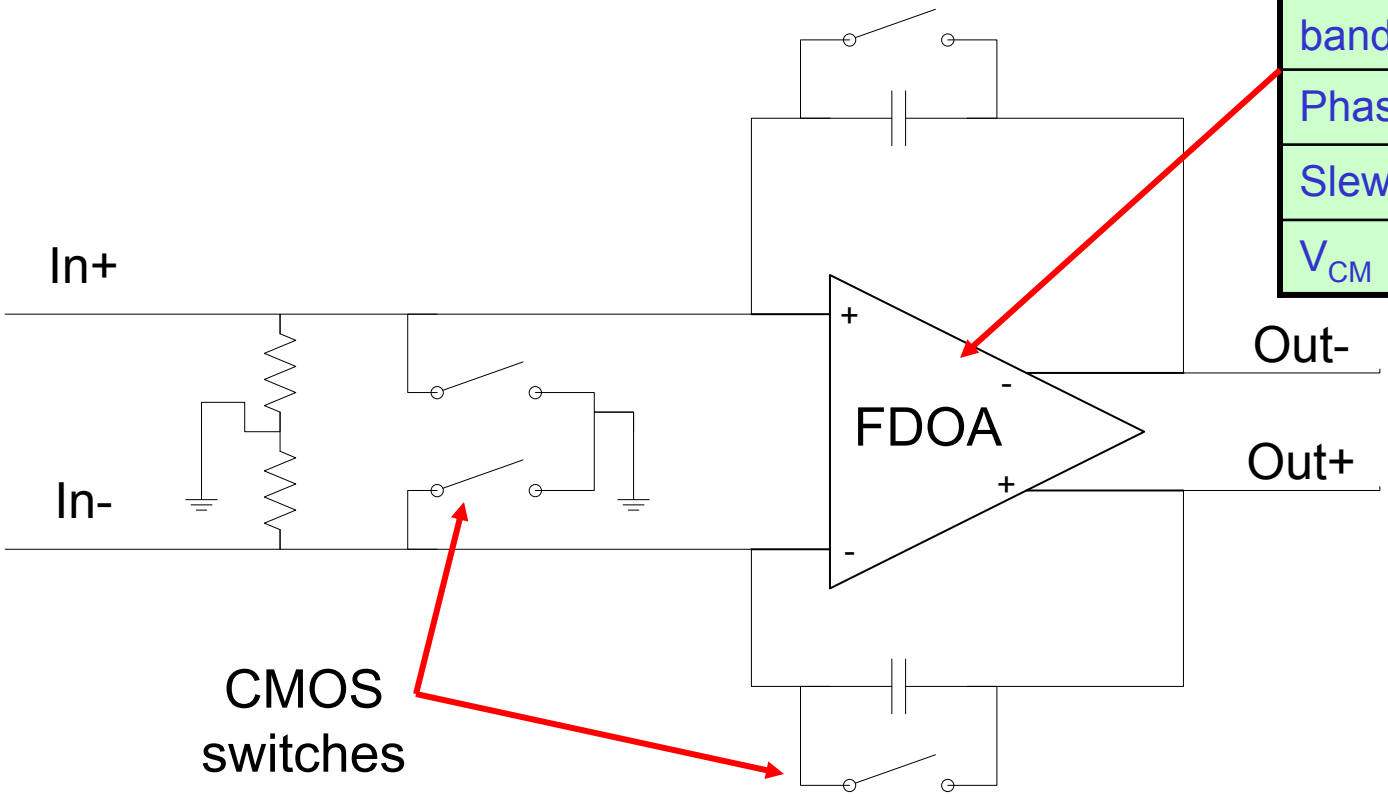


$$Z_i = \frac{1/g_{m1} + R_e}{1+K} + \frac{K}{1+K} mR_f$$

Introduction: Integrator

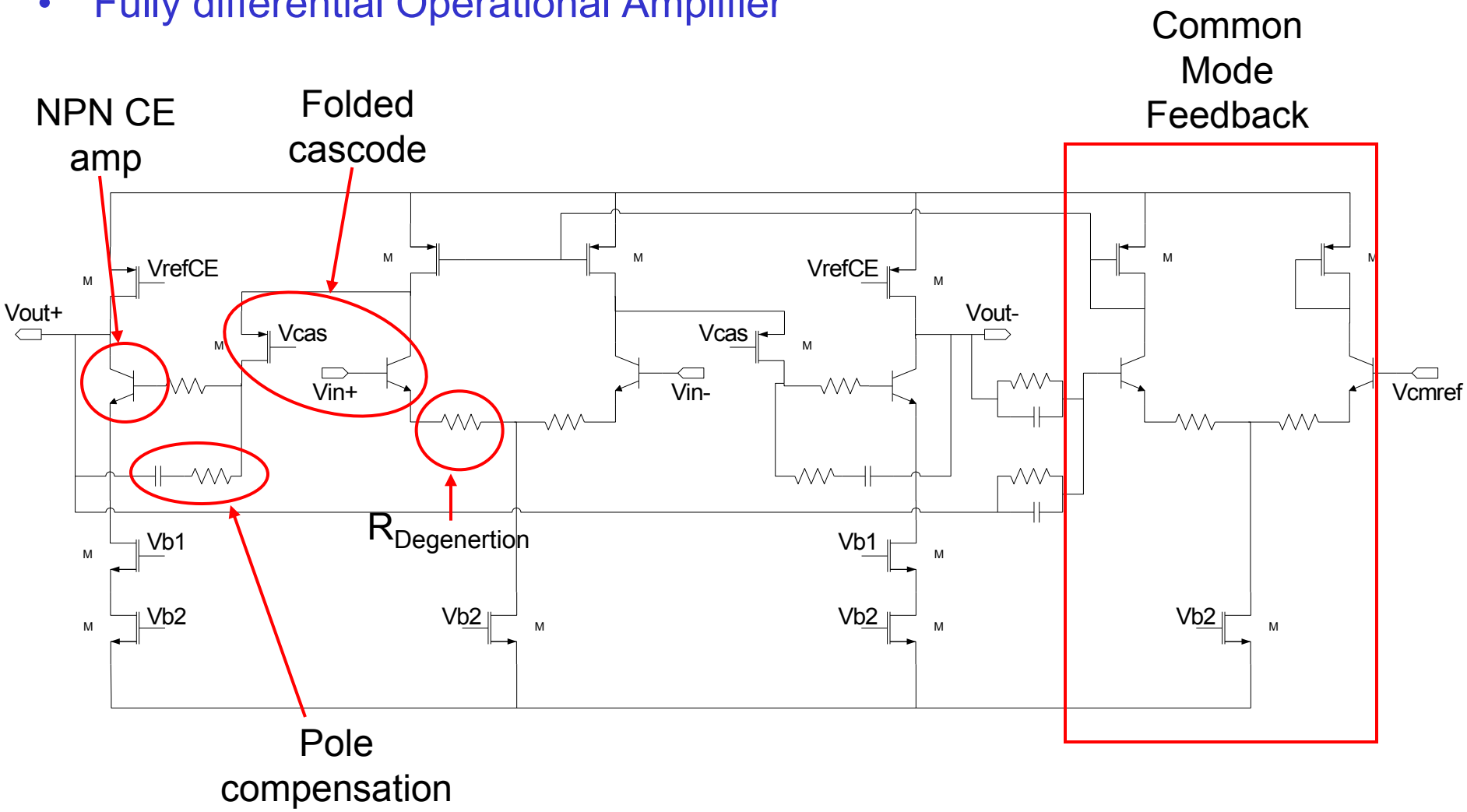
- Switched integrator architecture

FDOA specifications	
Parameter	**Value**
Gain bandwidth	500 MHz
Phase margin	> 65º
Slew rate	> 2 V/µs
V_{CM}	1.65 V



Introduction: FDOA design

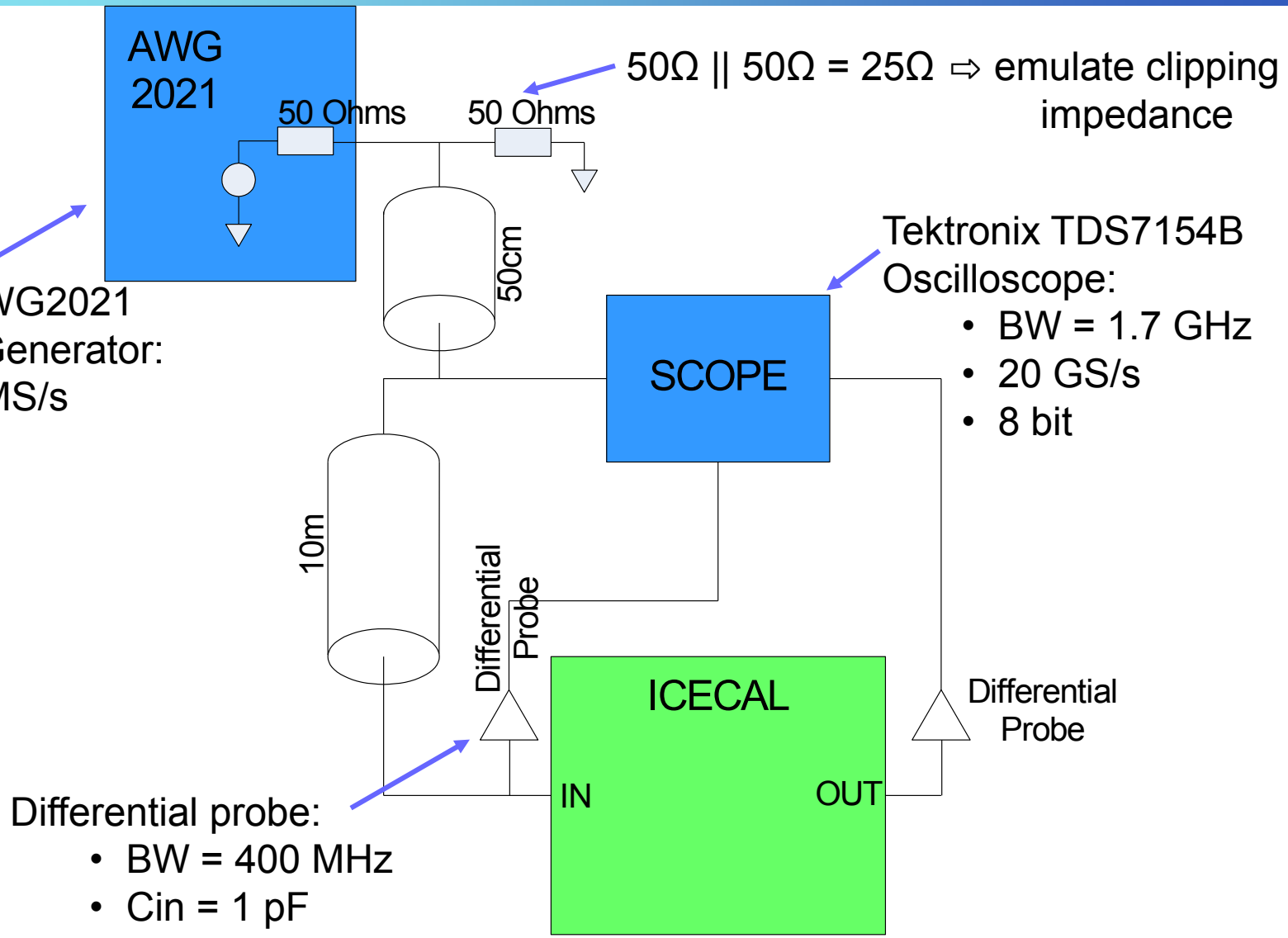
- Fully differential Operational Amplifier



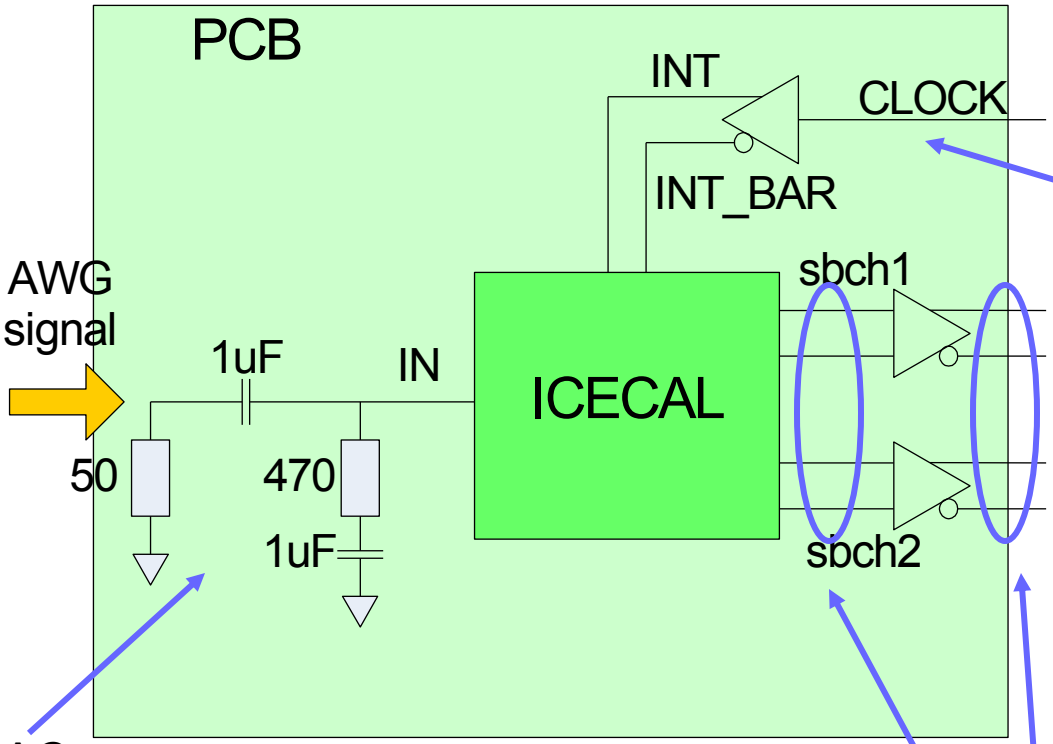
Key tests on the first prototype

- The purpose of this prototype is to test key points of a novel circuit idea:
  - Input impedance control by current feedback
  - Low noise performance
  - Dynamic range:
    - Linearity
- Also to test critical aspects of a switched solution:
  - Offset between subchannels
  - Noise
  - “Flatness” of the integrator output
    - Effect of jitter on clock versus signal
- Finally, the two key building blocks are prototyped separately in order to be characterized:
  - Current preamplifier
  - Fully differential OpAmp

Test set-up


AWG
2021
50 Ohms
50 Ohms
50Ω || 50Ω = 25Ω ⇨ emulate clipping impedance
50cm
Tektronix TDS7154B
Oscilloscope:
• BW = 1.7 GHz
• 20 GS/s
• 8 bit
Tektronix AWG2021
Waveform Generator:
• 250 MS/s
• 12 bit
SCOPE
10m
Differential
Probe
ICECAL
IN
OUT
Differential
Probe
Differential probe:
• BW = 400 MHz
• Cin = 1 pF

Test set-up

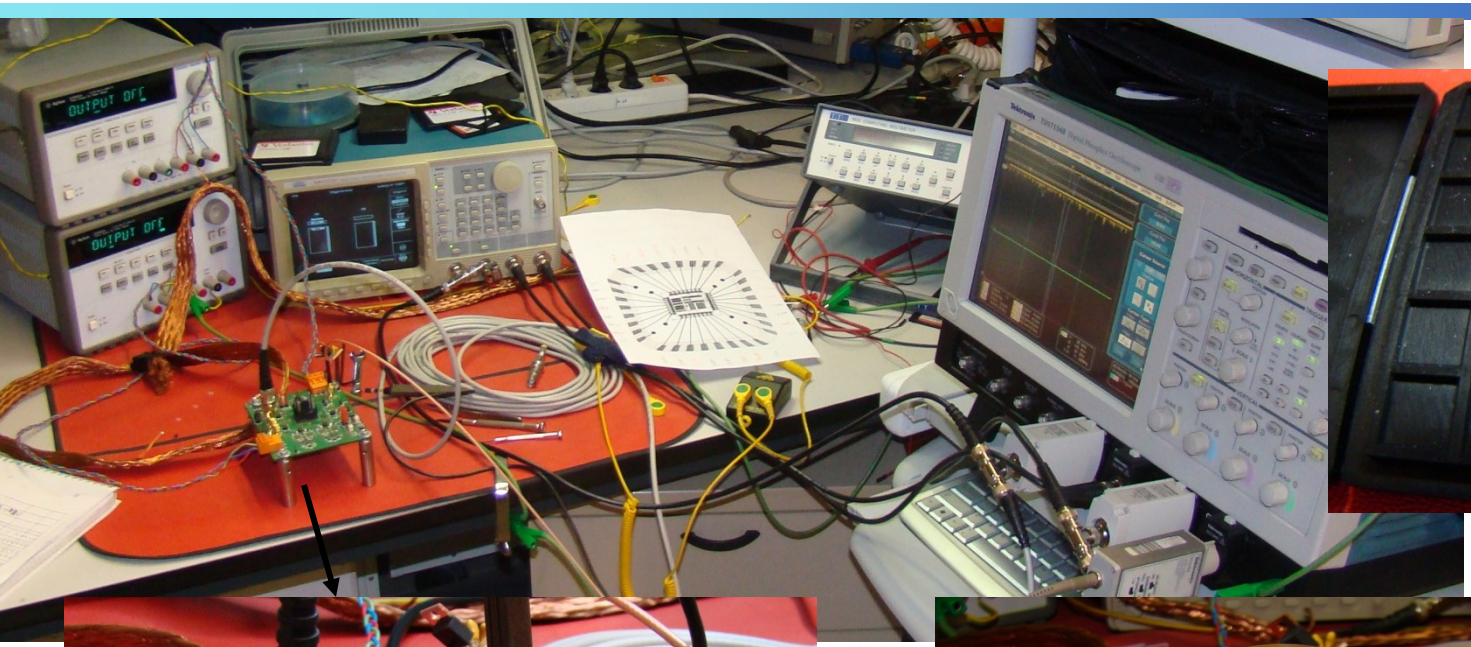


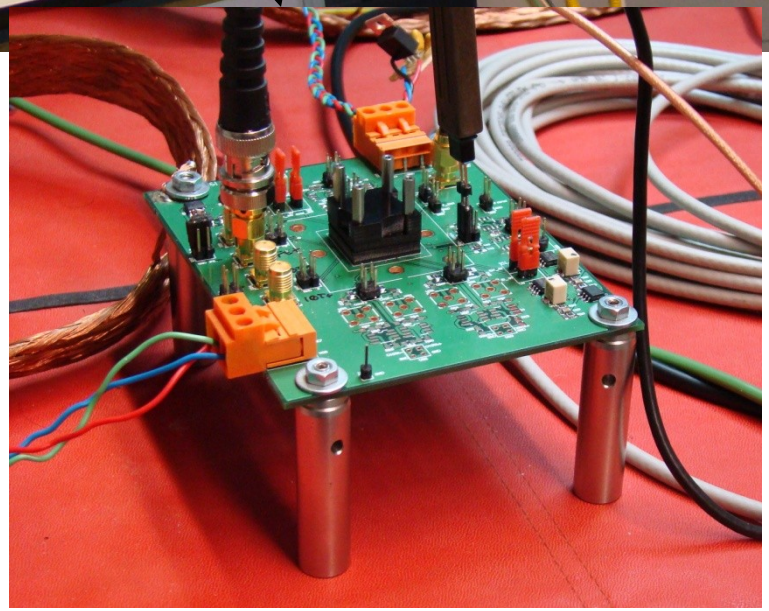
Integrator clock signals generated with comparator

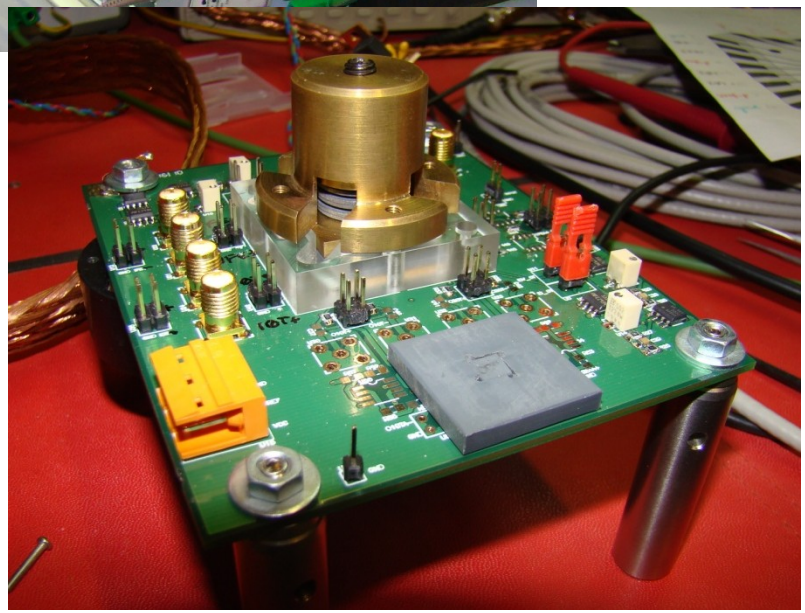
Input circuit with AC coupling and Rpar

Outputs are measured at ASIC outputs and after x10 amplification

Test set-up





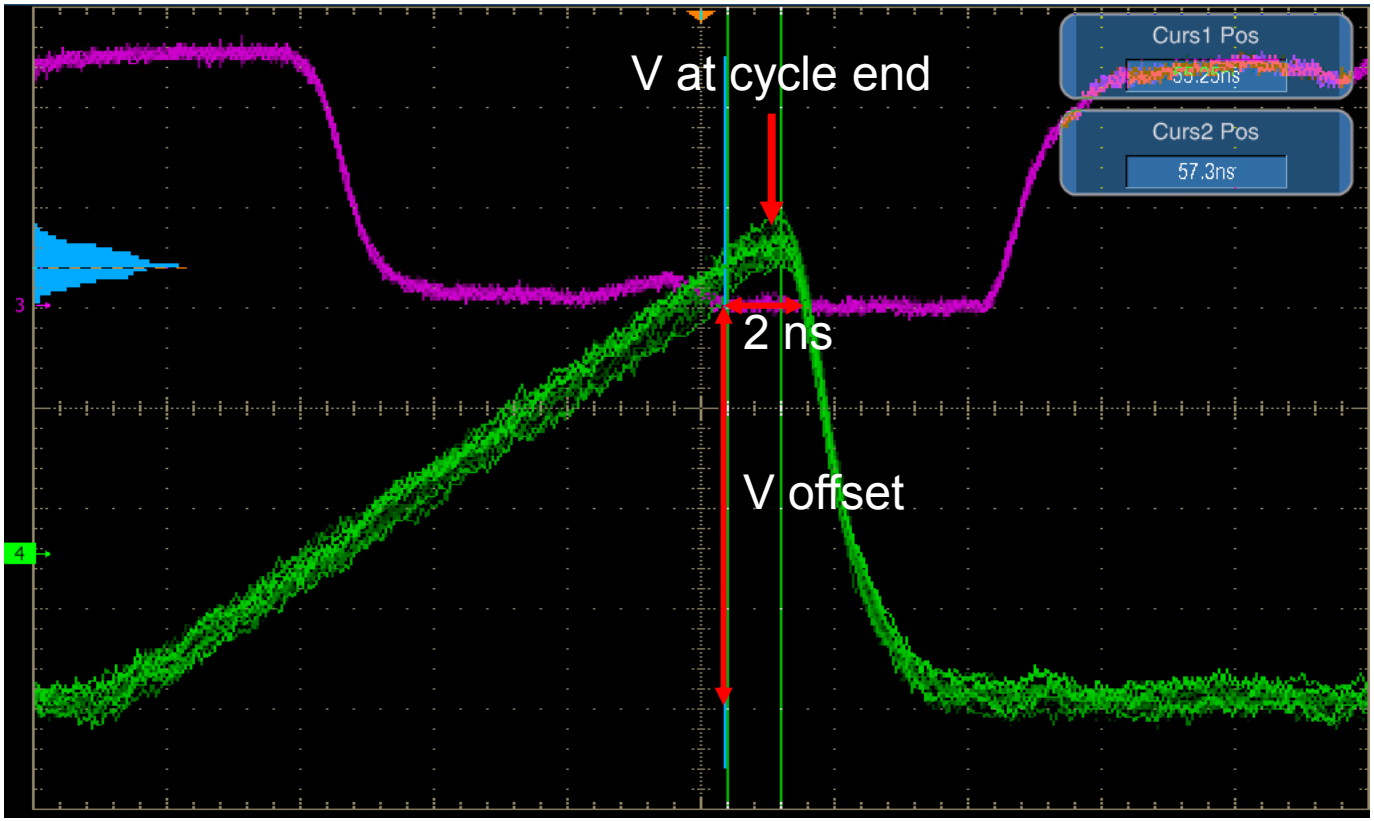


Offset

Offset measurement:

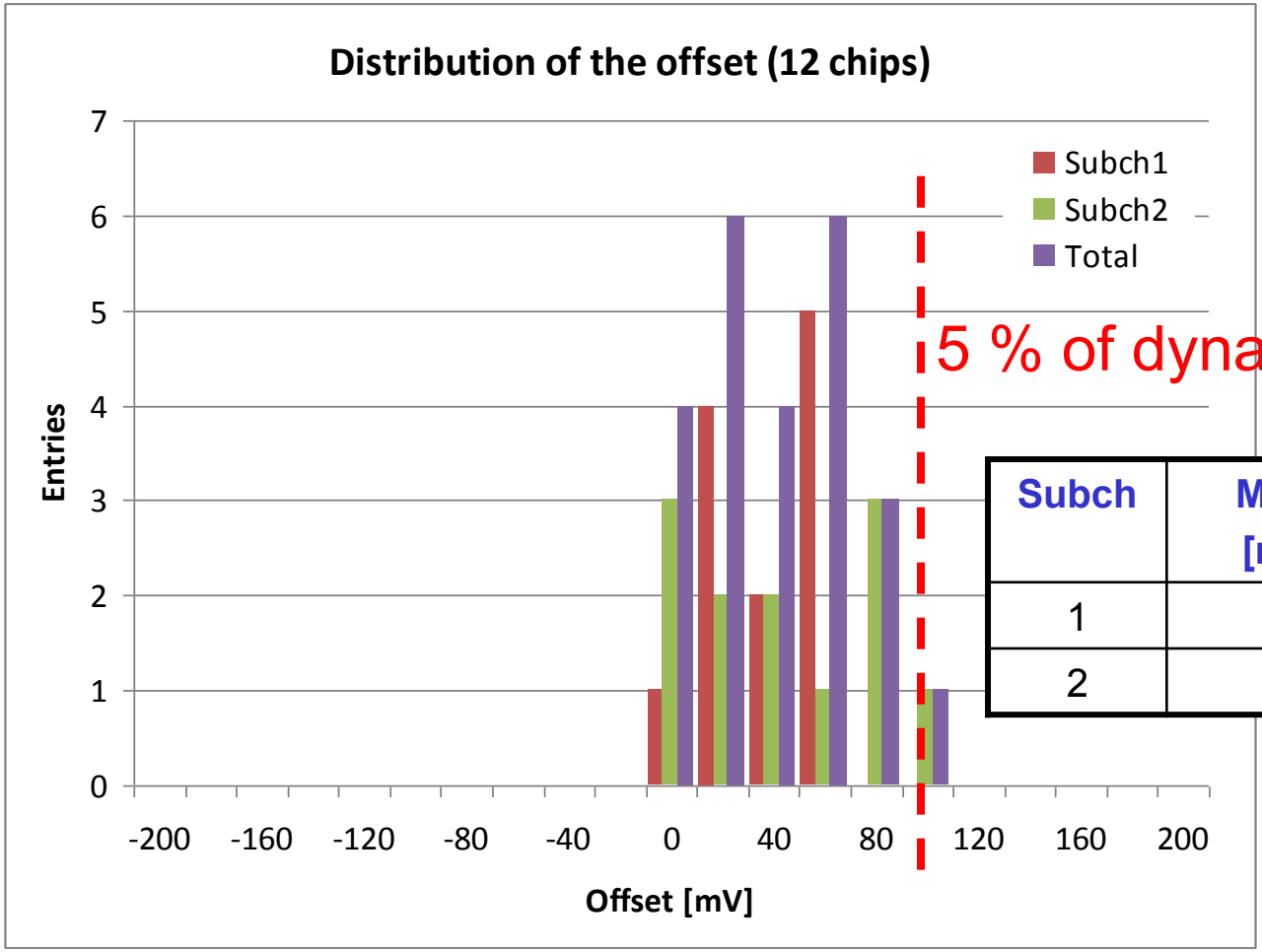
Preamp current offset is integrated

=> Offset at output



Offset

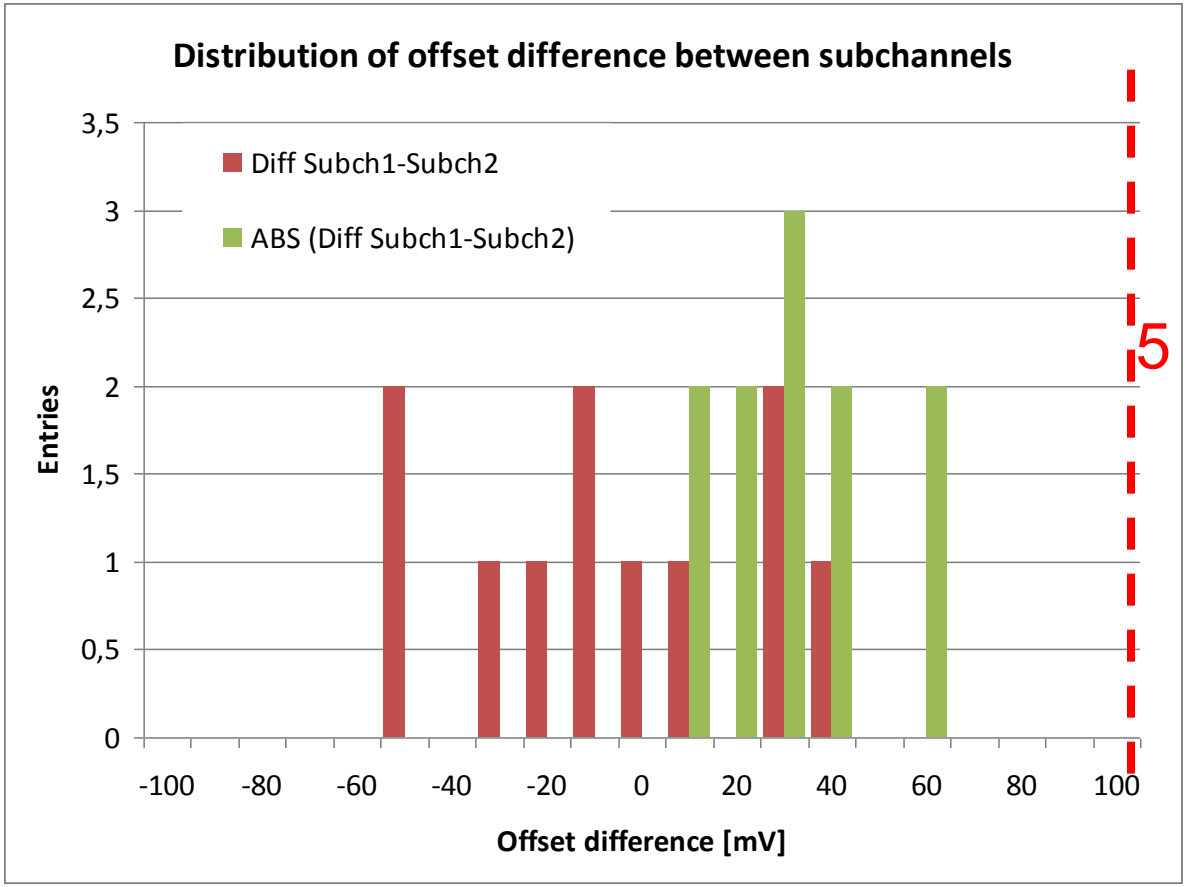
- About 5 % of the full scale range (2 V)
- Slight asymmetry between subchanels (clock)



Subch	Mean [mV]	Std Dev [mV]
1	27	20
2	34	35

Offset

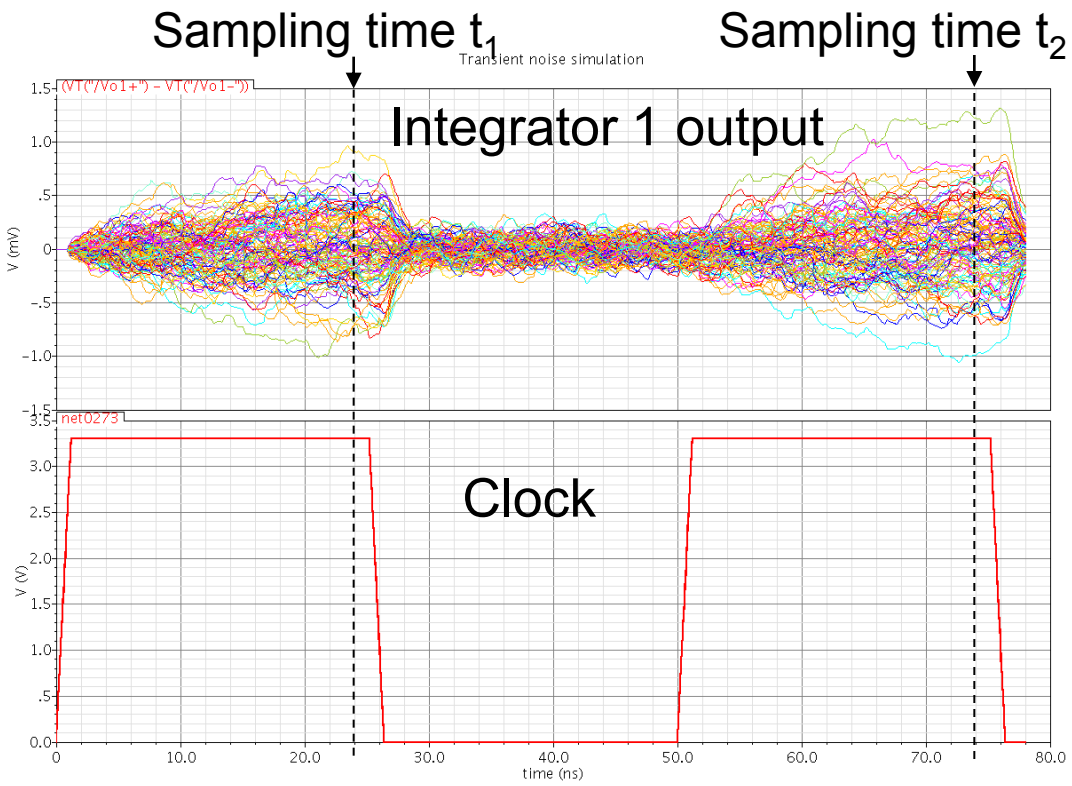
- With AC coupling between ICECAL and ADC what really matters is the difference between the offset of the 2 subchannels
- Well below the 5 % of the full scale range (2 V)

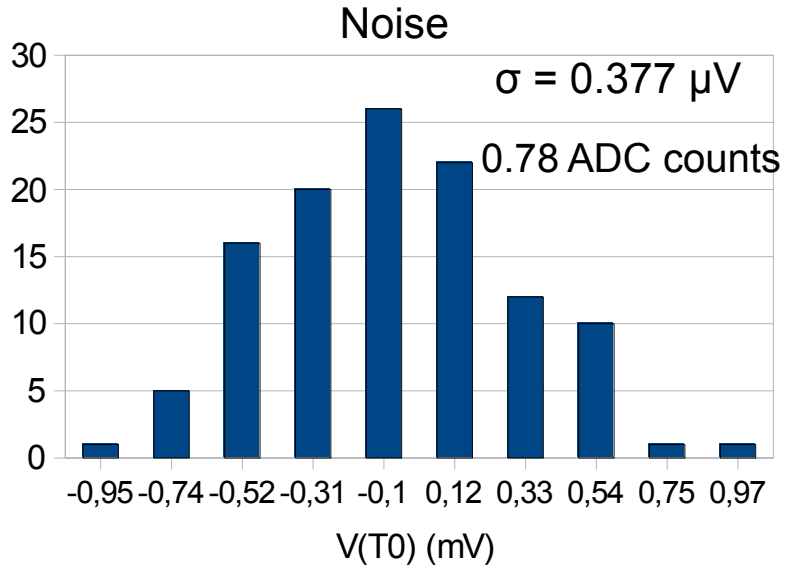


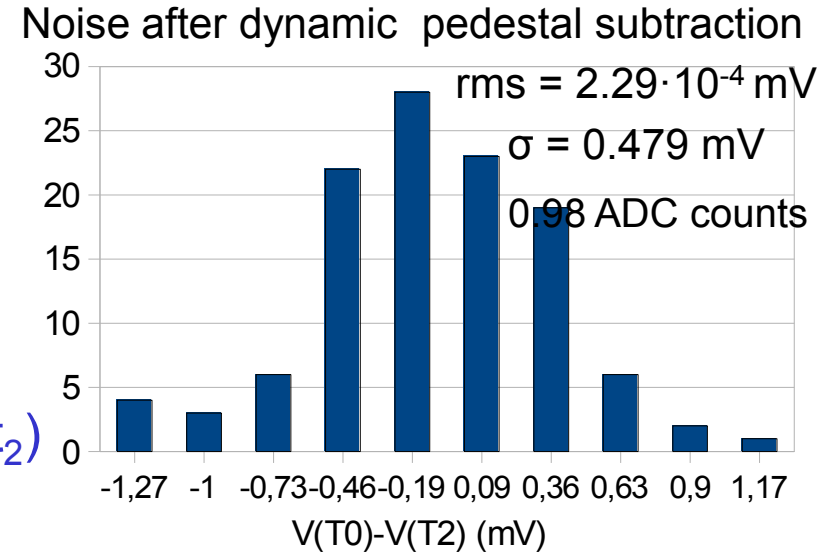
5 % of dynamics

Noise: simulation

- Transient noise analysis



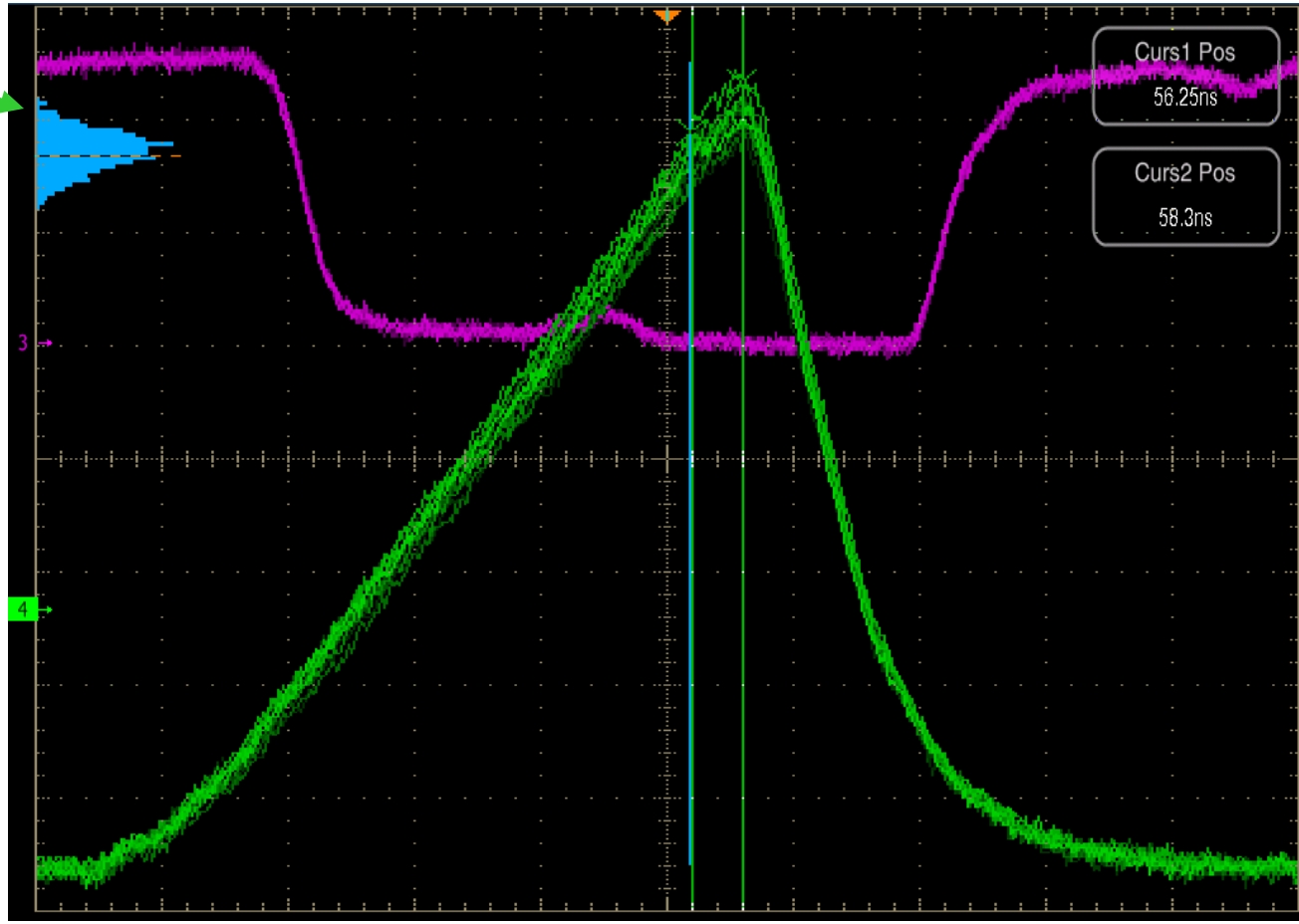




- Correlated noise: distribution of $V(t_2)$
- Uncorrelated noise: distributon of $V(t_1)$- $V(t_2)$

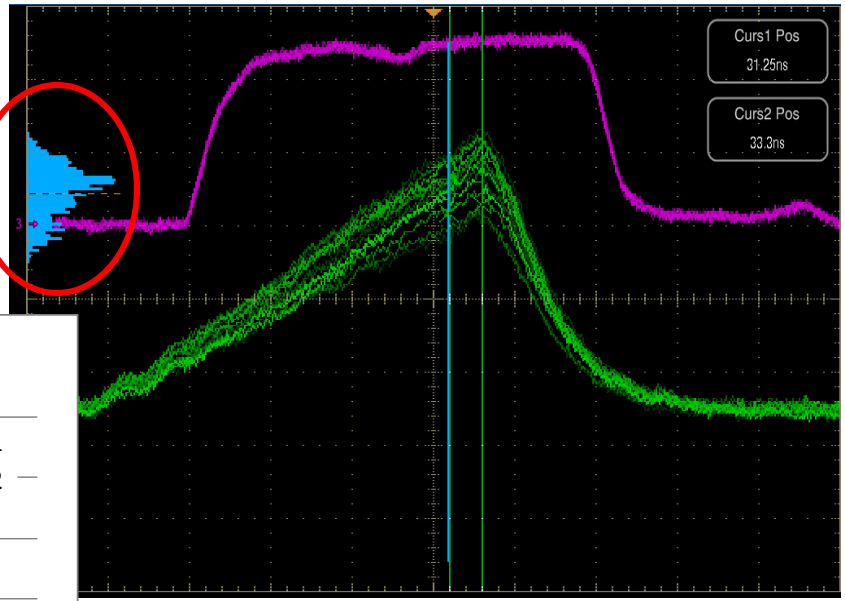
Noise

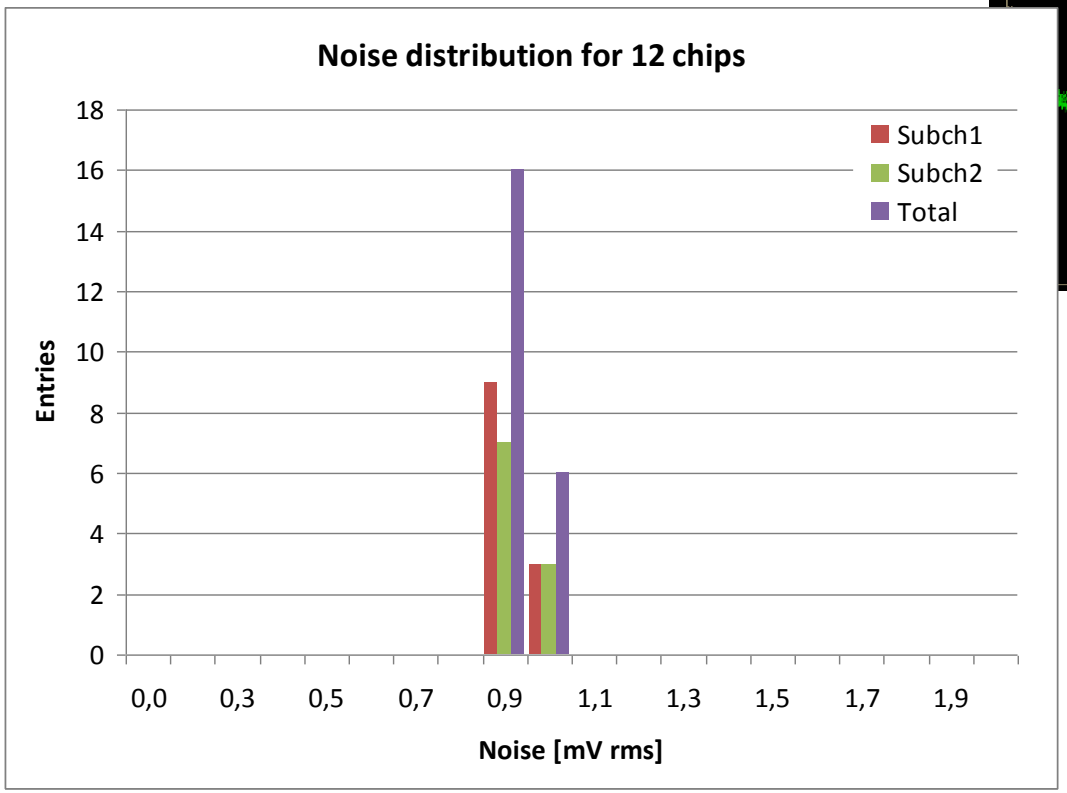
- The noise:
  - Generate a histogram of the voltage value by the end of the cycle.
  - Gaussian fit => standard deviation
- Noise is dominated by the differential probe at the ASIC output => use an amplifier of gain 10.



Noise

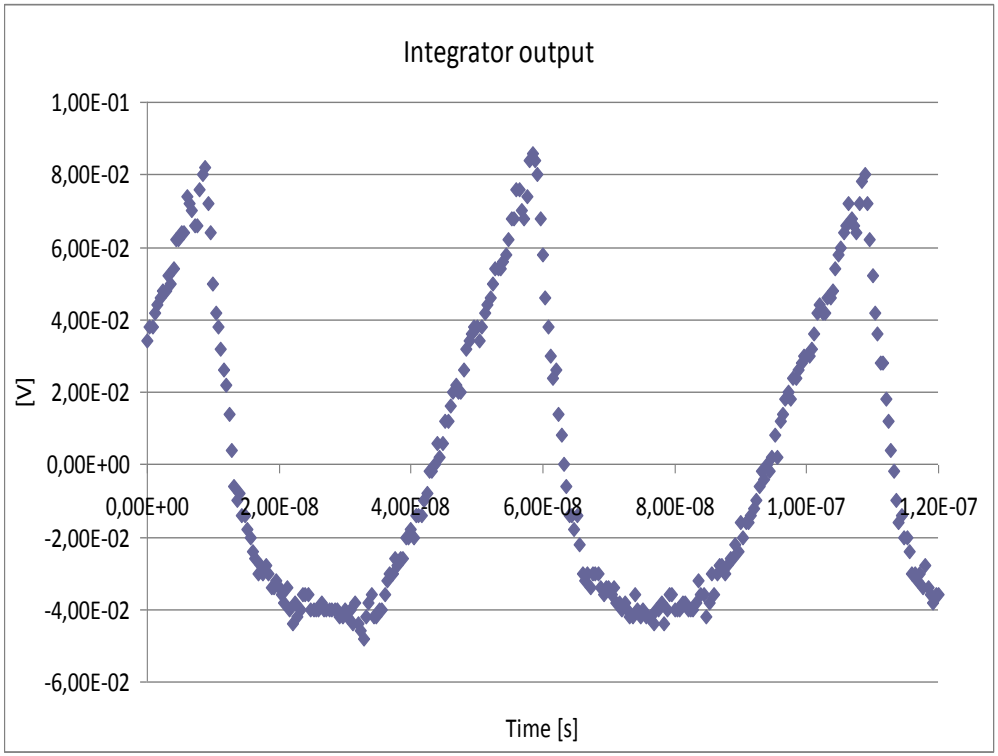
- Average noise is about 1.8 ADC counts, higher than expected
- Histogram is not fully Gaussian:
- Noise pick-up:
  - Depends on chip connection (socket)

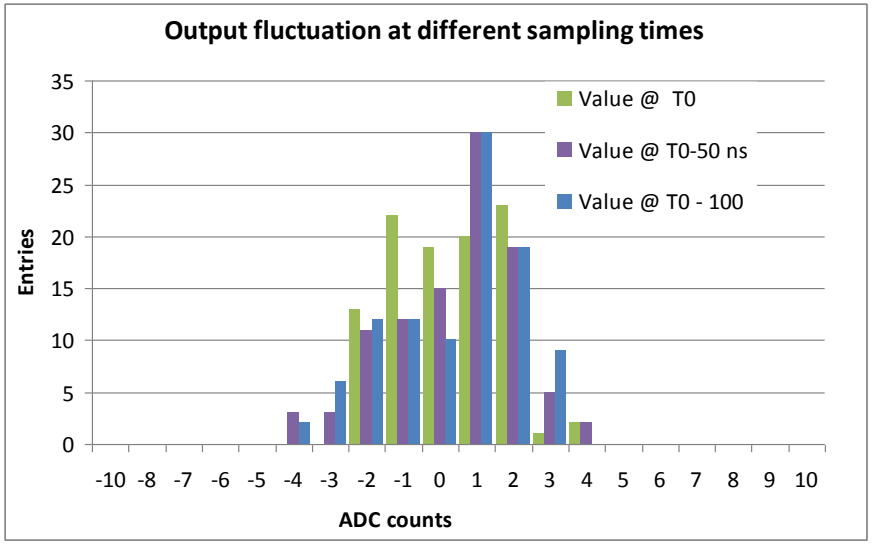




Noise

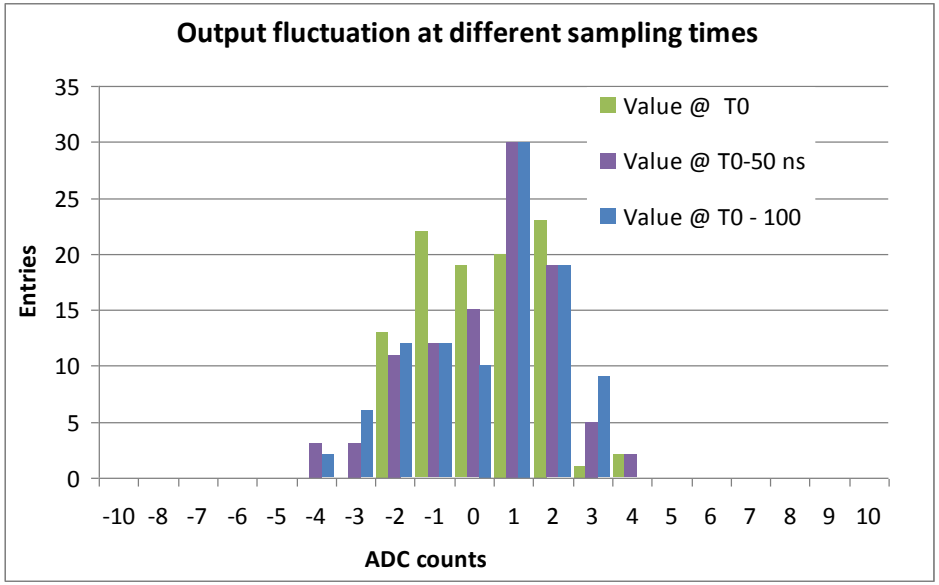
- Alternative method: acquire 100 waveforms and make histogram

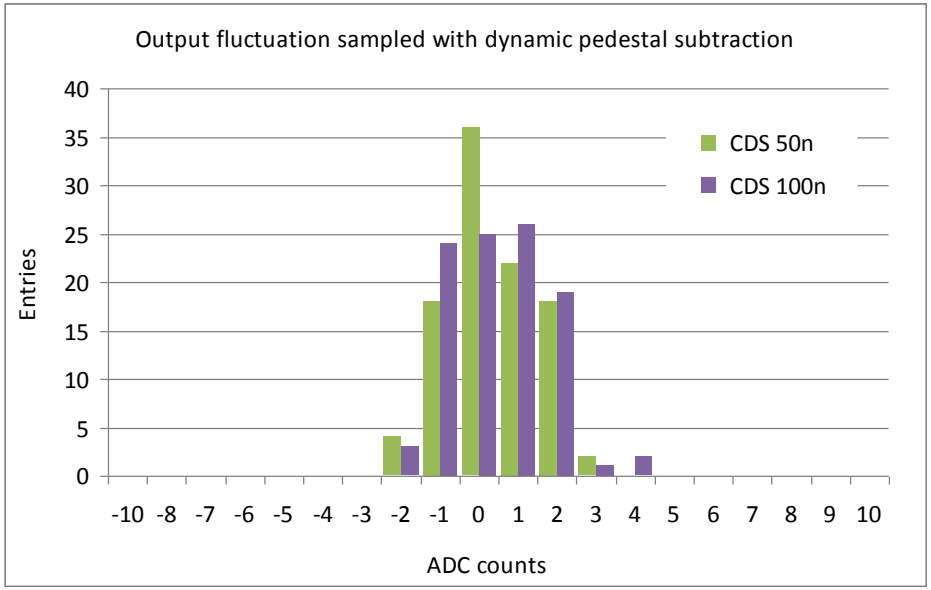




Noise

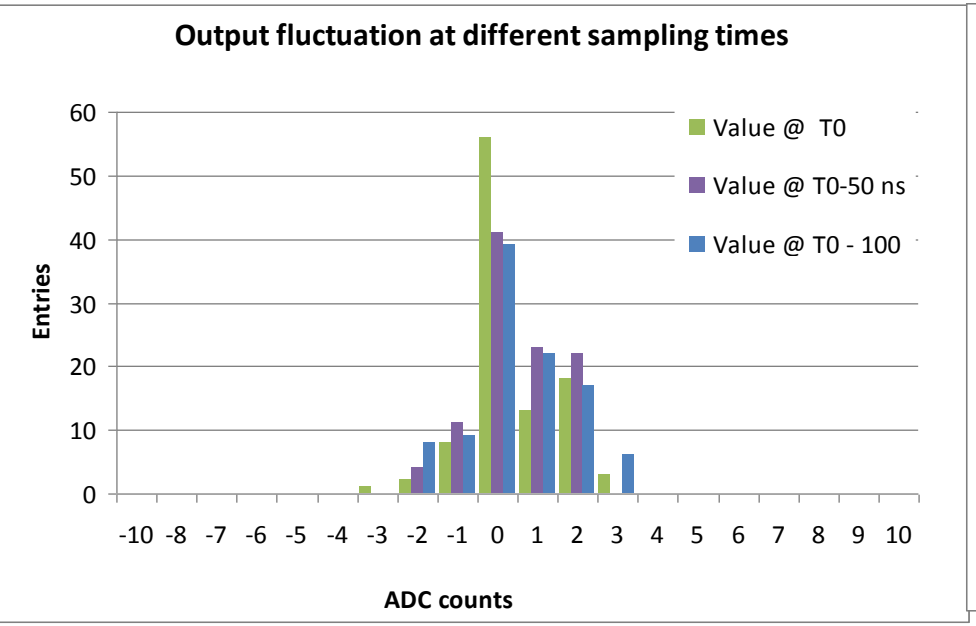
- Alternative method: acquire 100 waveforms and make histogram
- Study effect of correlated sampling CDS (dynamic pedestal subtraction)
  - Typically noise improves after CDS
    - CDS increases uncorrelated noise (HF)
    - CDS attenuates LF noise
  - That confirms the presence of pick-up noise
  - After CDS noise is about 1.2 ADC counts (close to simulation:1 ADC count)

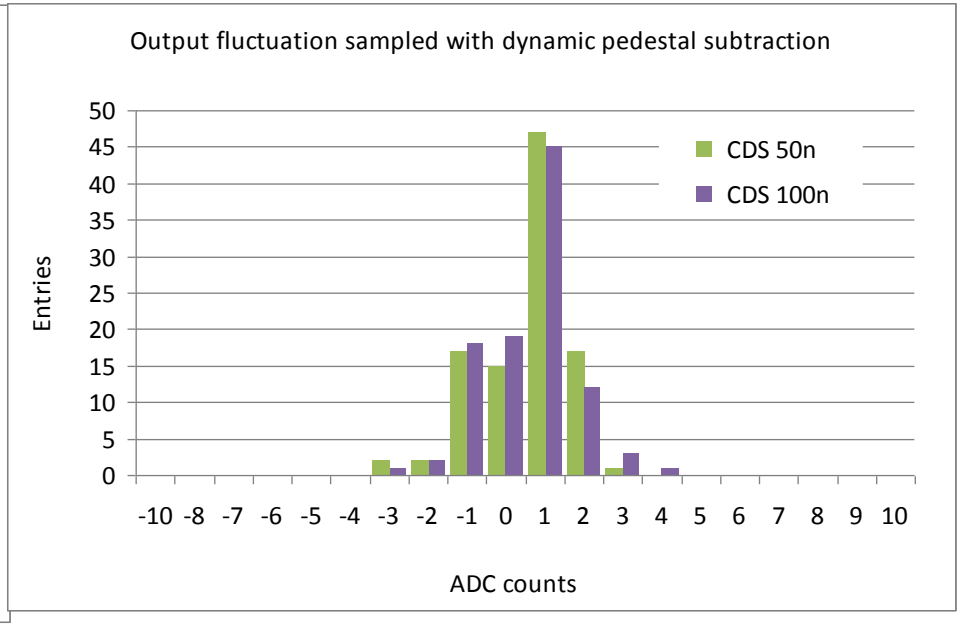




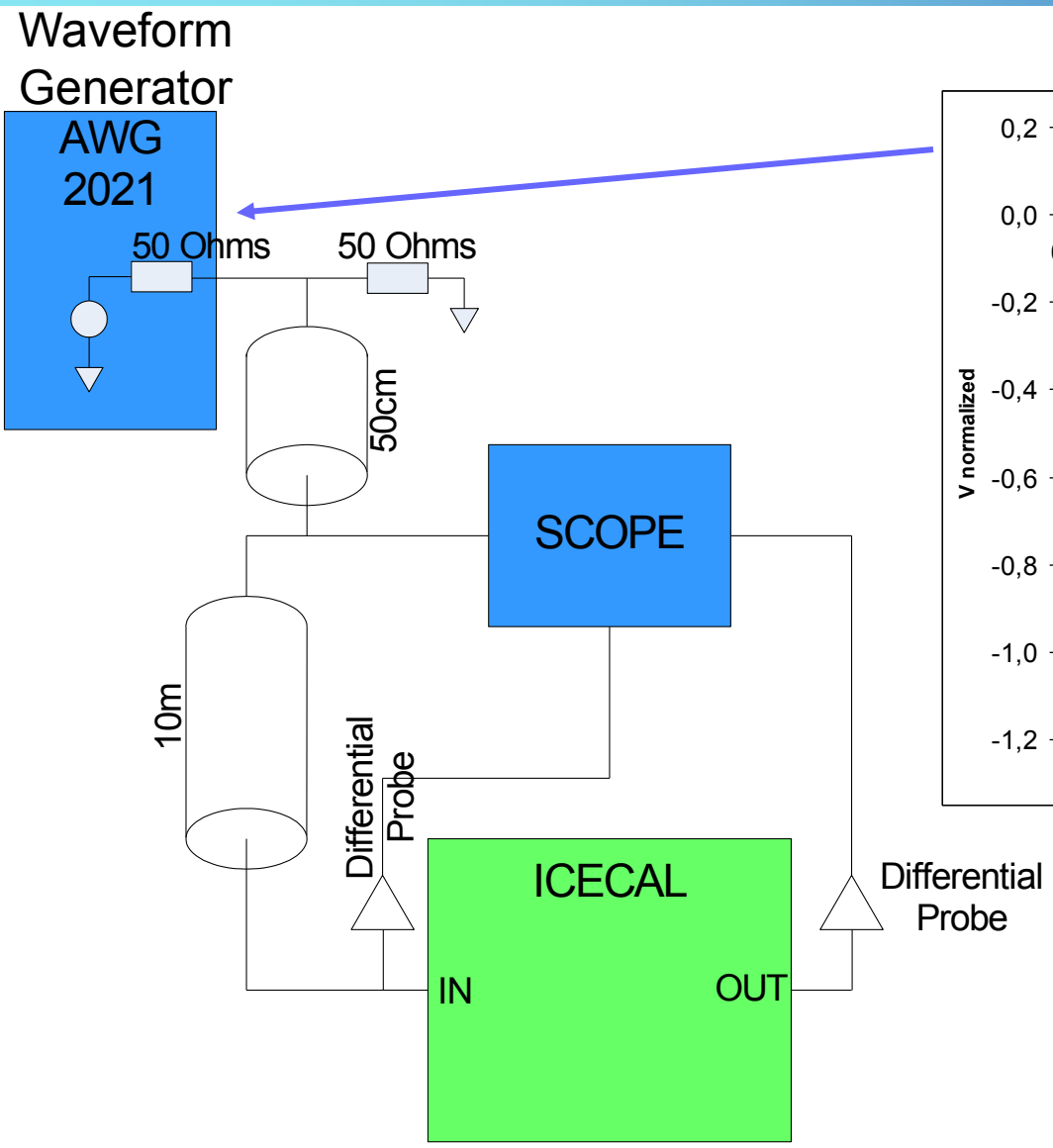
Noise

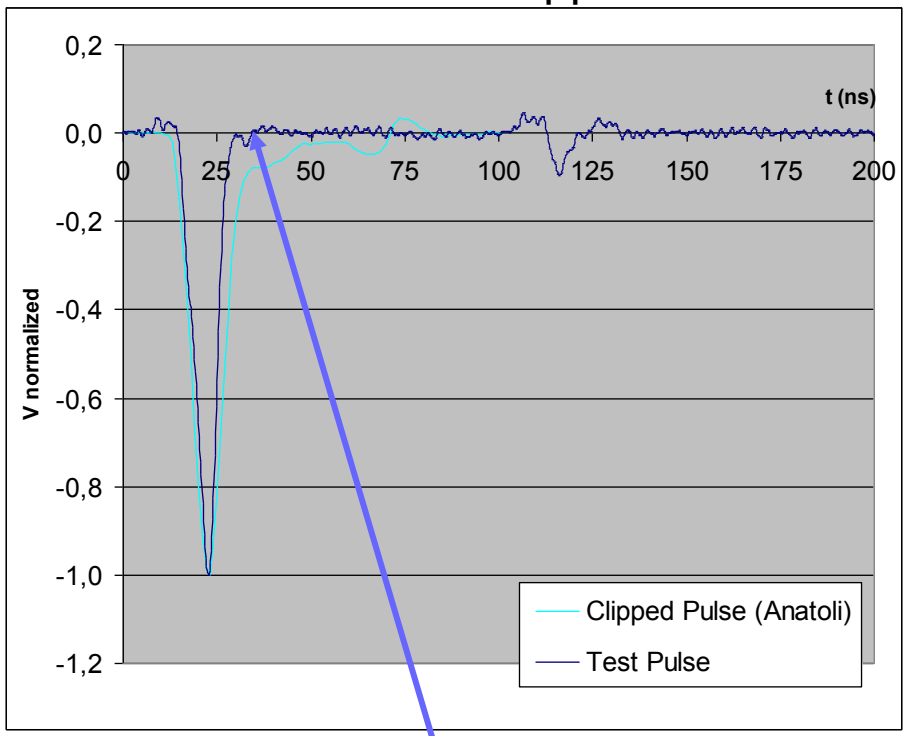
- On very few cases noise after CDS is higher
  - 1.1 ADC counts before CDS
  - 1.2 ADC counts after CDS
- That means that pick up noise and the increase of uncorrelated noise by CDS are comparable





Input impedance

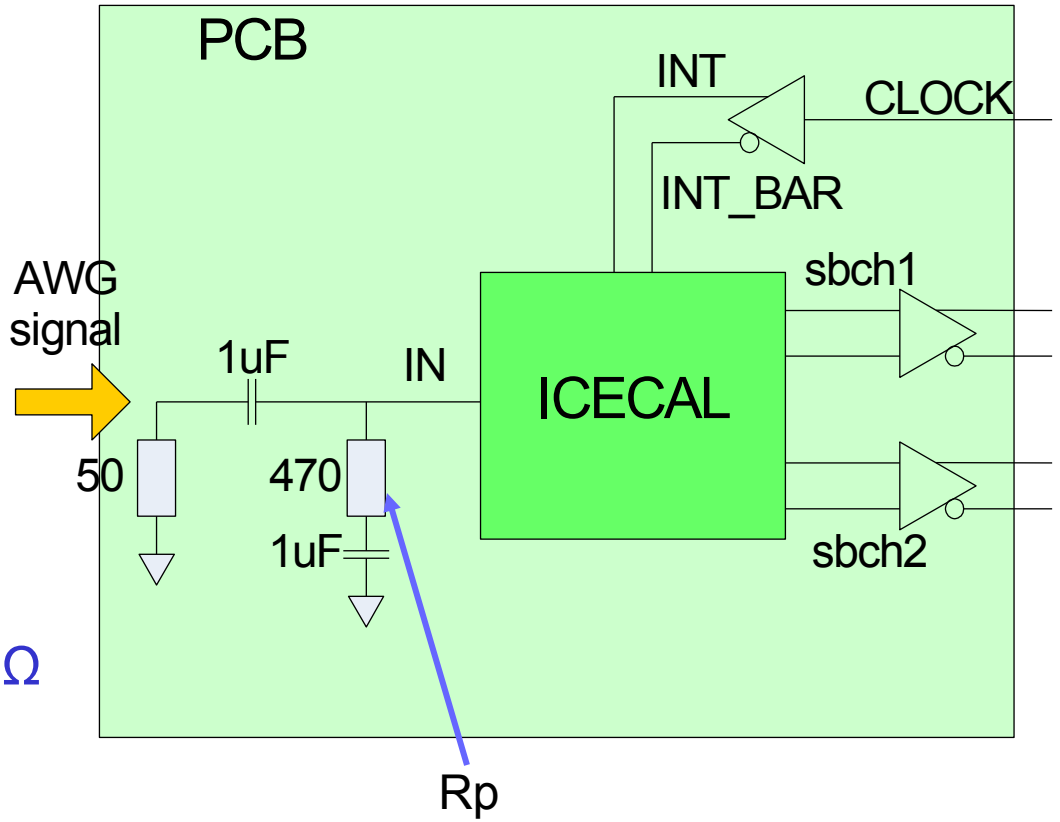




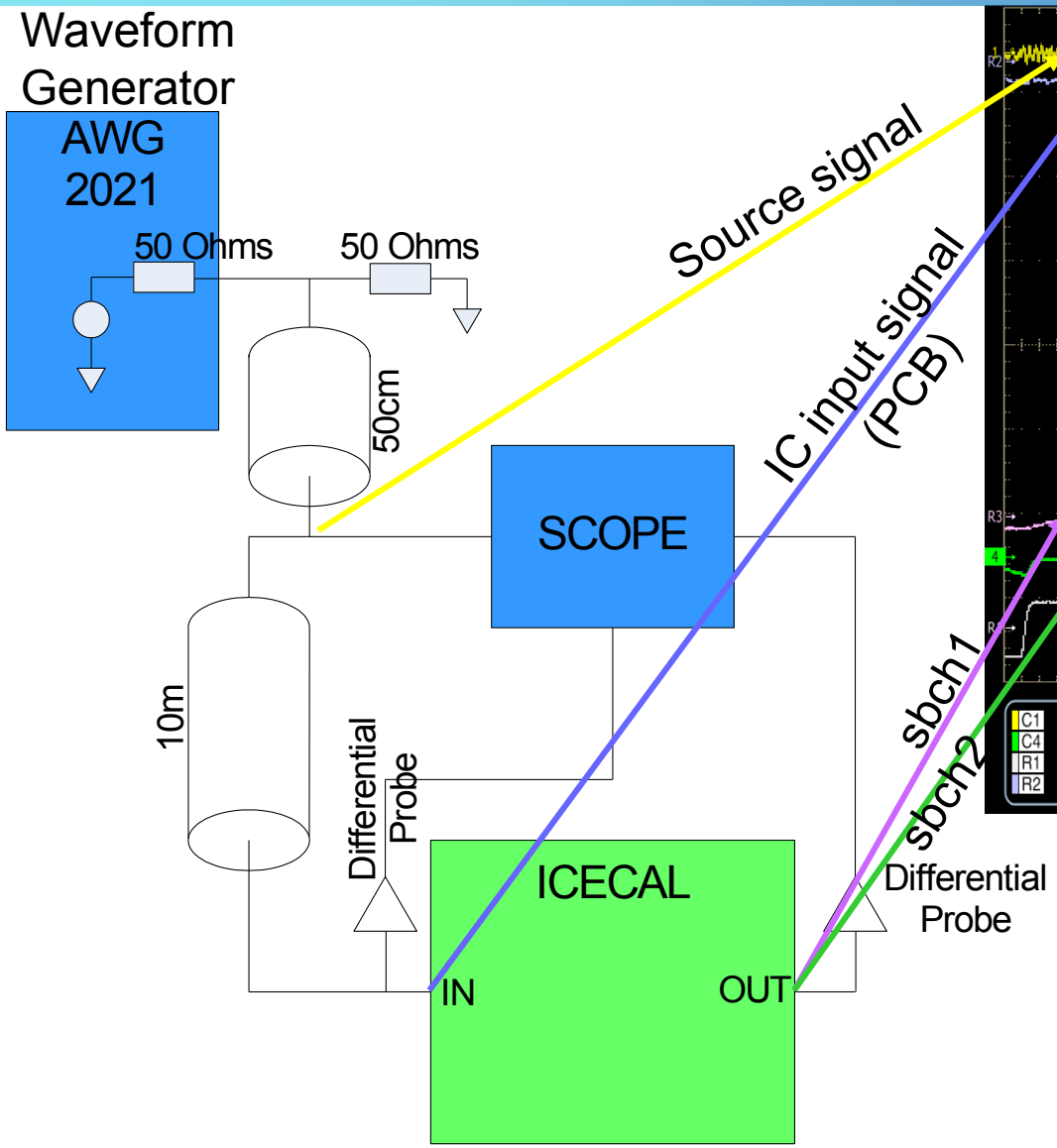
Fast pulse (no tail) to measure reflections

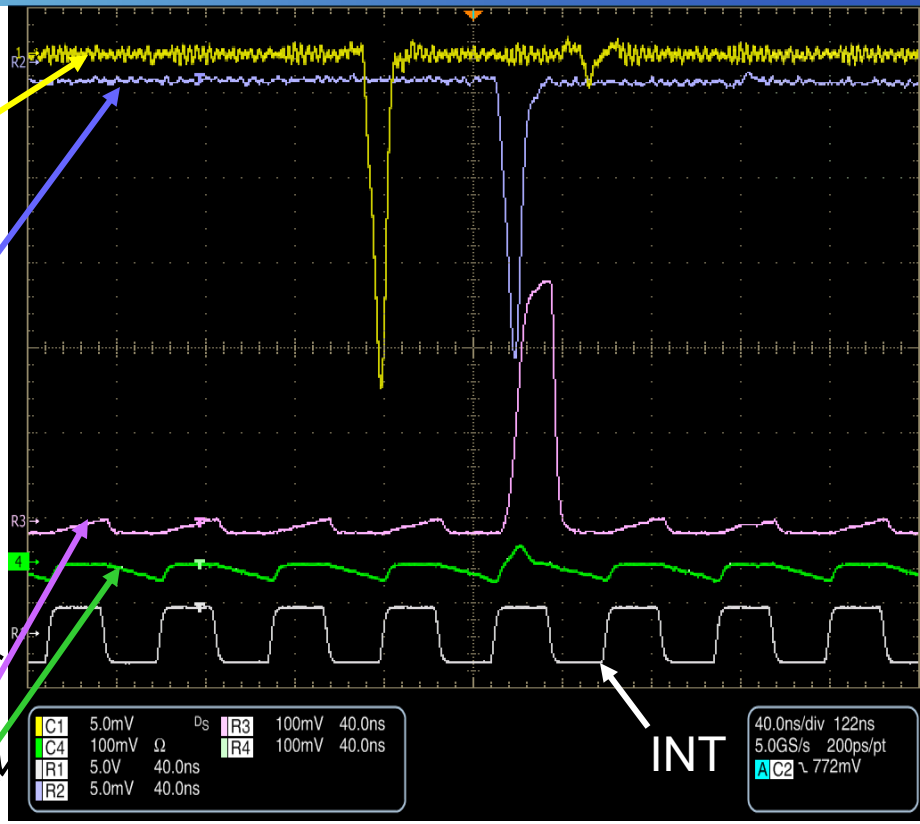
Input impedance

- PCB input circuit:
  - AC coupling
  - Rpar:
    - Zin a little higher than 50Ω
    - Rp used to fine tune Zin

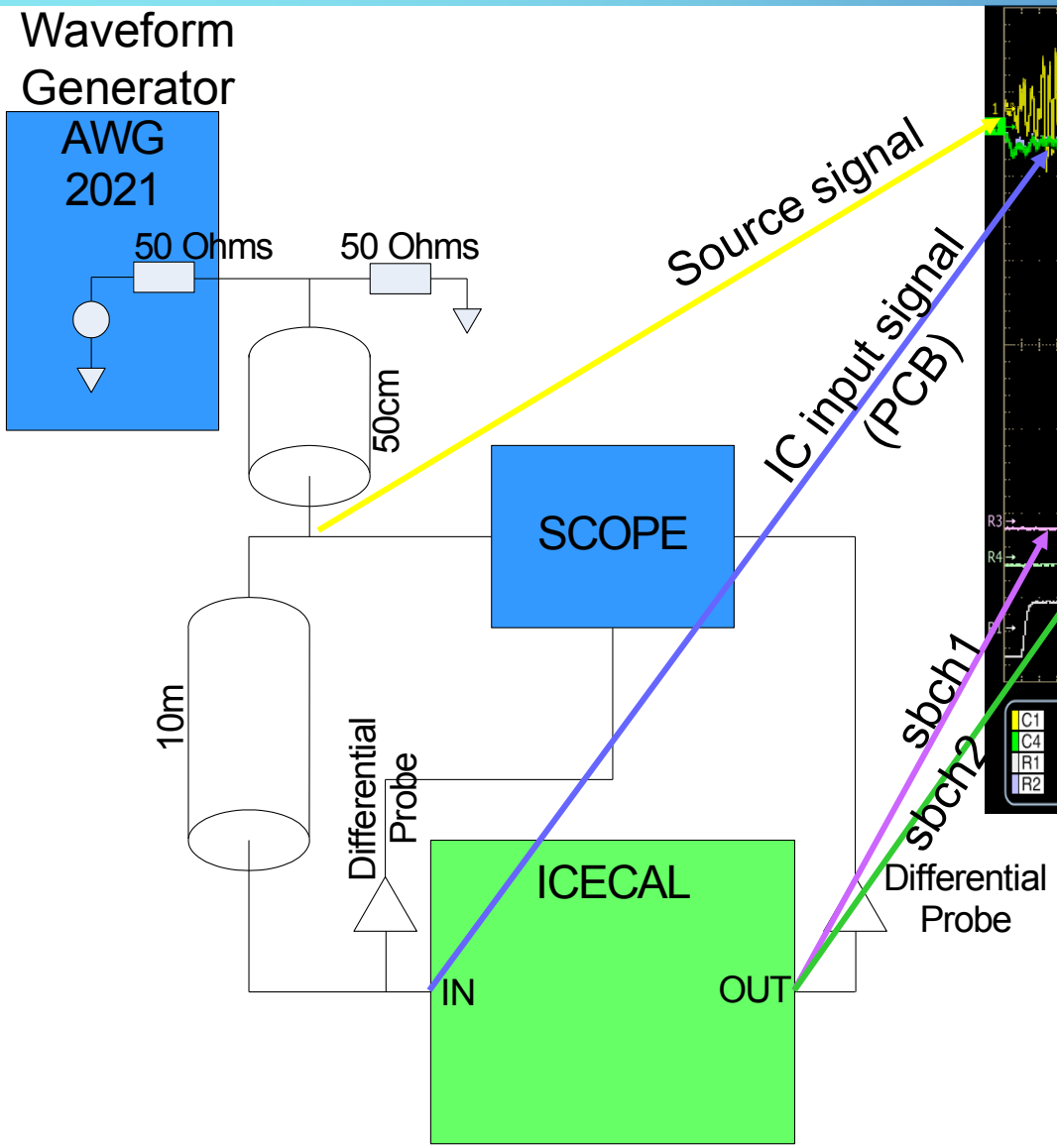


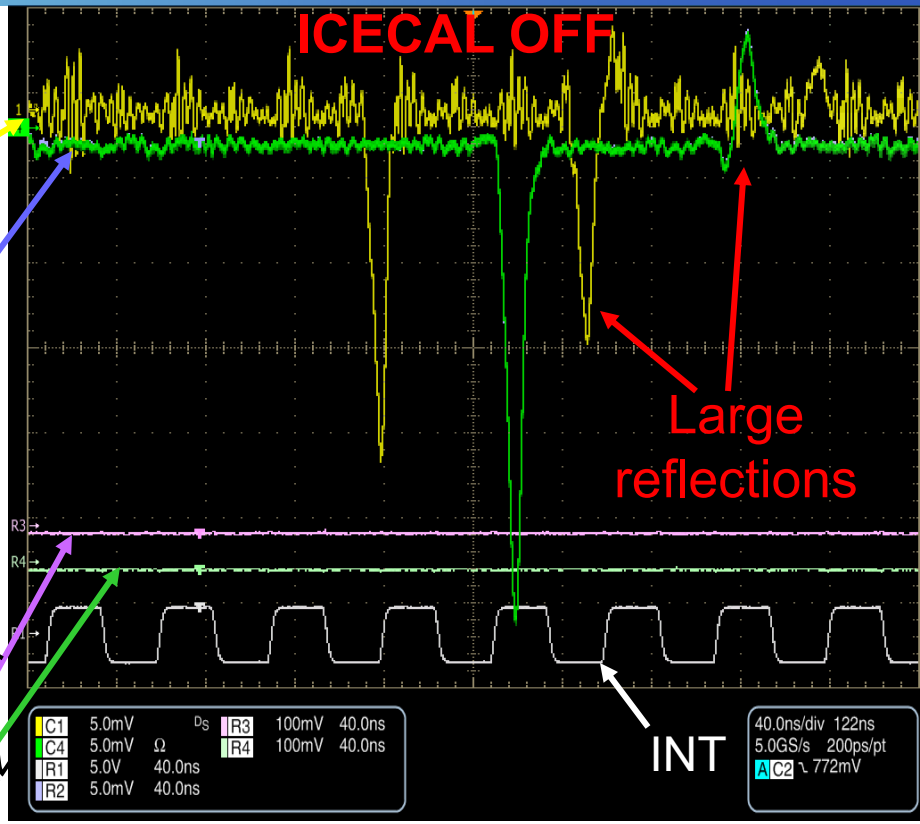
Input impedance





Input impedance





Input impedance

Reflection coefficients

Source (AWG)

IC input (PCB)

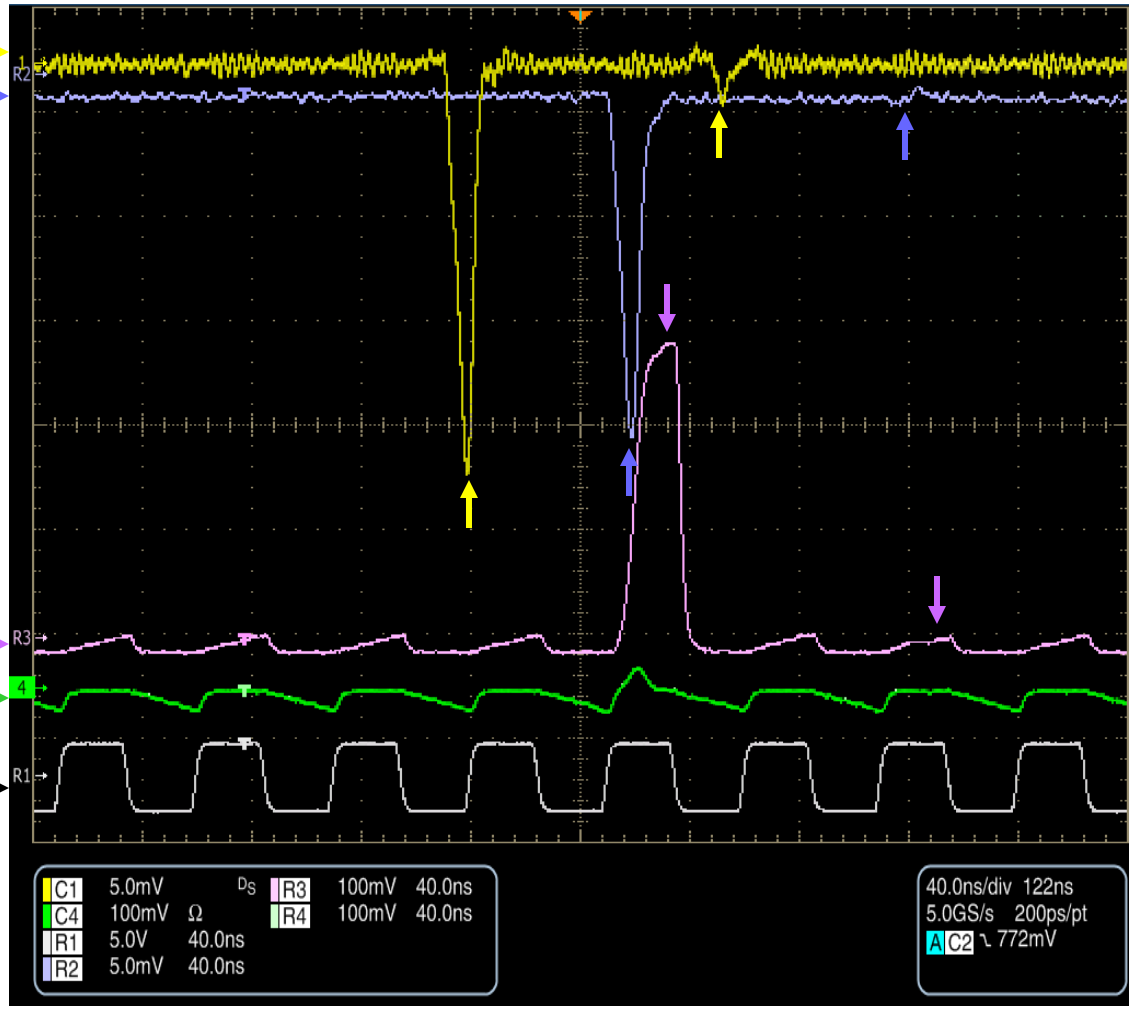
Reflection Coefficients for source, IC input, and output signals.

Refl. Coeff. = 1st pulse integral / 2nd pulse integral

Out sbch1

Out sbch2

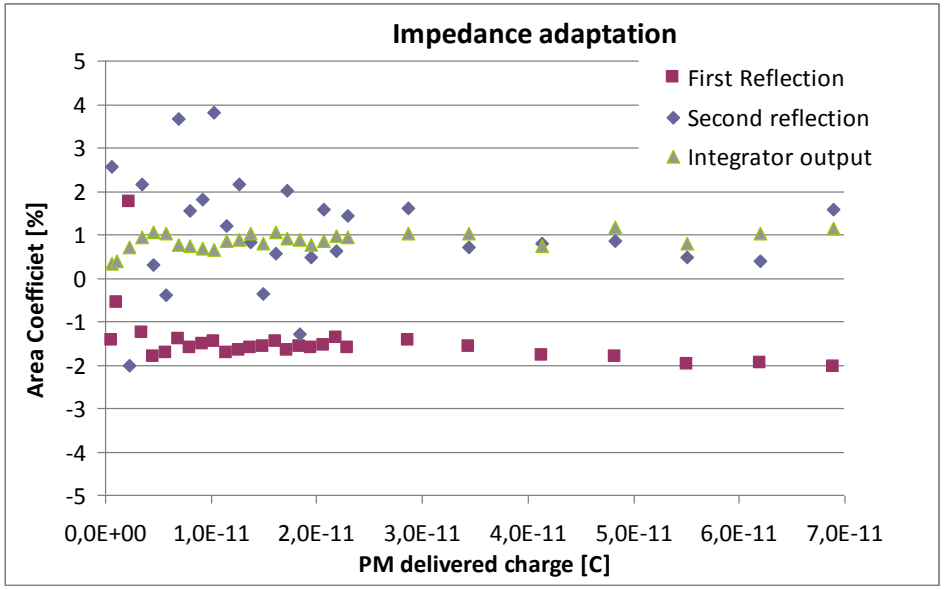
INT



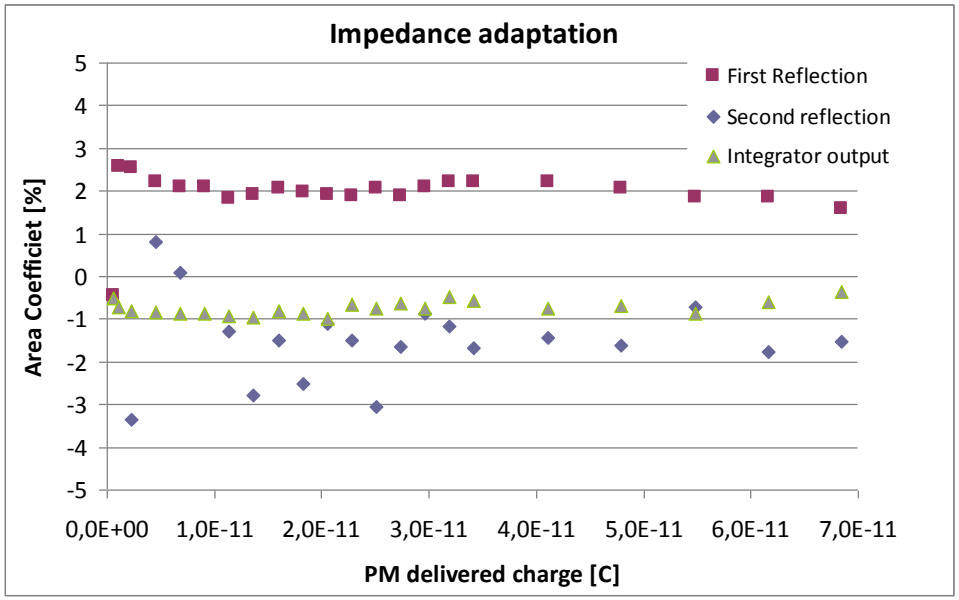
Input impedance

- Optimal Rp is between 360 and 390 ohm
- Dynamic variation of input impedance is << 1 % for full dynamic (50 pC)
- Measurement error for second reflection is quite high for low amplitudes
  - Noise of the differential probe

Rp = 360 Ohm

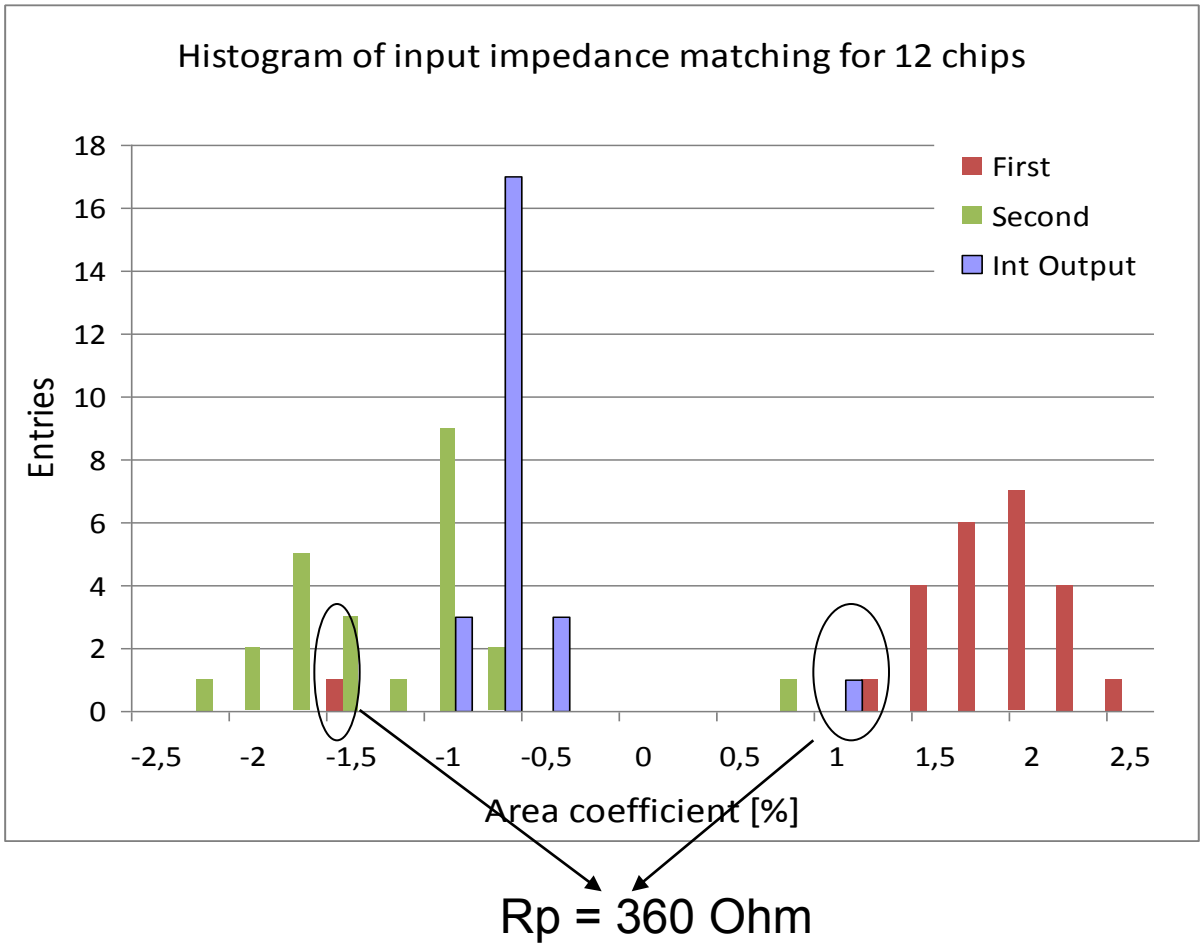


Rp = 390 Ohm



Input impedance (12 chip statistics: new!)

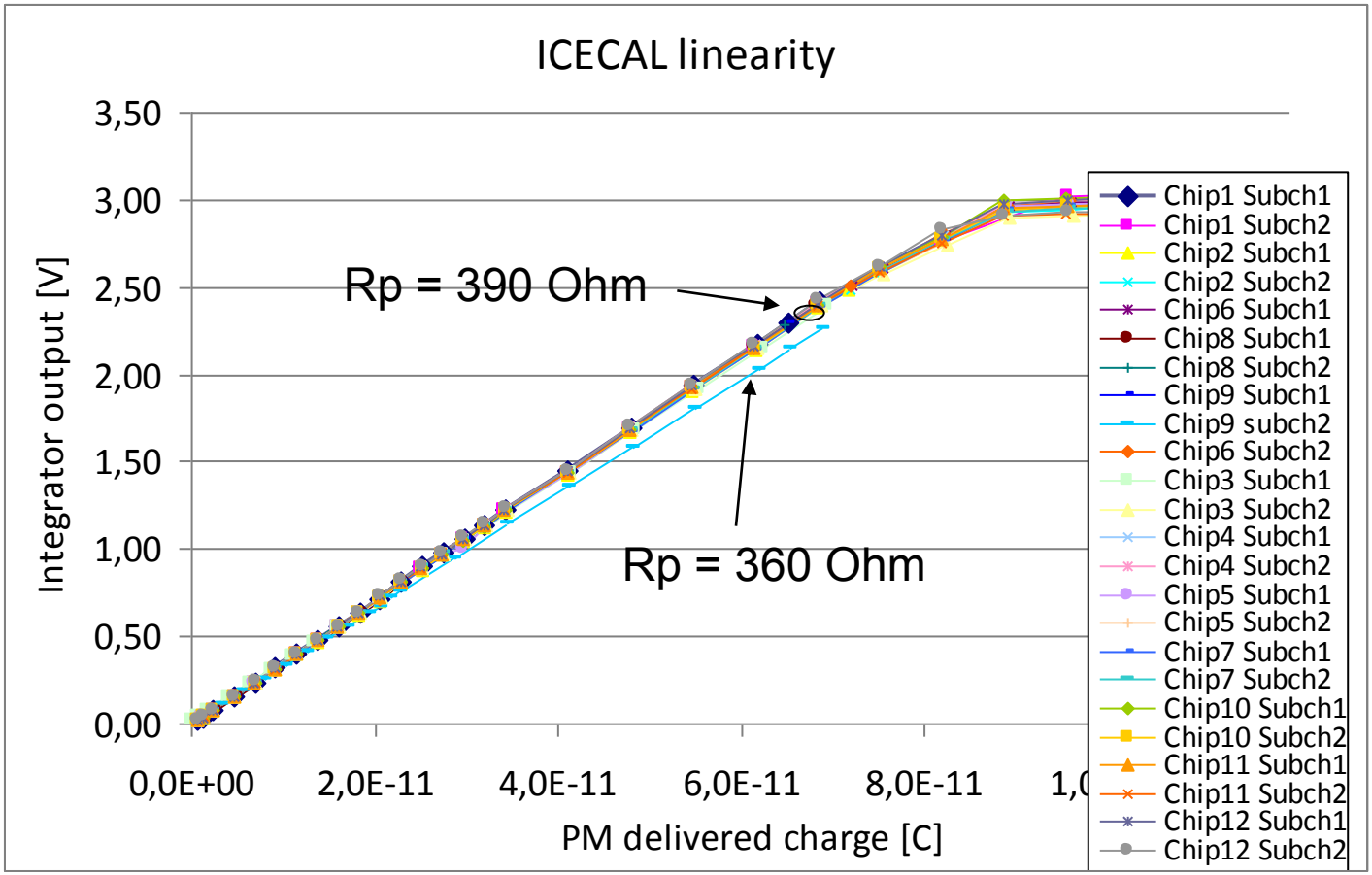
- Dispersion is low: < 0.5 %
  - Only 5 chips have been measured



	Mean [%]	Std Dev [%]
First	1,99	0,21
Second	-1,75	0,43
Int output	-0,82	0,11

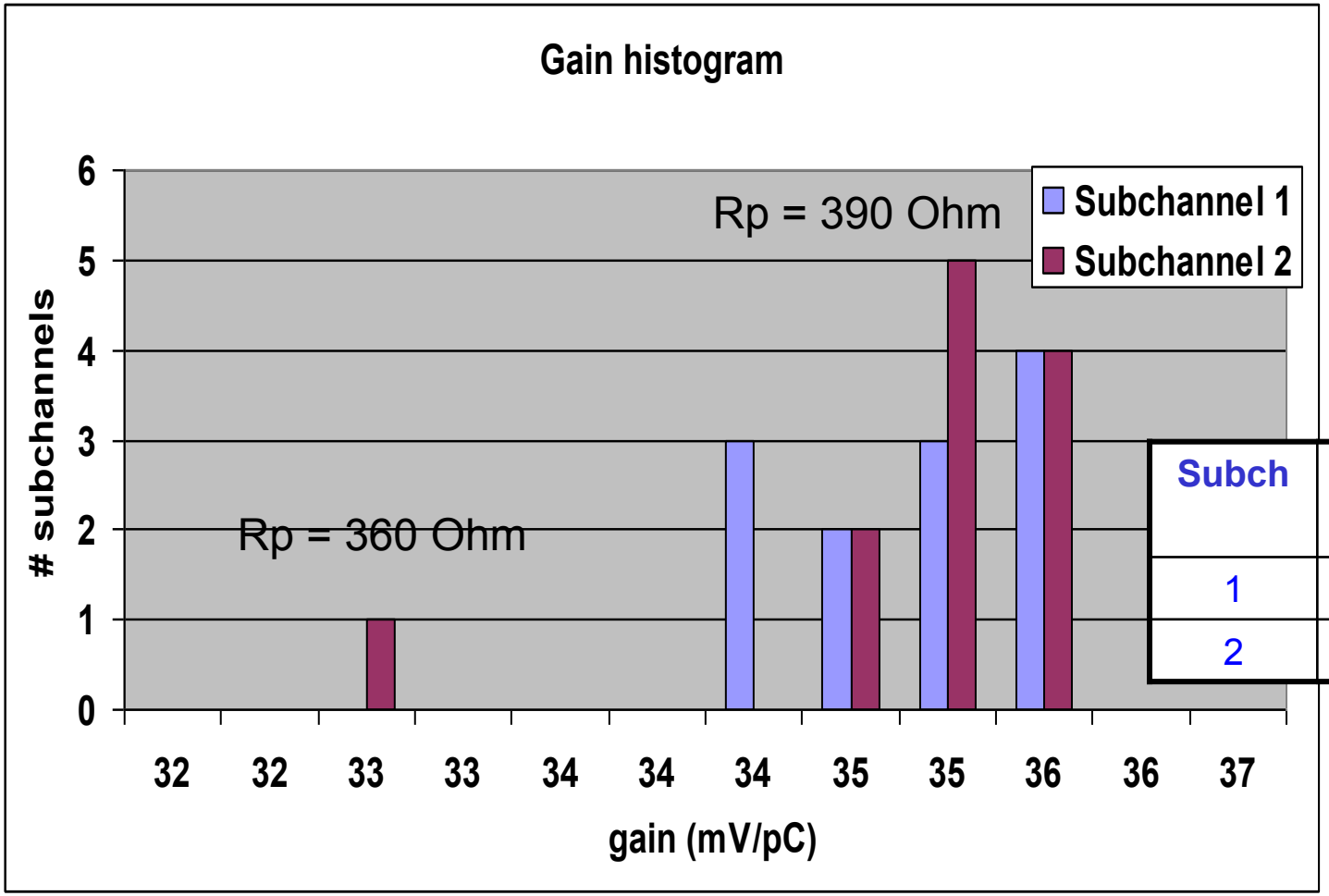
Linearity (12 chip statistics: new!)

- Dynamic range is ok (50 pC required)
- Rp (input impedance) affects the amount of charge sensed by the ASIC
  - Rp 360 Ohm: negative reflection coefficient: lower amplitude @ ICECAL input
  - Rp 390 Ohm: positive reflection coefficient: higher amplitude @ ICECAL input



Linearity (12 chip statistics: new!)

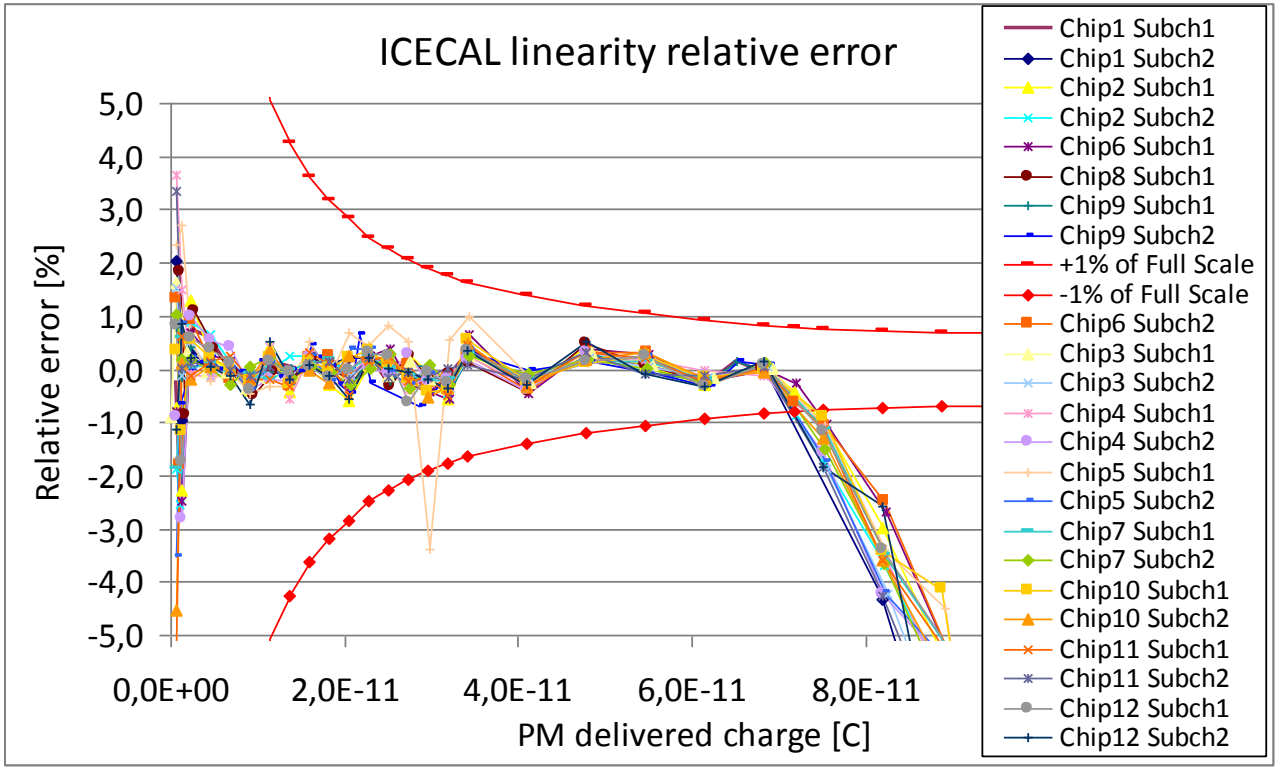
- Slight sistematic difference between subchannels (clock) ?



Subch	Mean [mV/pC]	Std Dev [mV/pC]
1	34,84	0,41
2	35,13	0,32

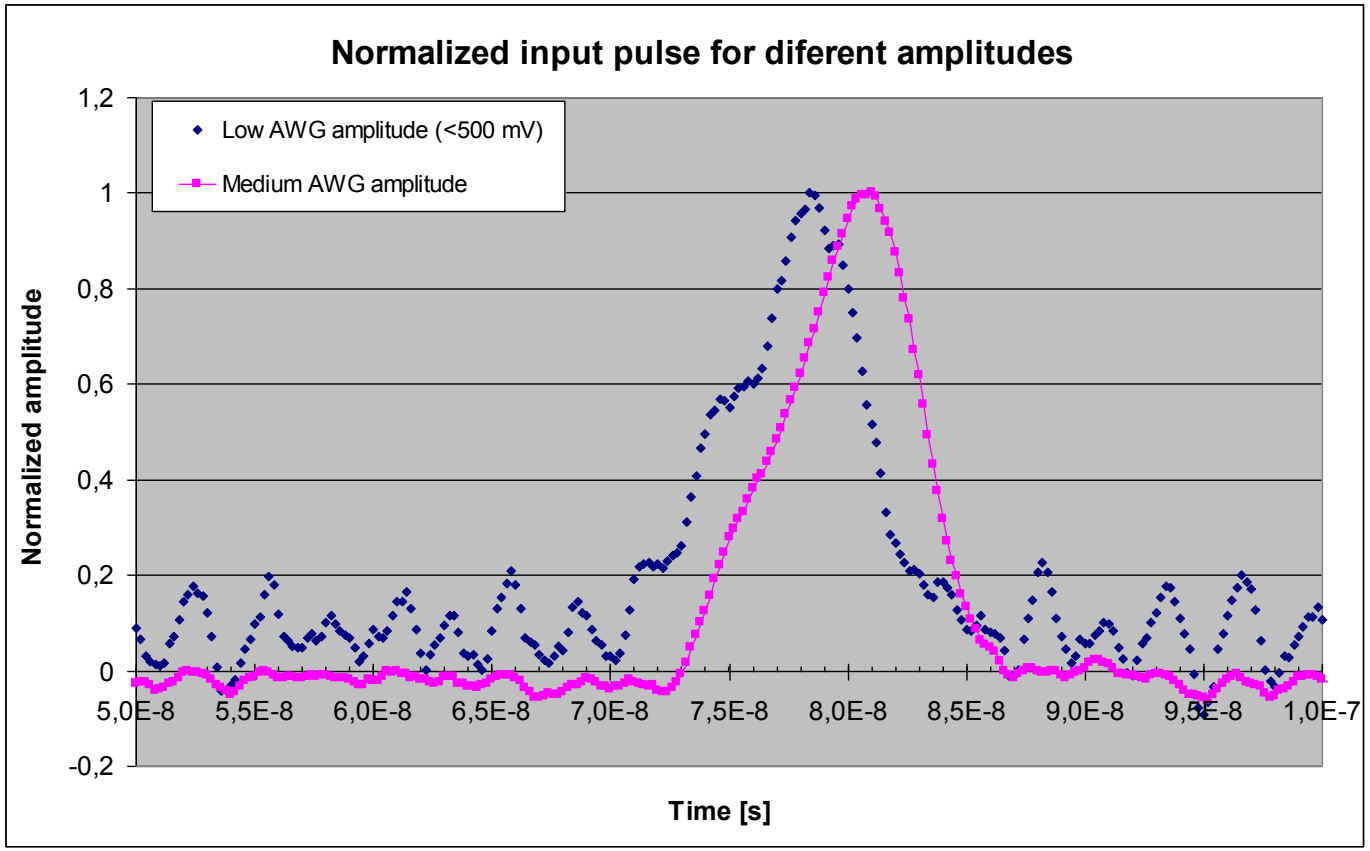
Linearity (12 chip statistics: new!)

- Relative linearity error is below 1% for the full range (50 pC)
- Very difficult calibration of the measurement system:
  - Scope vertical scale and attenuation of the probe
  - Cross-check using calibrated attenuators
- Problems with very low amplitudes: see next slides
  - Still well below 1 % of the Full Scale



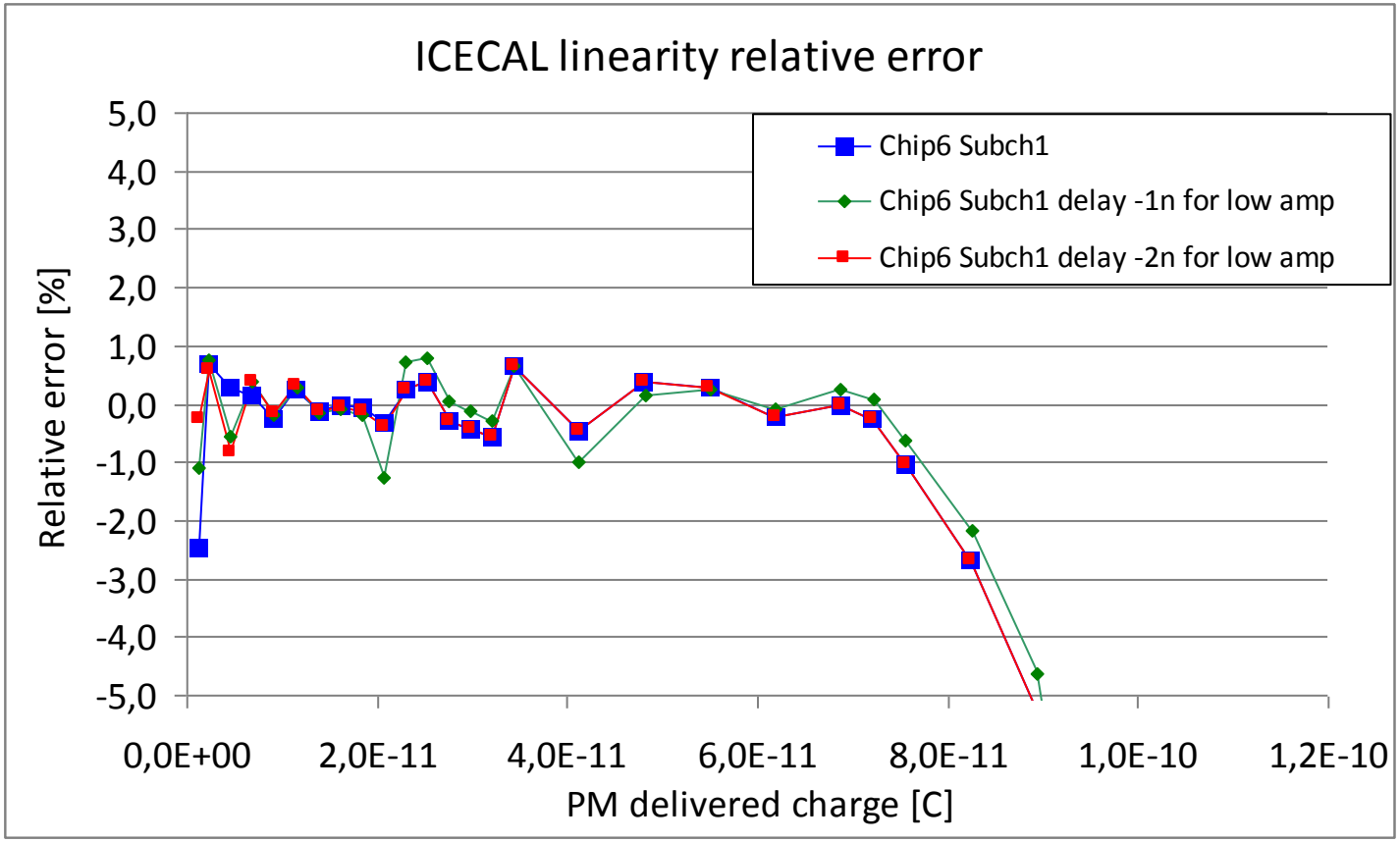
Linearity

- What happens at low amplitudes?
- Problem with AWG generator:
  - Different signal delay as fucntion of the amplitude (advanced for low amp)
  - Again, it can be bypassed using calibrated attenuators



Linearity

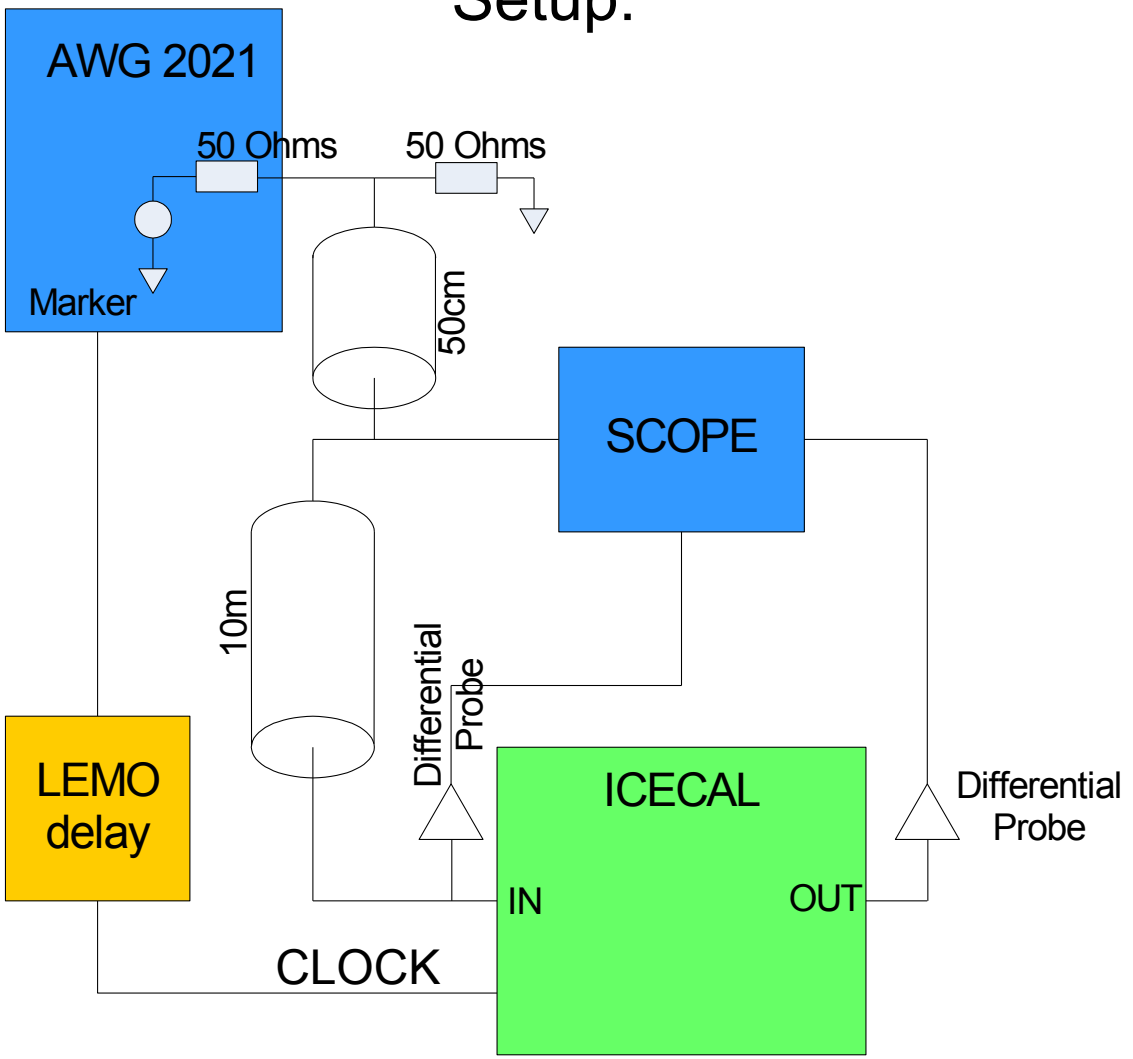
- Adding some delay for low AWG amplitudes corrects the problem
- In that case, relative linearity error is well below 1 % even for low amplitudes



Flatness at the integrator output

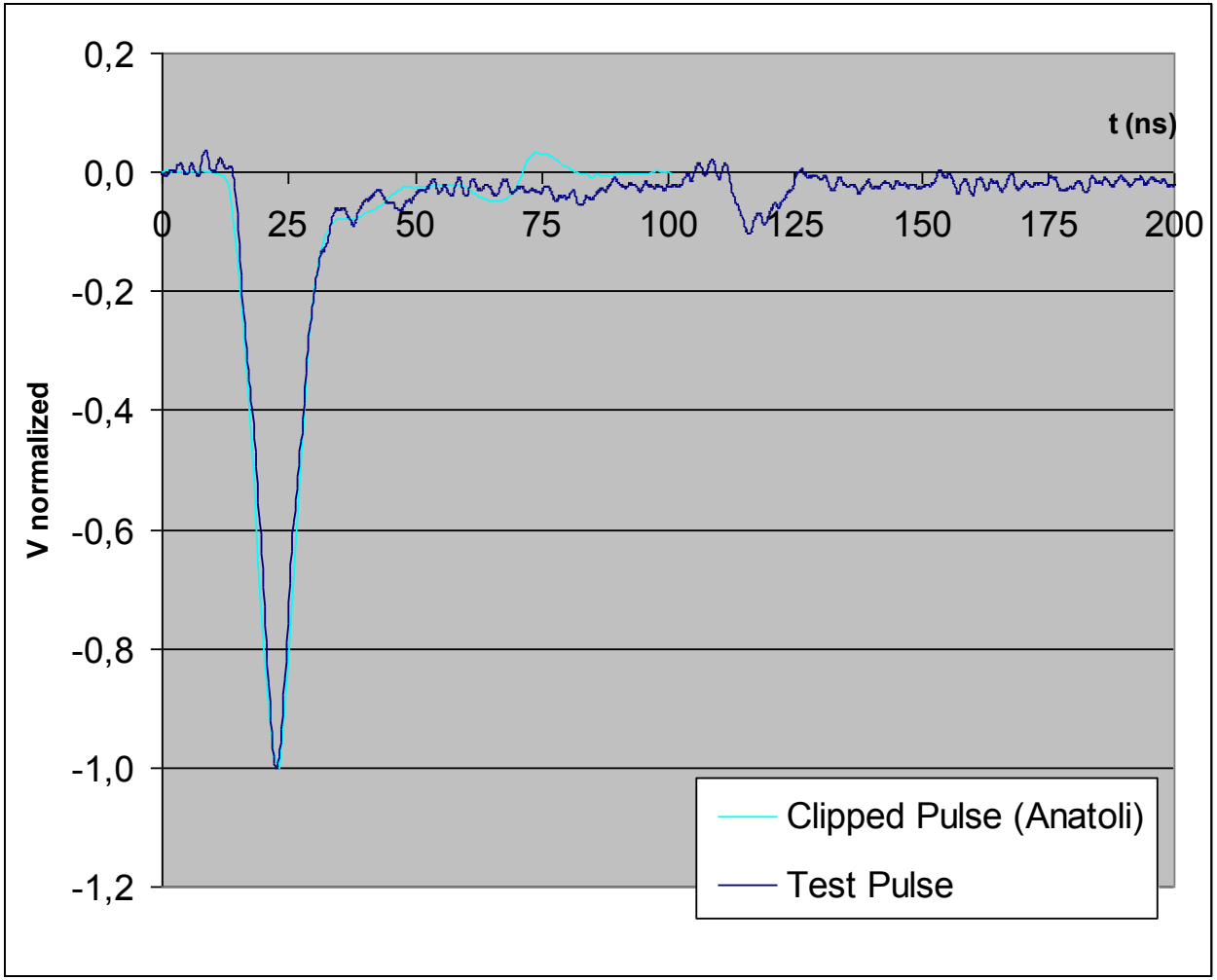
- Problem:
  - Due to clock jitter, the signal at the output must be stable (<1%) for 4 ns.
- Input signal:
  - AWG generated similar to clipped (see next slide)
- Method:
  - Delay clock signal in 1ns increments
  - Use LEMO cable (minimum number of cables, 0 to 3)
  - Measure output signal and analyze

Setup:



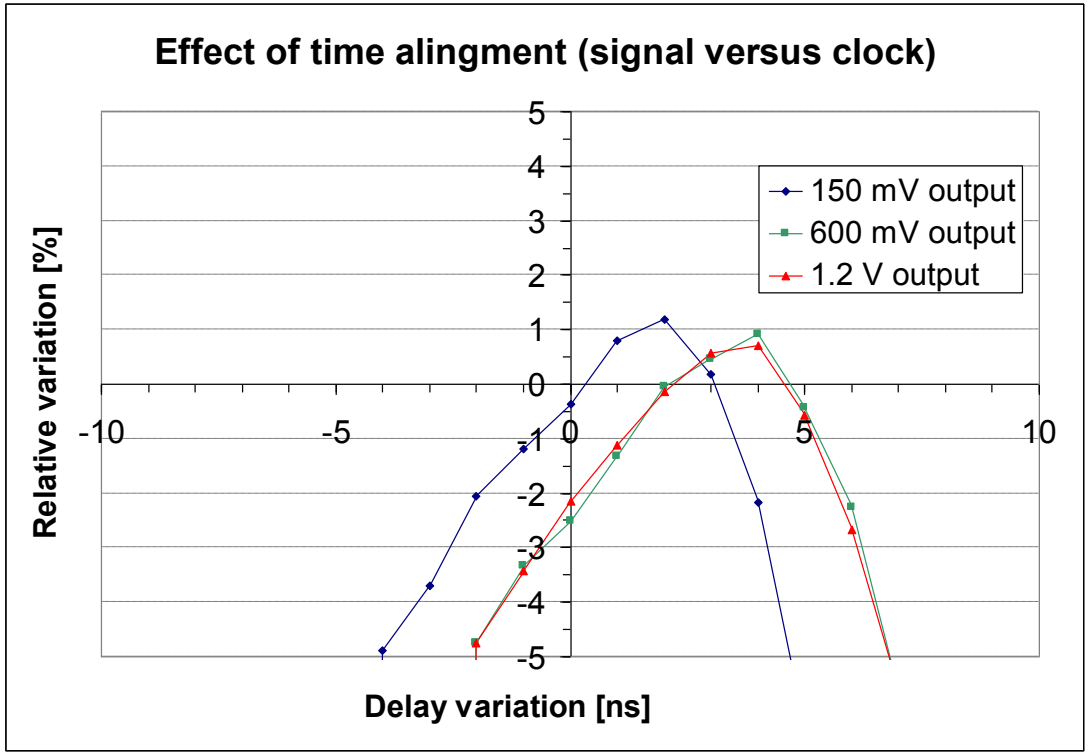
Flatness at the integrator output

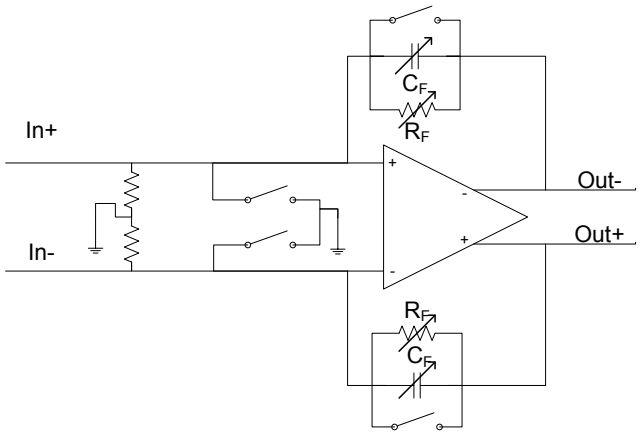
Waveform Generator signal vs. Measured clipped signal (Anatoli)



Flatness at the integrator output

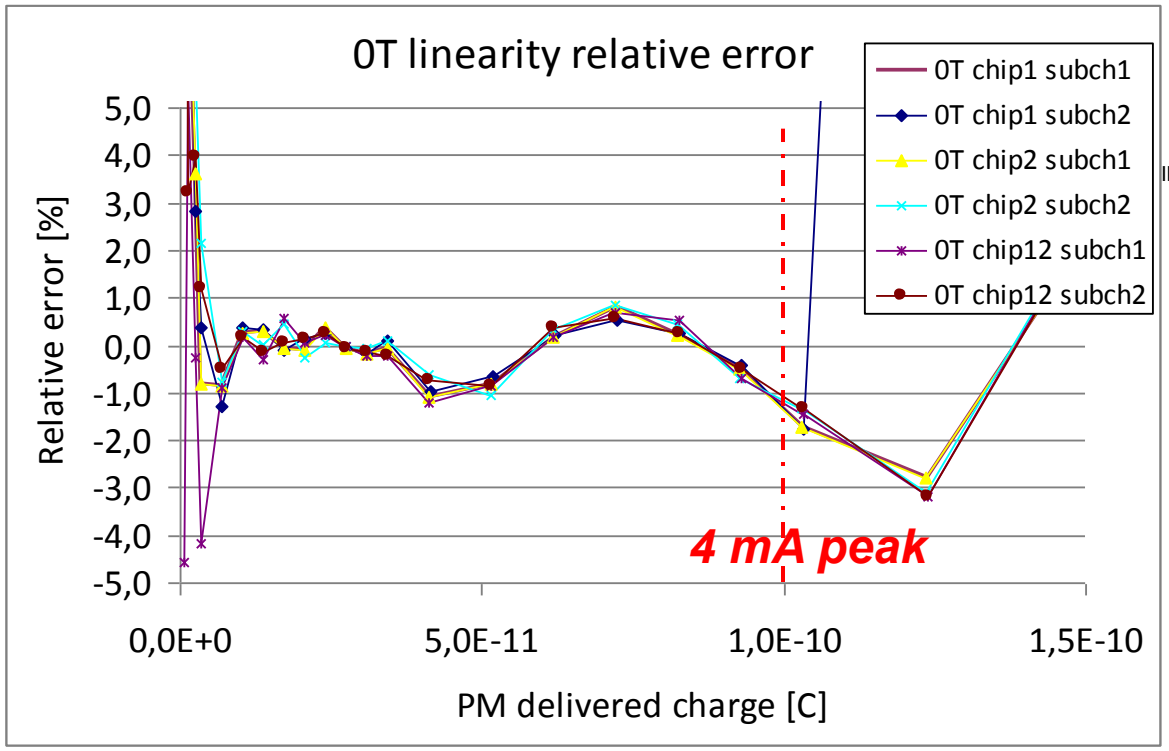
- The output variation is smaller than 1% for about 3 ns delay variation
  - Consistent for different signal amplitudes
- Can be improved using a resistor in parallel to the integrator capacitor

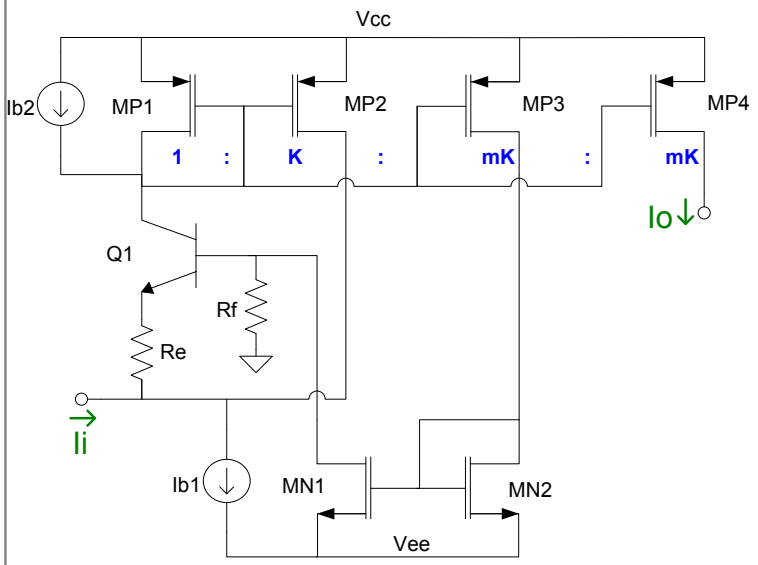




Current preamp (0T): first results (new!)

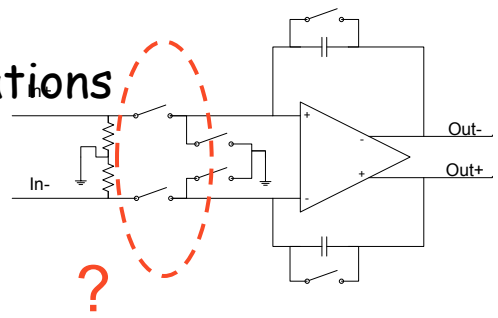
- We just started characterization
  - Current preamp (0T)
- Input range of about 4 mA peak current

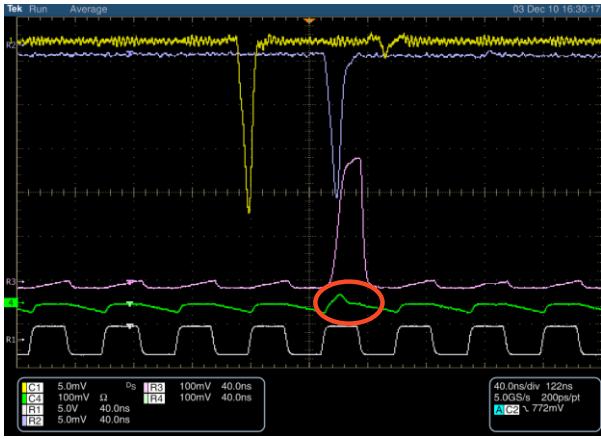




Summary and news

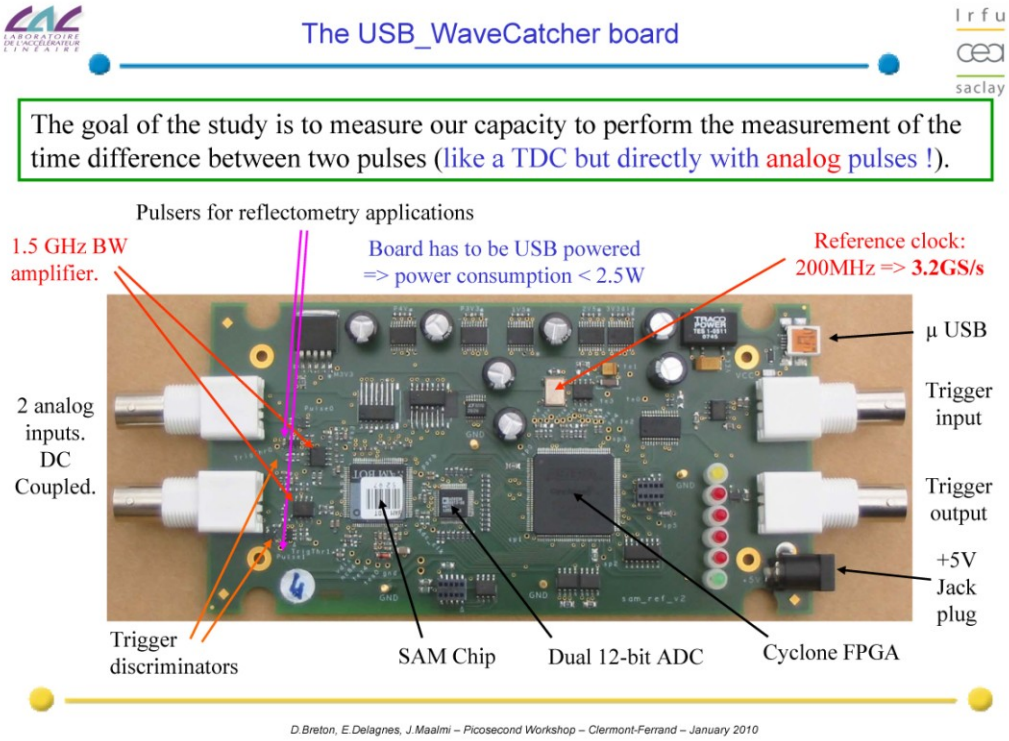
- Measurements of the input stage (preamp+integrator) are about finished
  - Principle is ok
  - Good results with 12 chips statistics
  - Need to study the effect of bias (op. paint) variation
- Characterization of individual blocks has started
  - Preamplifier:
    - Linear input range is almost 4 mA peak current
    - Could tolerate unclipped signal
    - Additional gain trimming should be foreseen
  - Fully differential amplifier: TbD
- Impact of the residual amplification in reset?
  - To be tested
  - Additional switches ?
  - Not needed according simulations
    - Few % error in the tail





Summary and news

- We are preparing a new set-up: AUTOMATIZED IN CAT
  - Analog mezzanine including ICECAL+ADC (see Carlos talk)
  - Calibrated and programmable attenuators (avoid generator “jitter” problem)
  - 12 bit 500 MHz (3 GS/s) DAQ: Wavecatcher (advertisement for Dominique)
    - Pulse reflectometry to measure input impedance
    - USB -> we should integrat it in CAT (or maybe it is done…)

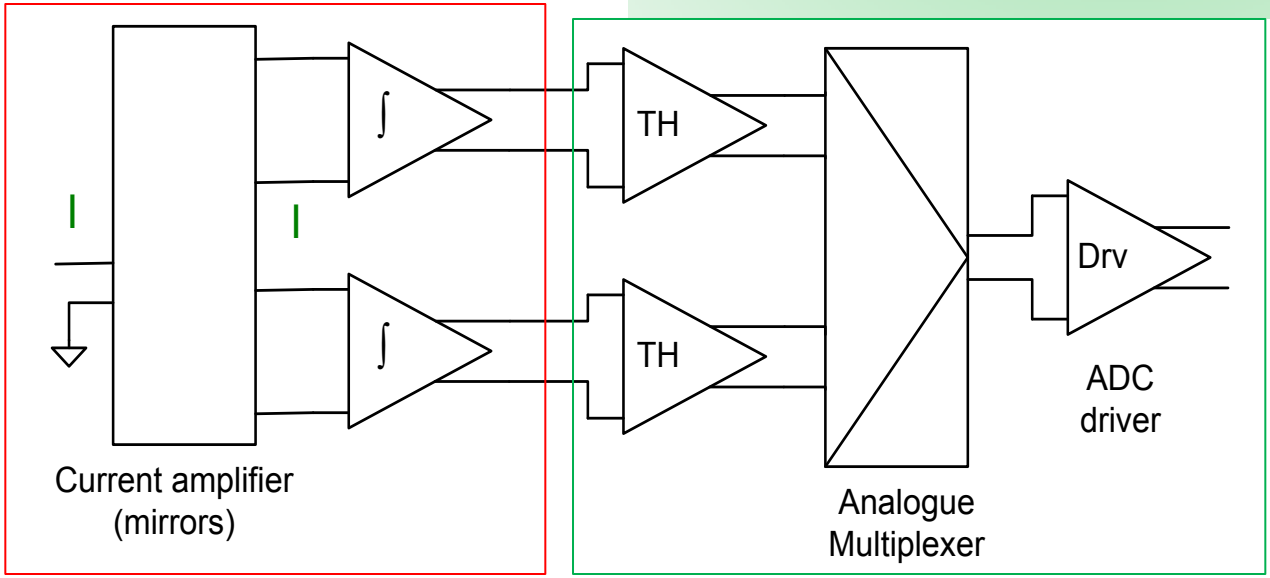


New blocks

- Prototyped in June AMS run:
  - Low noise current amplifier:
    - Basic schemes
  - Integrator:
    - High GBW fully differential OpAmp
      - Could be used in other stages

Ok, but need to add som tuneability

- To be tested in future runs:
  - Compensation of process variation of amplifier's input impedance
  - Track and hold (if needed)
  - Analogue multiplexer
  - ADC driver
    - ADC needs to be characterized
  - Common blocks:
    - Clock generation
    - Biasing (CMOS band gap already exists)



Plans

- Plans for 2011
  - Test and design until Q3 2011
  - There is no clear need of making more "partial" prototypes
  - Submit a prototype with few complete channels in Q4 2011
    - Still possible to send a critical block in June 2011 if needed
    - Goal of submitting a complete channel in Q4 2011 should be preserved
- And for 2012, if everything is ok…
  - Test beam ?
    - Mind we said that in December, before Chamonix…
  - Radiation tests?
- Long term: technology obsolescence…
  - AMS 0.35 um is a "mature" techno
  - We asked to Europractice: 5 years are "guaranteed"
    - Low volume productions are scheduled
    - Production (engineering run) is safe
    - But for desin (MPW runs) we should not relax