Laboratoire de l'Accélérateur Linéaire (IN2P3-CNRS) Orsay, France

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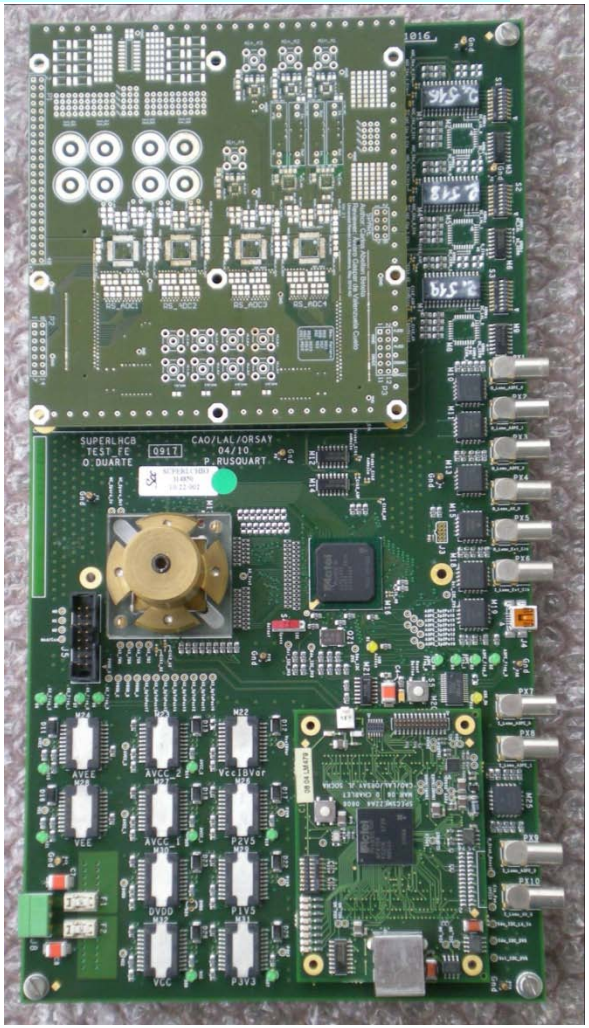
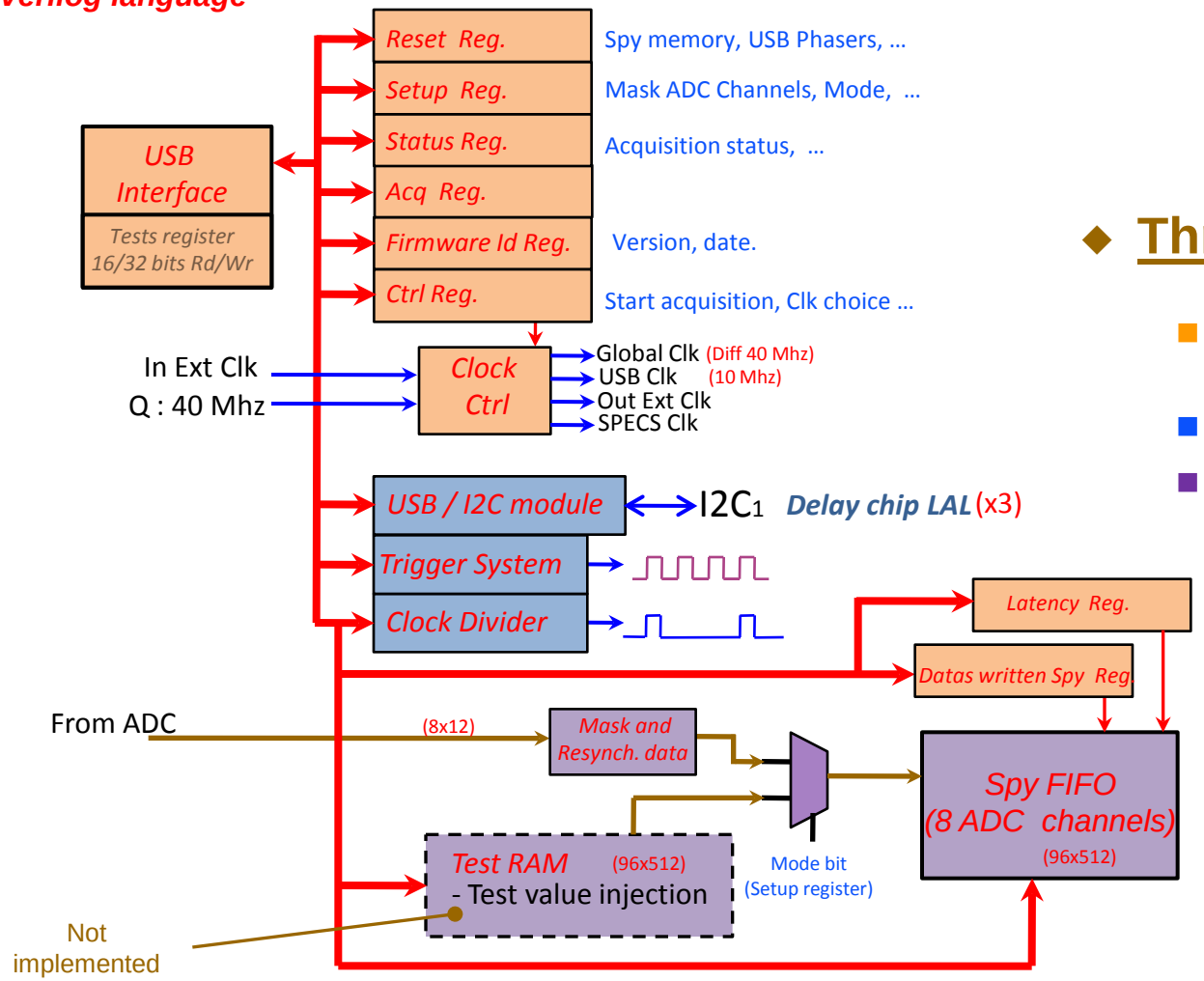
Tests Front-end card Status

- Firmware A3PE
  - Architecture status
  - Clock divider and Trigger generator
- Acquisition sequence
- Basic DAQ
- Test status
- Next step



Firmware architecture status

All Blocks inside A3PE1500 in Verilog language



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- **Three functional parts**
  - **USB and control board**
  - **General functionality**
  - **DAQ**

A3PE firmware blocks : Clock divider and trigger generator

- **Clock divider**
  - **50 ns to 0.4s (24 bits counter)**

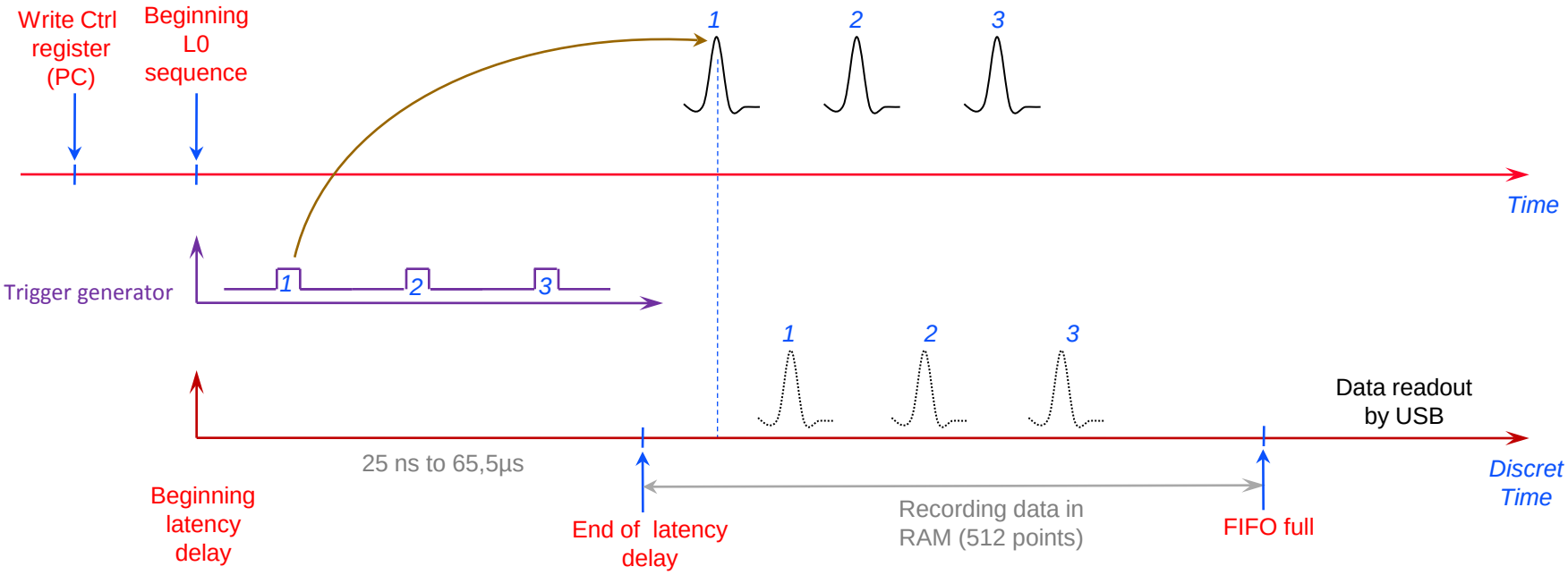
- **Trigger generator (L0)**

  With this module we can produce trigger (external trigger or software command)

Trigger generator registers (32b) loaded by USB

bit[7:0] : define Tdelay
bit[23:8] : define time between 2 trigger
bit[31:24] : define trigger number

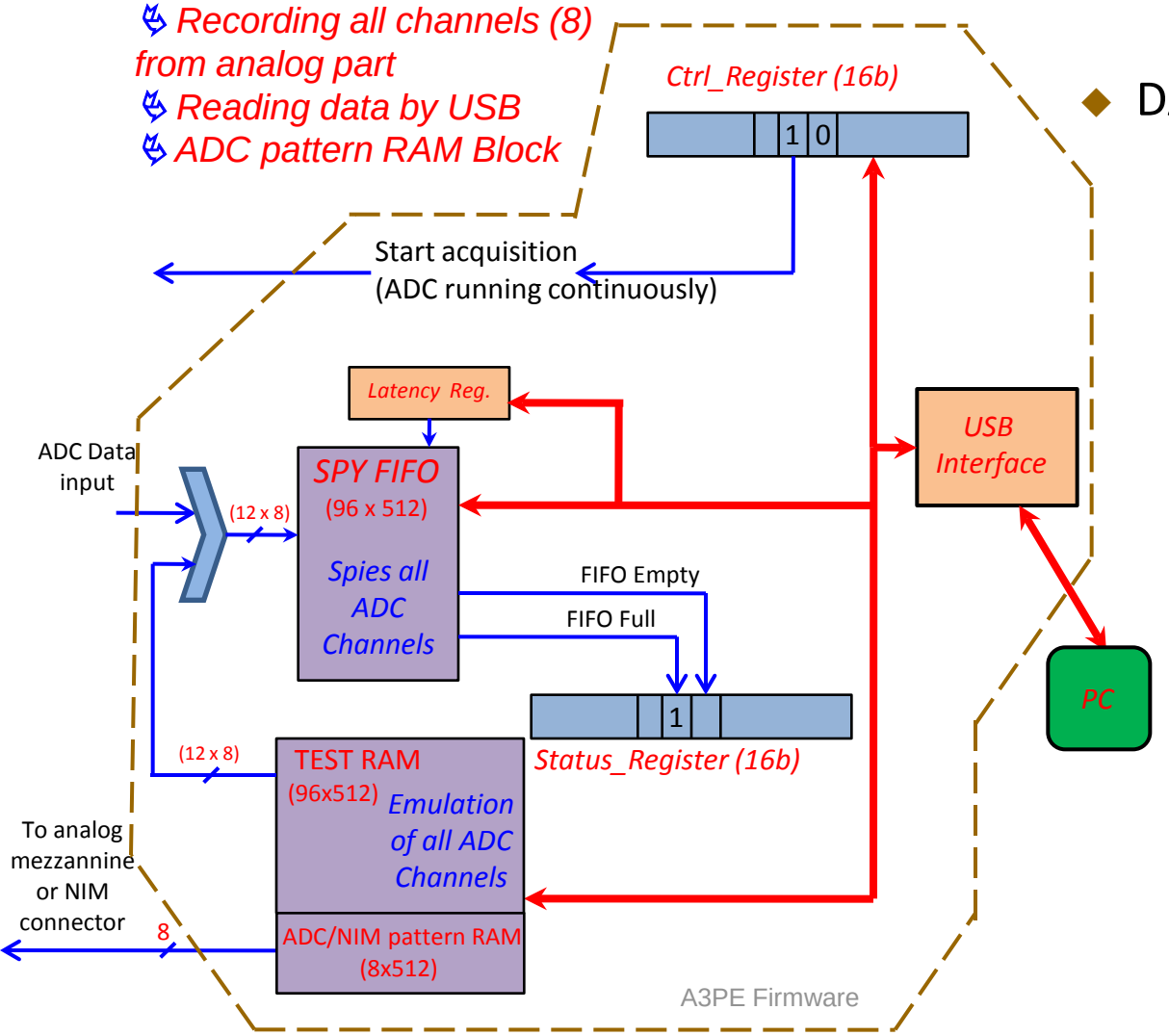
Acquisition sequence



- **PC write start sequence bit of Ctrl register.**
- **Beginning of L0 sequence.**
- **Each trigger pulse involve pulse shape.**
- **At the end of the latency delay recording 512 points of data.**
- **At the end of the record the system write one “end of acquisition”bit in the Status register.**
- **The PC scrutinize the Ctrl register, when the “end of acquisition” is high the PC download data with the USB interface.**

Basic DAQ

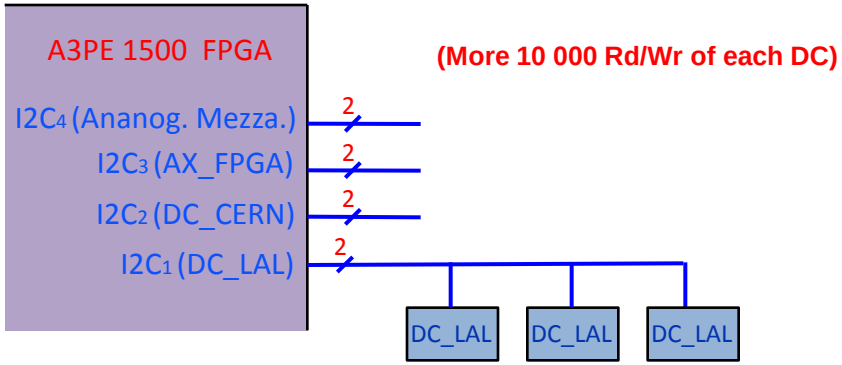
- Recording all channels (8) from analog part
- Reading data by USB
- ADC pattern RAM Block



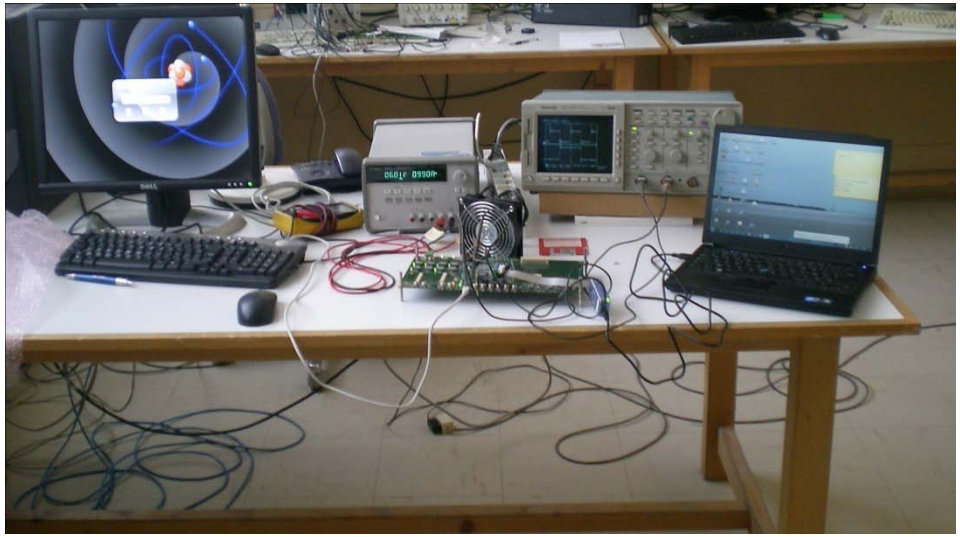
- DAQ sequence
  - Load RAMs sequences (Test and pattern)
  - USB Interface write the start_acquisition bit in the Ctrl_Register
  - ADC data are writing in FIFO
  - When the FIFO is full we write FIFO_full bit in the Status_register
  - The PC scrutinize the status register and when the FIFO_full bit is high the USB read the FIFO
  - When the FIFO is empty we can start new acquisition

Tests Status

- **Intensive tests with Frédéric's code**
  - **Rd / Wr register**
  - **Rd / Wr Spy FIFO**
  - **I2C module (Delay Chip)**
    (first I2C module to drive DC_LAL)



(More 10 000 Rd/Wr of each DC)



- **Tests with "test_245" by Chafik.**
  - **Latency delay**
  - **Reset tree**
  - **…**

Next steps

End of February

- **AX500 Basic test, before cabling 2 new board.**
- **RAM test.** *(Thierry's code)*
- **Tests trigger generator module for Lemo outputs.**
- **Intensive test of basic DAQ.**
  Recording all channels (8) from analog part and read data by USB
- **Digital board for Barcelona team.**
- **Analog board for LAL team ?**

Spring / summer

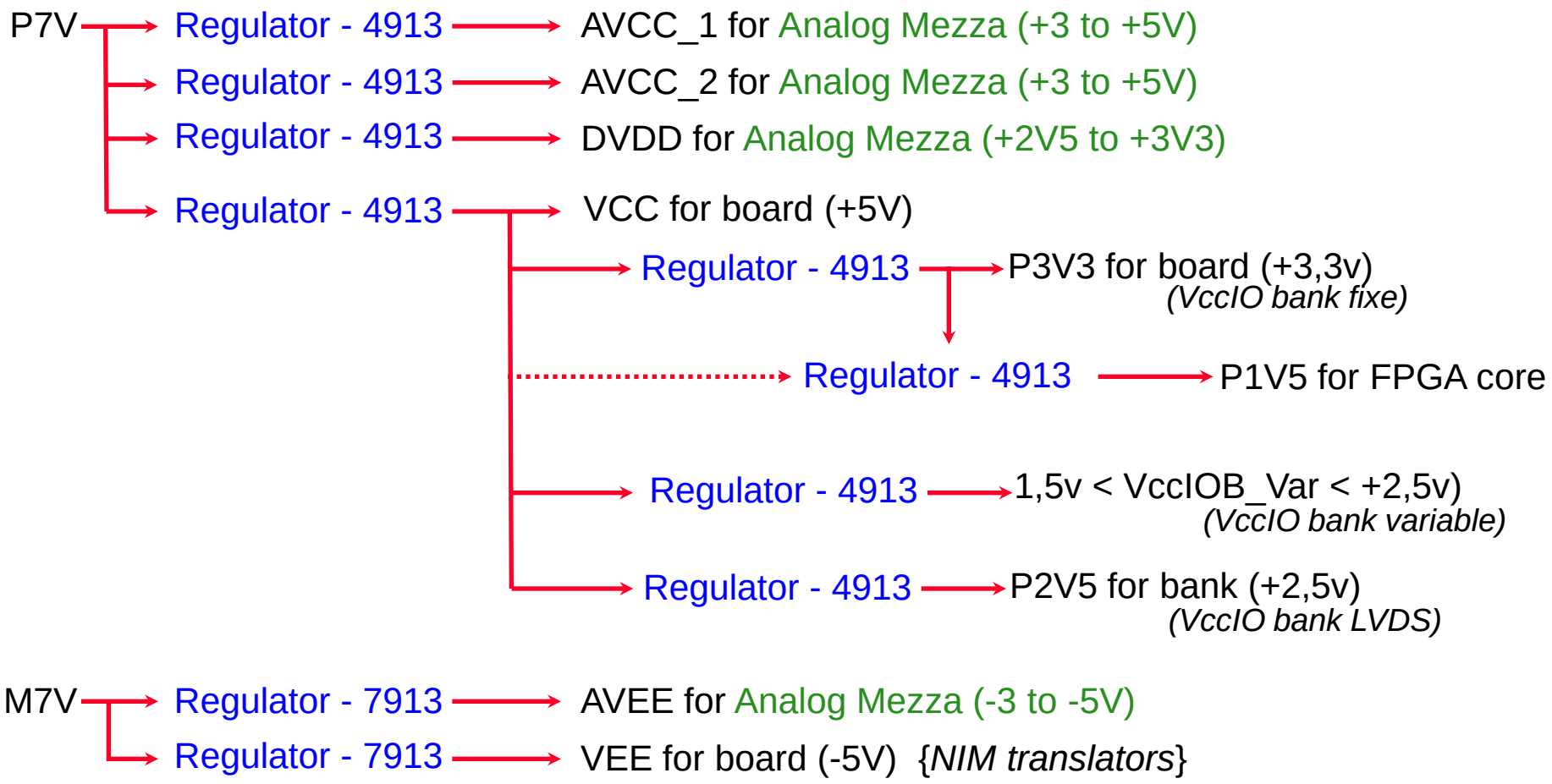
- **Processing ADC data (dynamic pedestal subtraction)**
  Adaptation Christophe's code or PC computing
- **Packing**
- **A3PE FPGA tests (SS0, SSI, …)**

Depending accelerator availability !

- **Radiation tests**

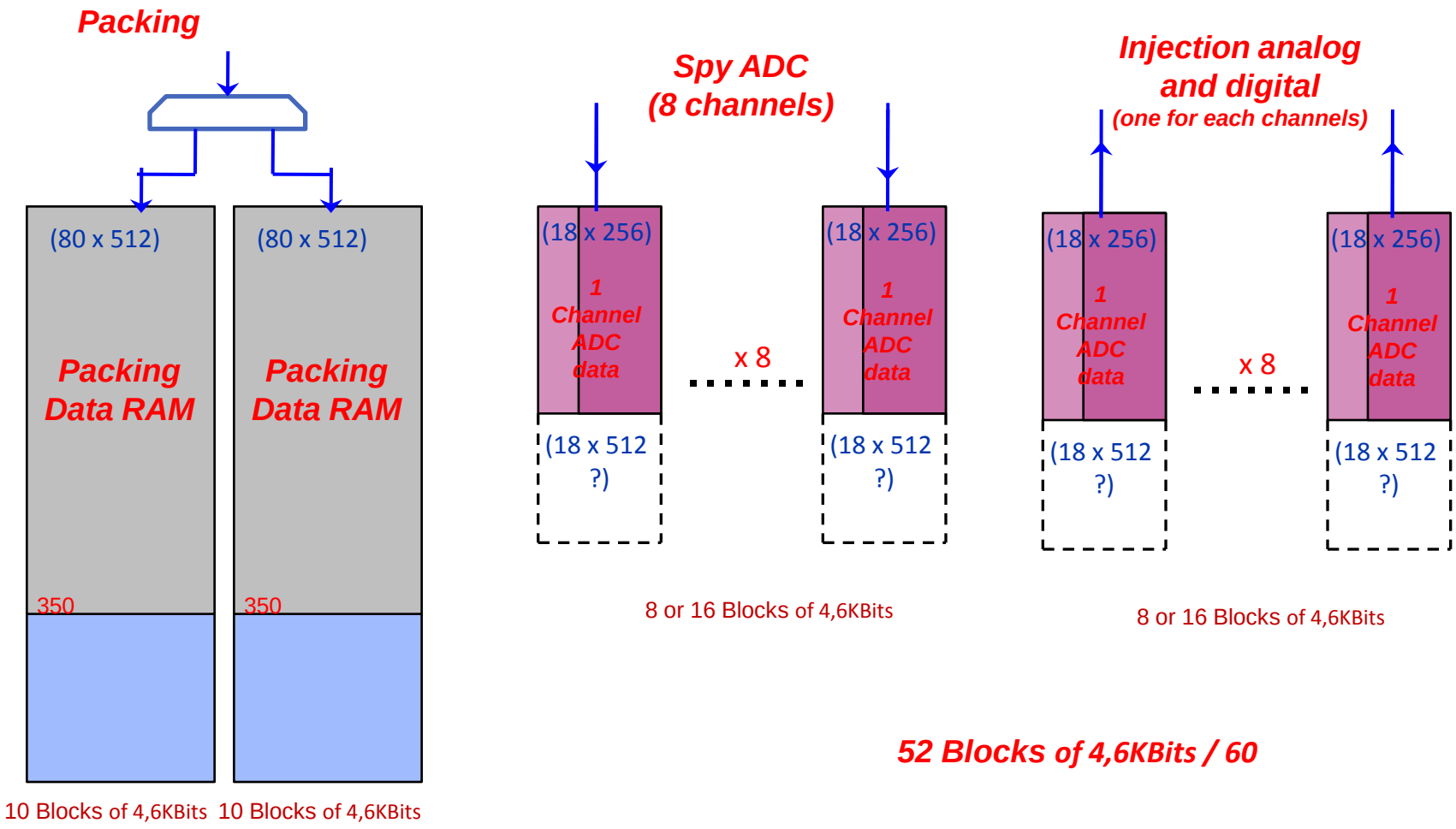
SPARE

Tests board power supply



- ***Lab. Power Supply input (+/- 7V)***
- ***10 Radiation tolerance regulators ! !***

New RAM Blocks organization



52 Blocks of 4,6KBits / 60