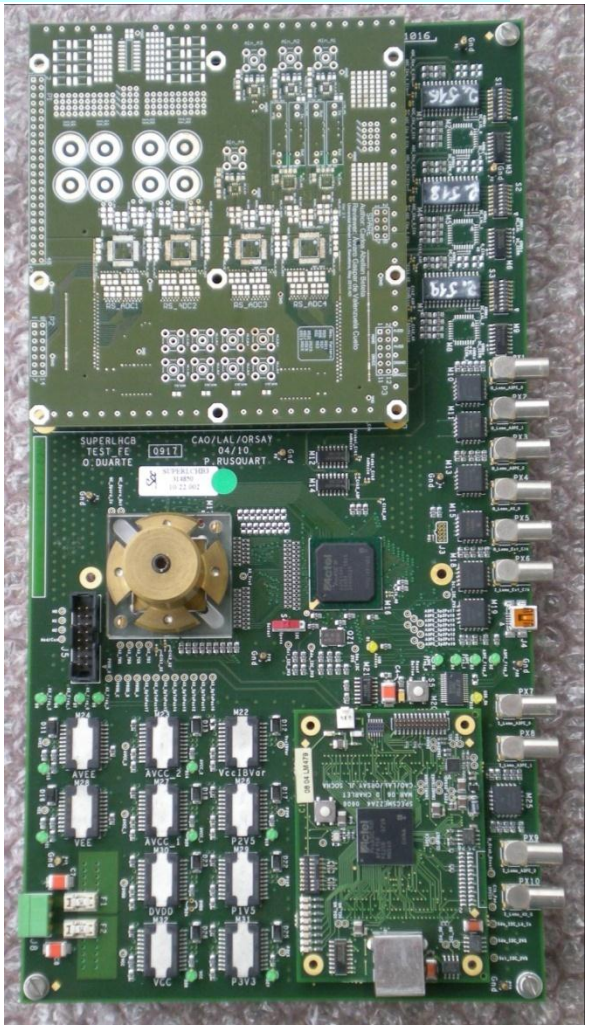
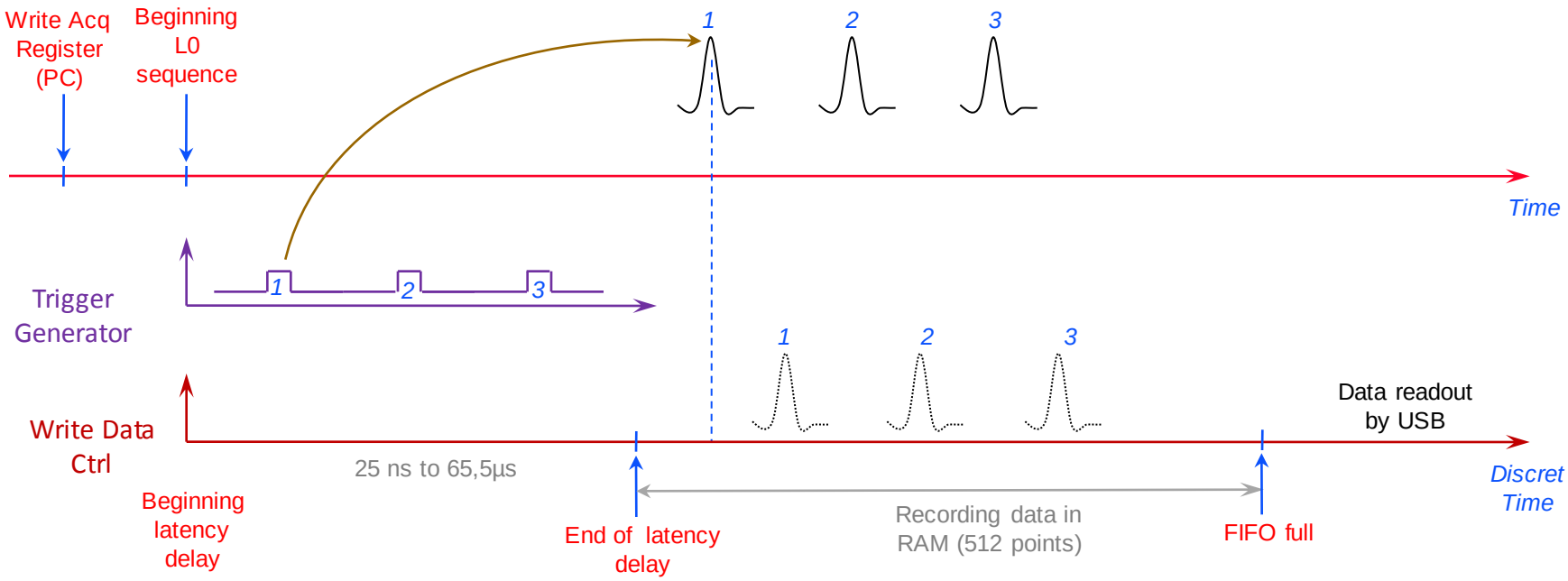
Tests tools for Analog and Digital parts

- Typical acquisition sequence
- Basic DAQ tests and results
- Tools to test Analog part
- First tests with AX FPGA
- Tools to test A3PE FPGA (SSO & SSI)
- Conclusion : next steps



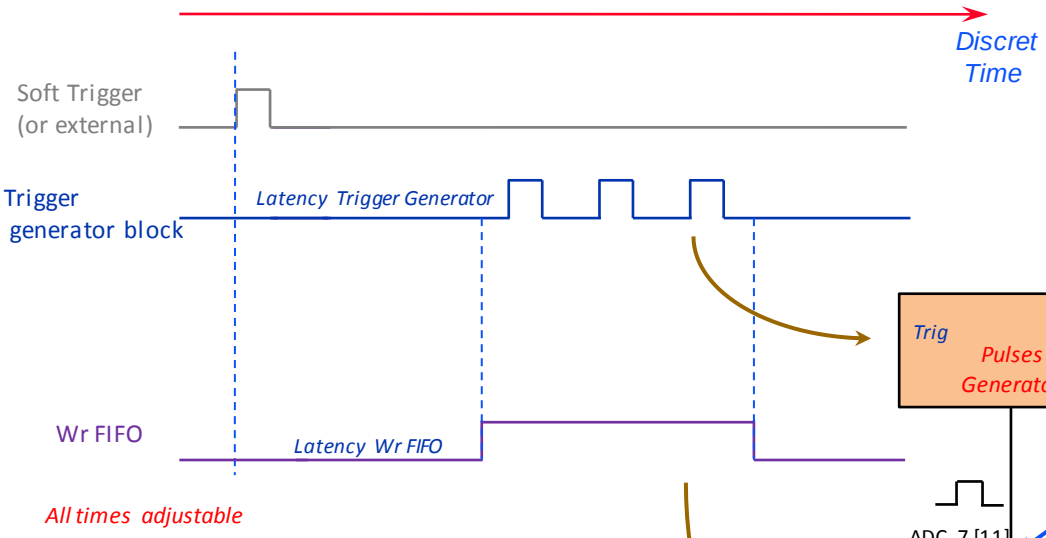
Caceres Thierry
Duarte Olivier

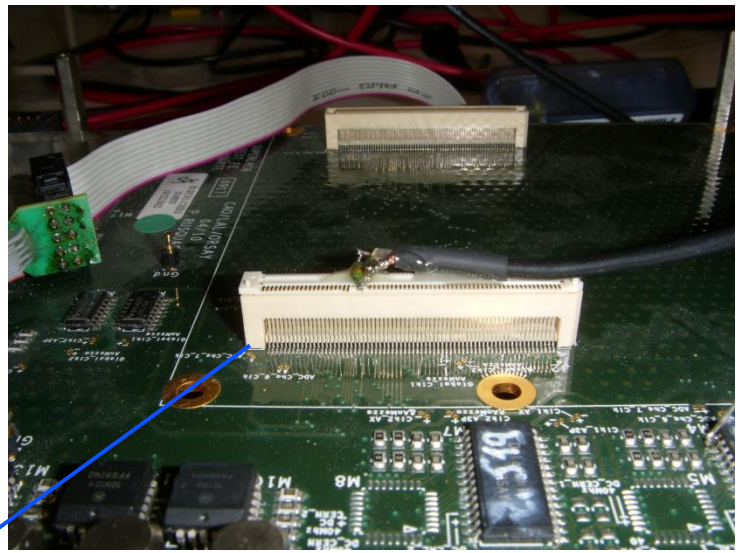
Reminder : Typical acquisition sequence

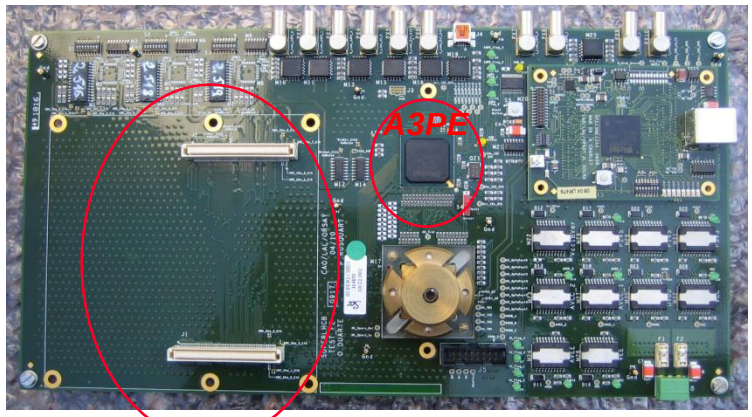


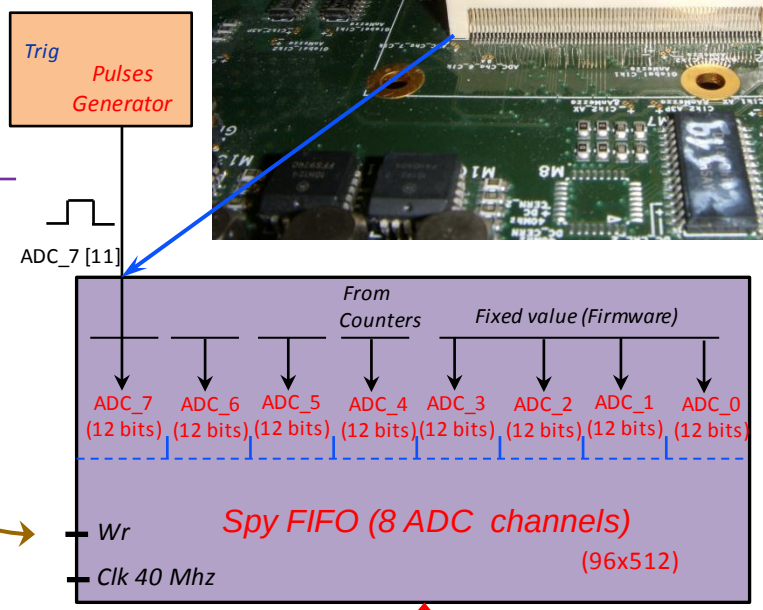
- PC write start sequence bit of Acquisition (Acq) Register.
- Beginning of L0 sequence.
- Each trigger pulse involve pulse shape.
- At the end of the latency delay recording 512 points of data (Max).
- At the end of the record the system write one “end of acquisition”bit in the Acq_Register .
- The PC scrutinize the Acq_Register, when the “end of acquisition” is high the PC download data with the USB interface.

Reminder : Basic DAQ tests



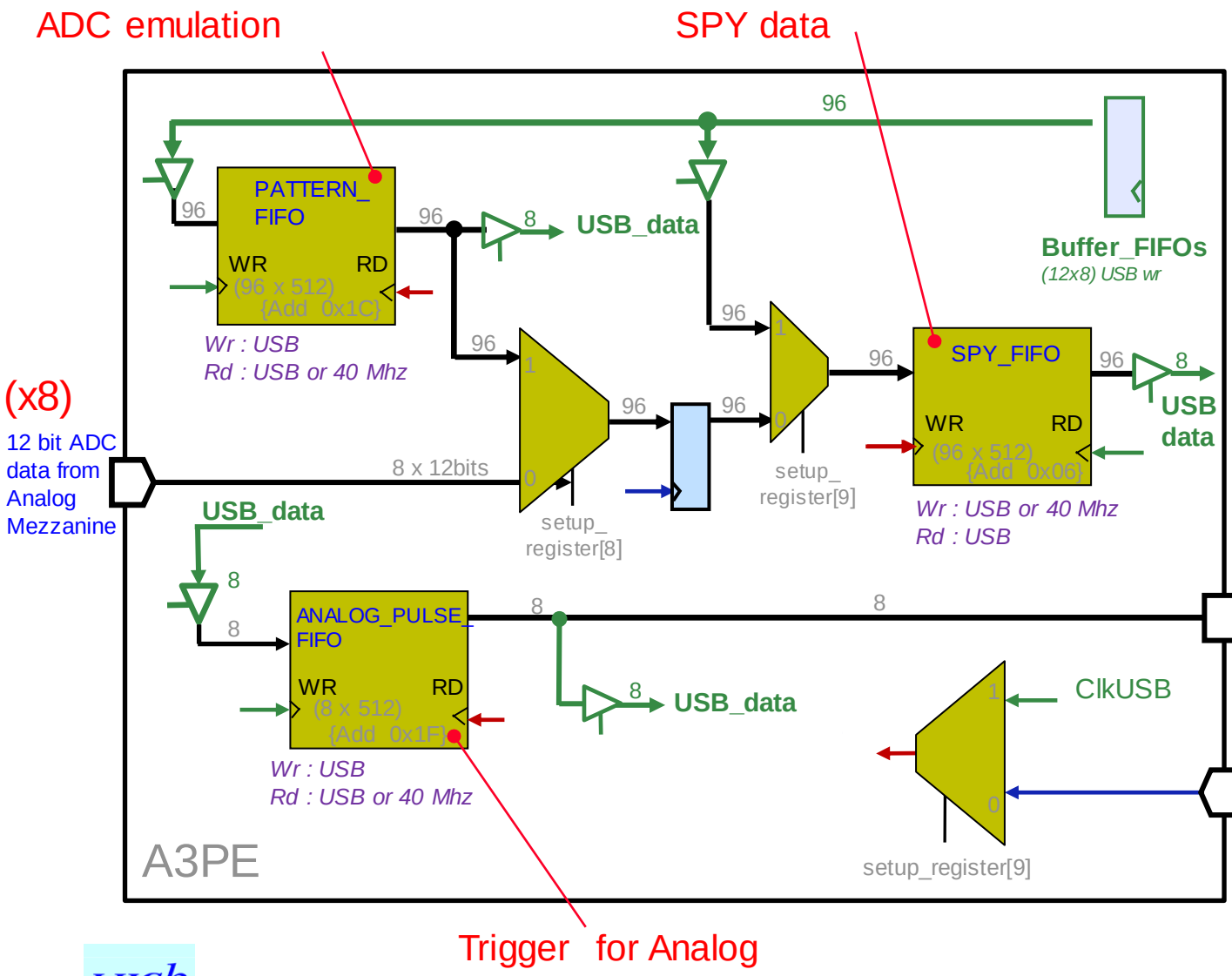






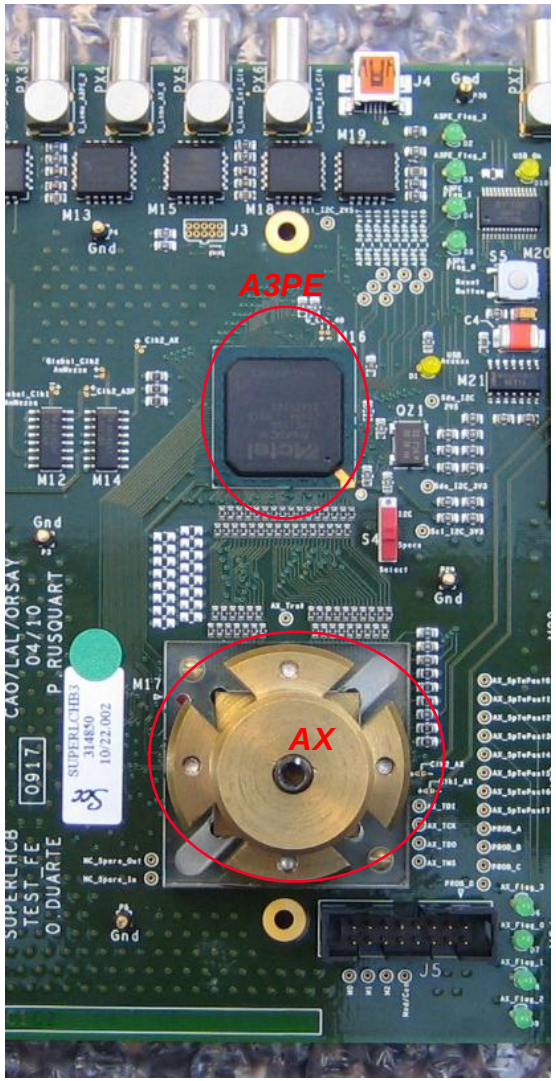
- Fixed data, counter and pulse stand in for ADC data from analog mezzanine

Tools to test Analog part

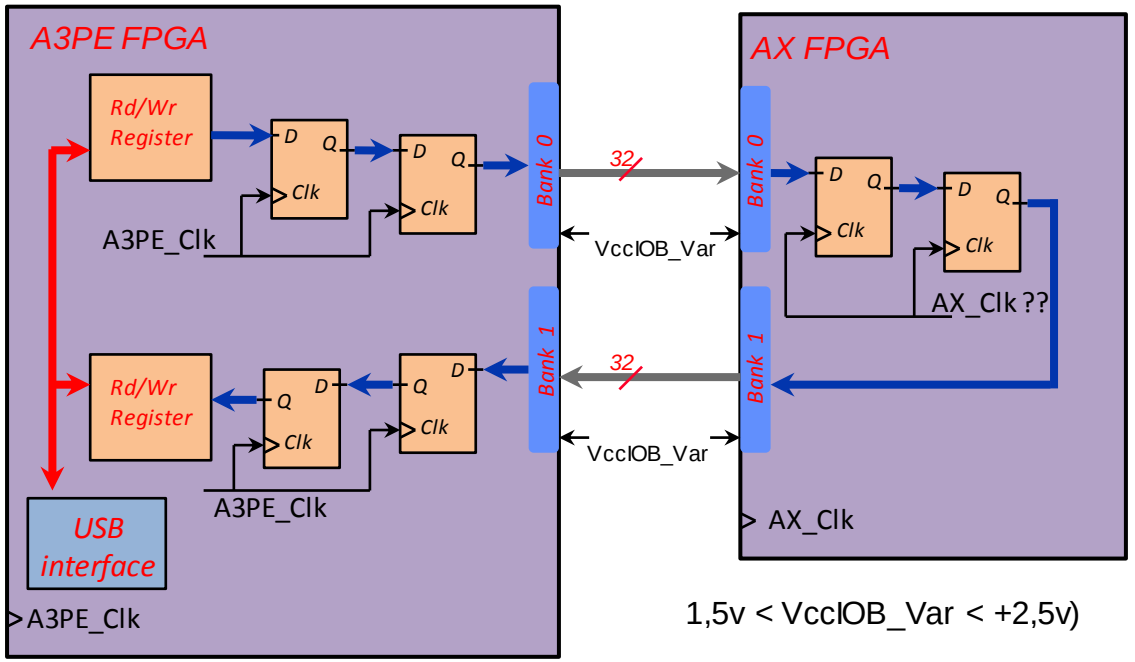


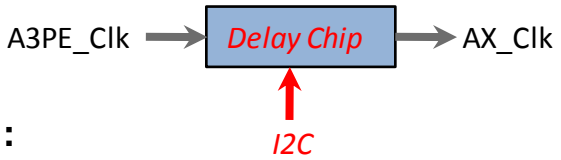
- **FIFO pattern**
  - Generate digital signals
  - Check FPGA computations
- **SPY FIFO**
  storage of processing results
- **ANALOG PULSE FIFO**
  generate trigger of analog pulses

First tests with AX FPGA



Idea : RAM pattern to test the A3PE IOs functioning by exchanging data between the 2 FPGA (SSO and SSI)

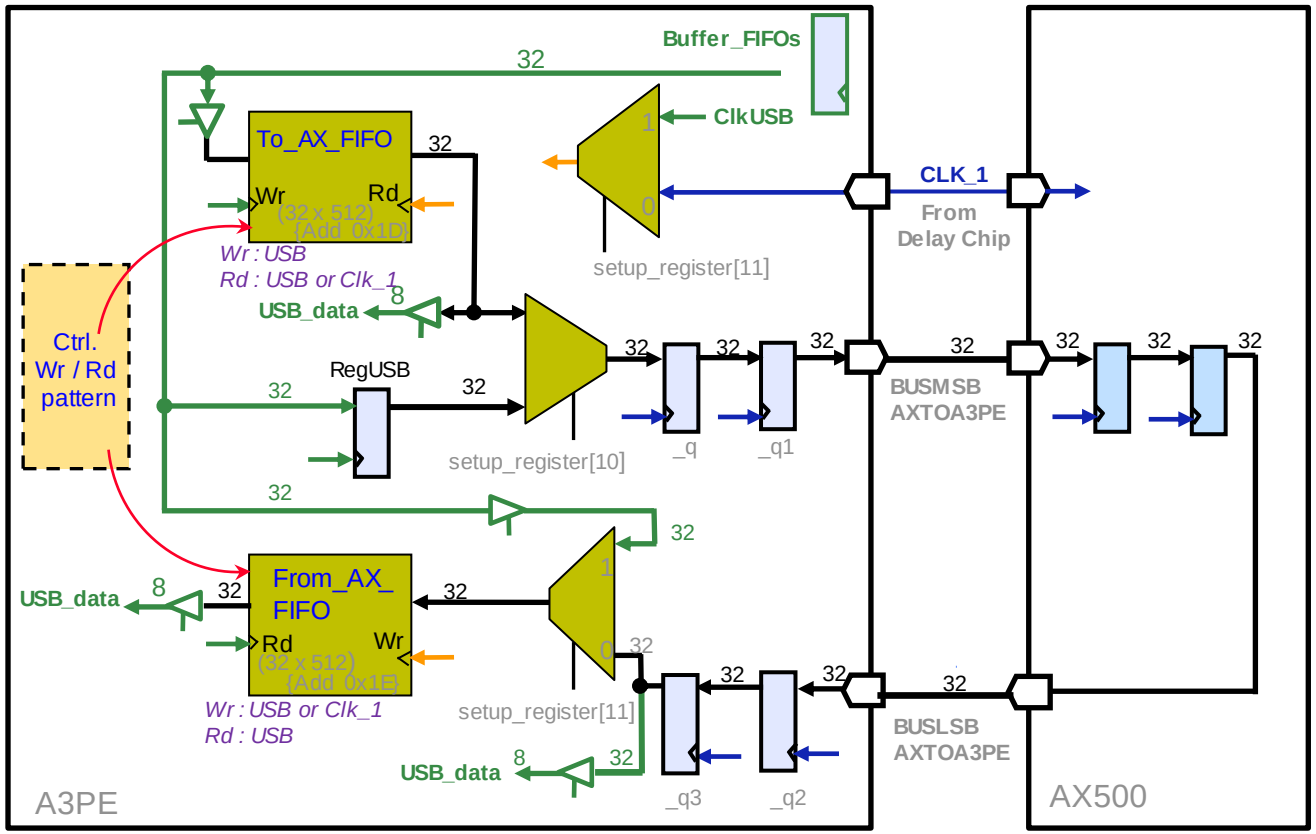




- **Reminder :**
  - ProASIC3 families are based on nonvolatile flash technology
    => reprogrammable
  - The latest antifuse FPGA family
    => Not reprogrammable

Tools to test A3PE FPGA (SSO & SSI)

Idea : RAM pattern to test the A3PE IOs functioning by exchanging data between the 2 FPGA (SSO and SSI)



- USB Rd / Wr the FIFO (To_AX and From_AX).

Sequence:

- To_AX _FIFO Rd/Wr by USB
- Start commande
- Loop on to AX_FIFO until stop command
- Programmable latency to capture data from To_AX_FIFO to FROM_AX_FIFO

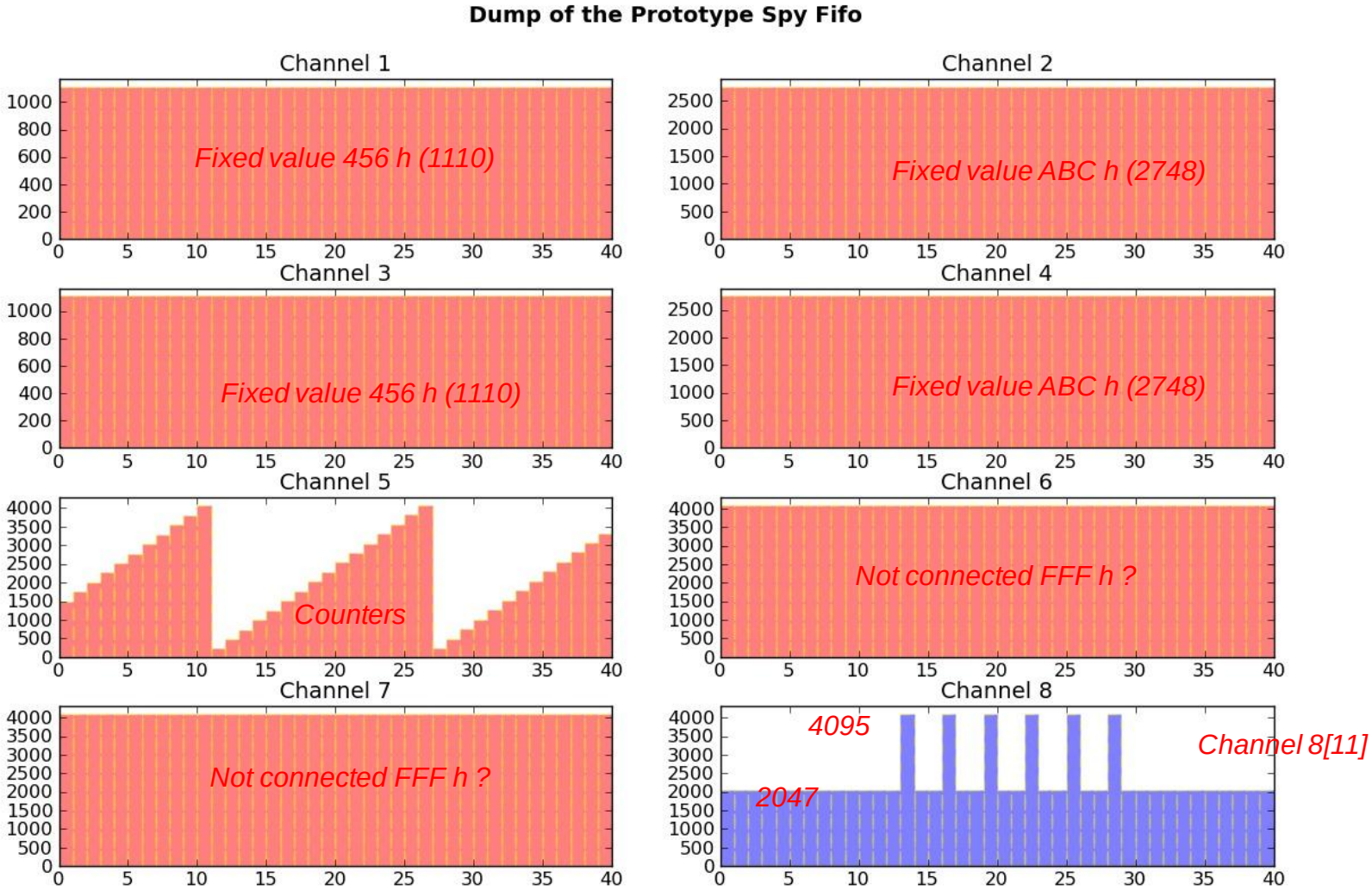
- Start / Stop and latency missing (not implemented yet)

Conclusion

- Digital electronic is ok, several adjustment have been done (Tests with Carlos at LAL in November).
- Do you have other needs of firmware to test the analog mezzanine ? ?
- Started Production of third mother digital board (ready in Jannuary)
- Should we considered a 8 channel prototype FEB for the end of 2012 with GBT ?
- Packing is in stand by. Waiting for decision on GBT bandwith.

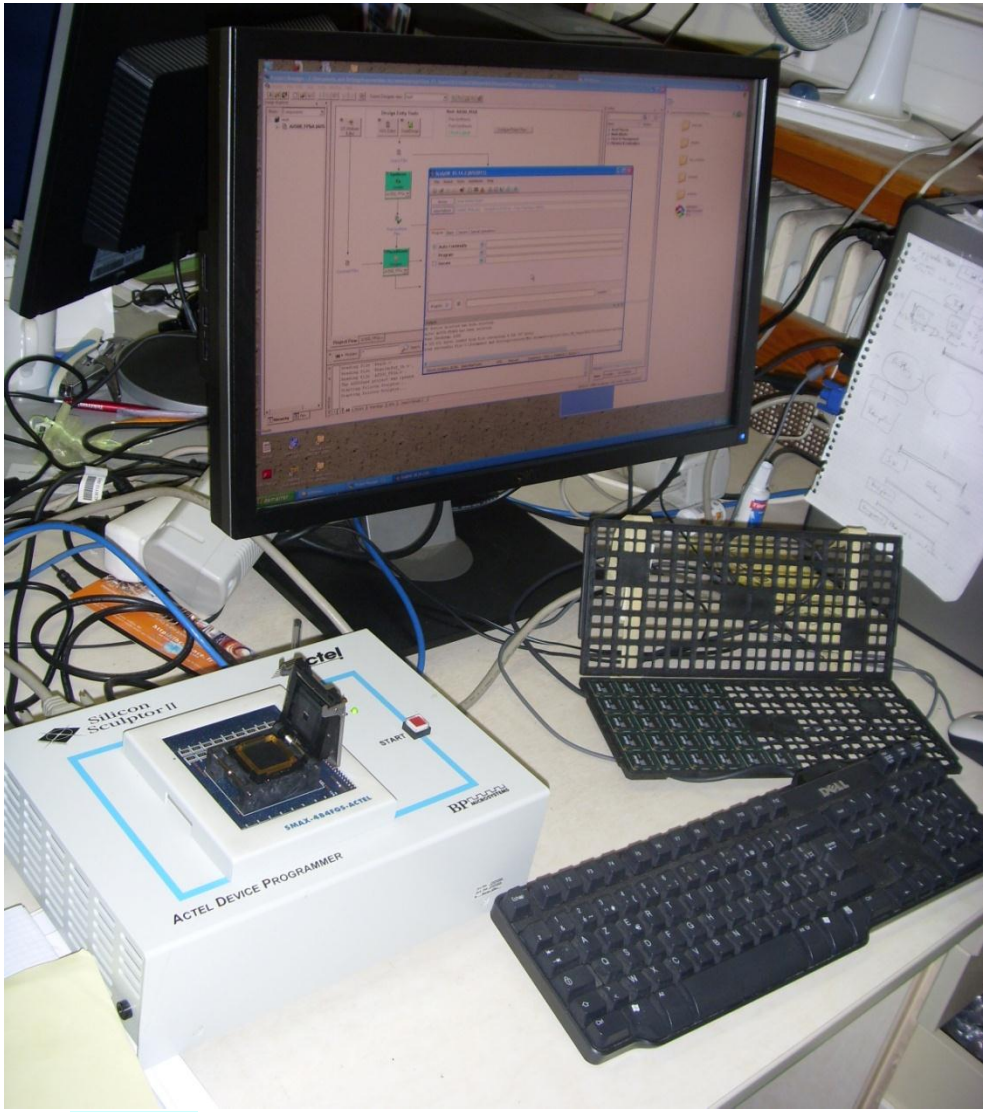
SPARE

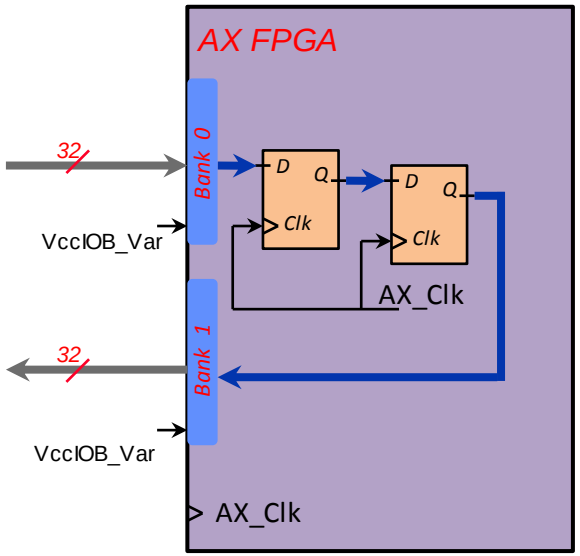
Reminder : Basic DAQ tests results



Trigger generator block

First tests with AX FPGA

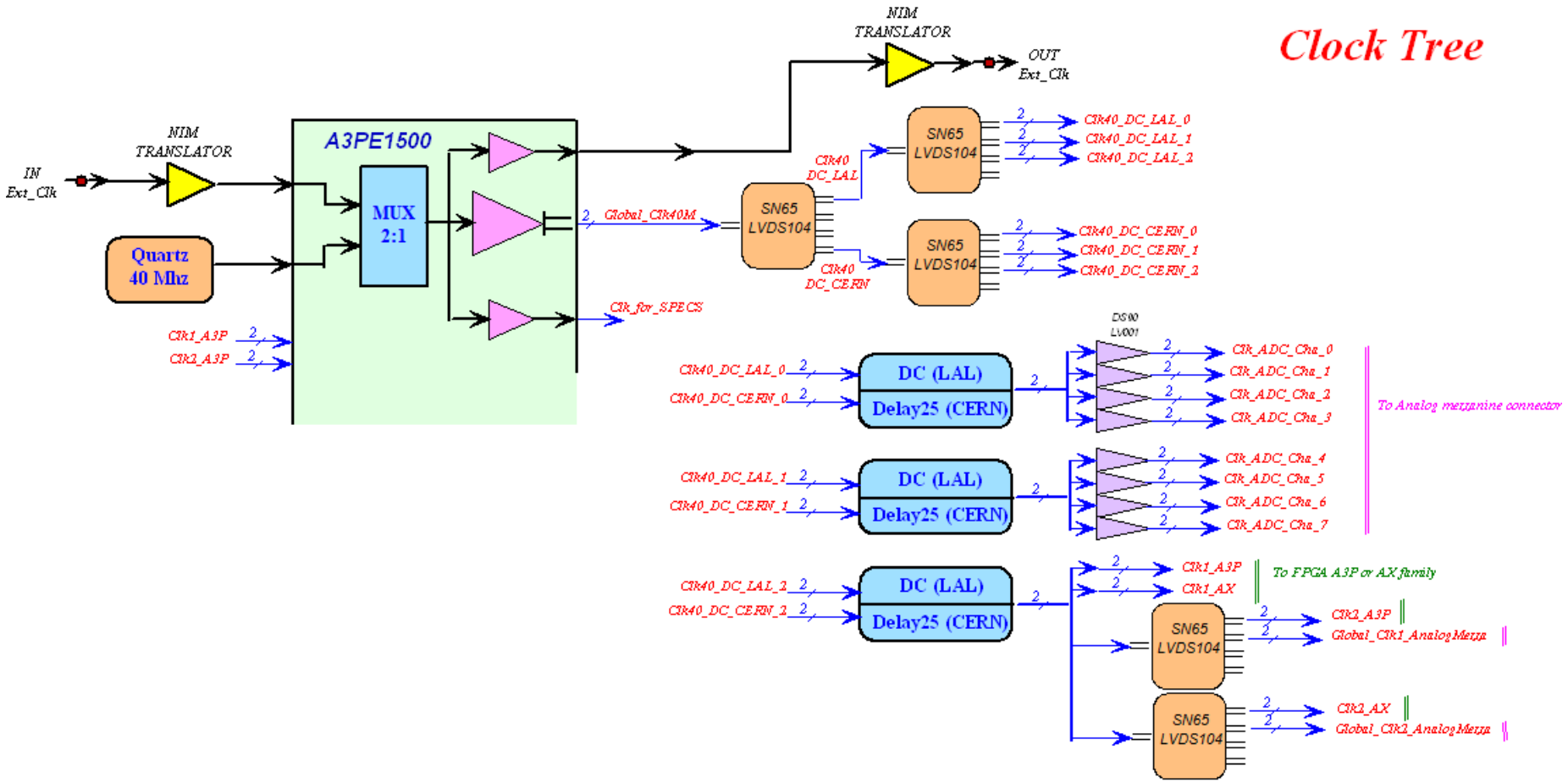




1,5v < VcclOB_Var < +2,5v)

- **Reminder :**
  - ProASIC3 families are based on not volatile flash technology
    => reprogrammable
  - AX is the latest antifuse FPGA family
    => Not reprogrammable
  - AX programmation with Silicon Scultor

Clock tree


Clock Tree
NIM TRANSLATOR
OUT Ext_Clk
NIM TRANSLATOR
IN Ext_Clk
A3PE1500
MUX 2:1
Quartz 40 Mhz
Clk1_A3P
Clk2_A3P
Global_Clk40M
Clk_for_SPECS
SN65 LVDS104
Clk40 DC_LAL
Clk40 DC_CERN
Clk40_DC_LAL_0
Clk40_DC_LAL_1
Clk40_DC_LAL_2
Clk40_DC_CERN_0
Clk40_DC_CERN_1
Clk40_DC_CERN_2
DS90 LV001
DC (LAL)
Delay25 (CERN)
Clk_ADC_Cha_0
Clk_ADC_Cha_1
Clk_ADC_Cha_2
Clk_ADC_Cha_3
Clk_ADC_Cha_4
Clk_ADC_Cha_5
Clk_ADC_Cha_6
Clk_ADC_Cha_7
To Analog mezzanine connector
Clk1_A3P
Clk1_AX
To FPGA A3P or AX family
Clk2_A3P
Global_Clk1_AnalogMezza
Clk2_AX
Global_Clk2_AnalogMezza
27th November , 2009