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LHCb Calorimeter Upgrade Electronics: ASIC solution status

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LHCb Calorimeter Upgrade Meeting – 16th December 2011 – CERN

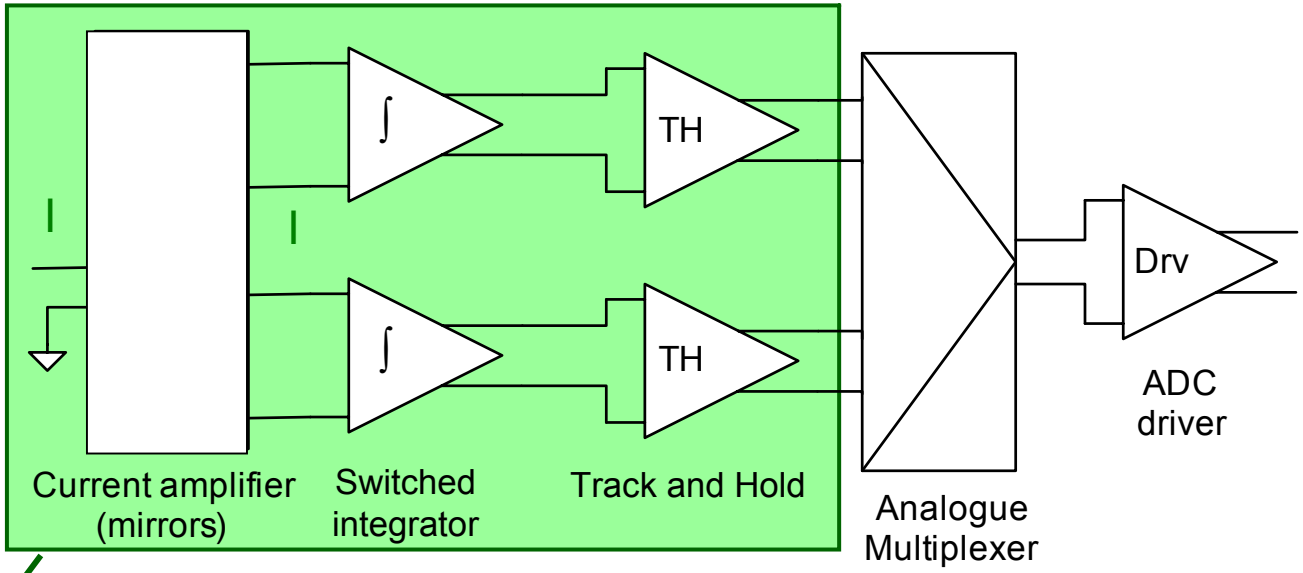
Outline

1. ASIC solution short review
2. Second prototype simulations and preliminar measurements
3. Discussion
4. Plans in short term
5. Plans in mid term

ASIC solution review

- Integrated circuit for the Upgrade of the LHCb Calorimeter Front End electronics
  - Architecture based on:
    - Current mode preamplifier with cooled termination for reduced input noise
    - 2 fully differential interleaved channels
    - Switched integrator
    - Track-and-Hold
- Measurements of the first prototype of the input stage (preamp+integrator) are about finished
  - Principle is ok
  - Good results with 12 chips statistics
  - Need to study the effect of bias (op. paint) variation
- A second prototype was submitted in June and received last week
  - It includes: preamp + integrator + track-and-hold
  - Added a feedback resistor to improve the integrator output stability

Second prototype



ICECAL2 chip:

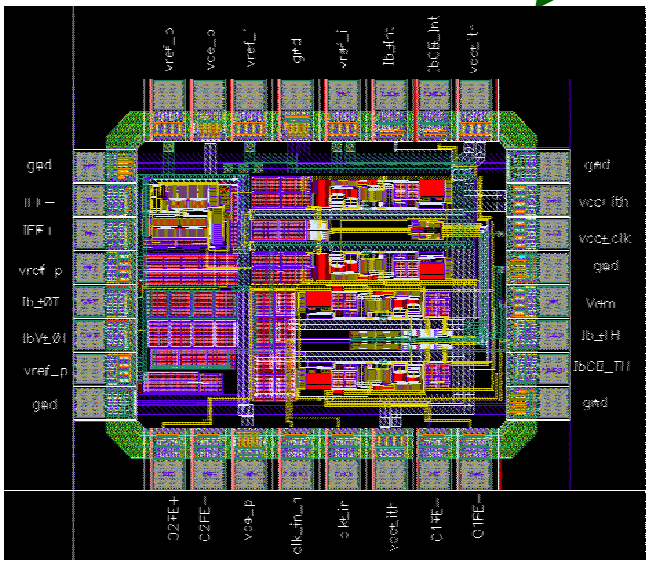
SiGe BiCMOS 0.35um

AMS 2 mm^2

10 units encapsulated (QFN32)

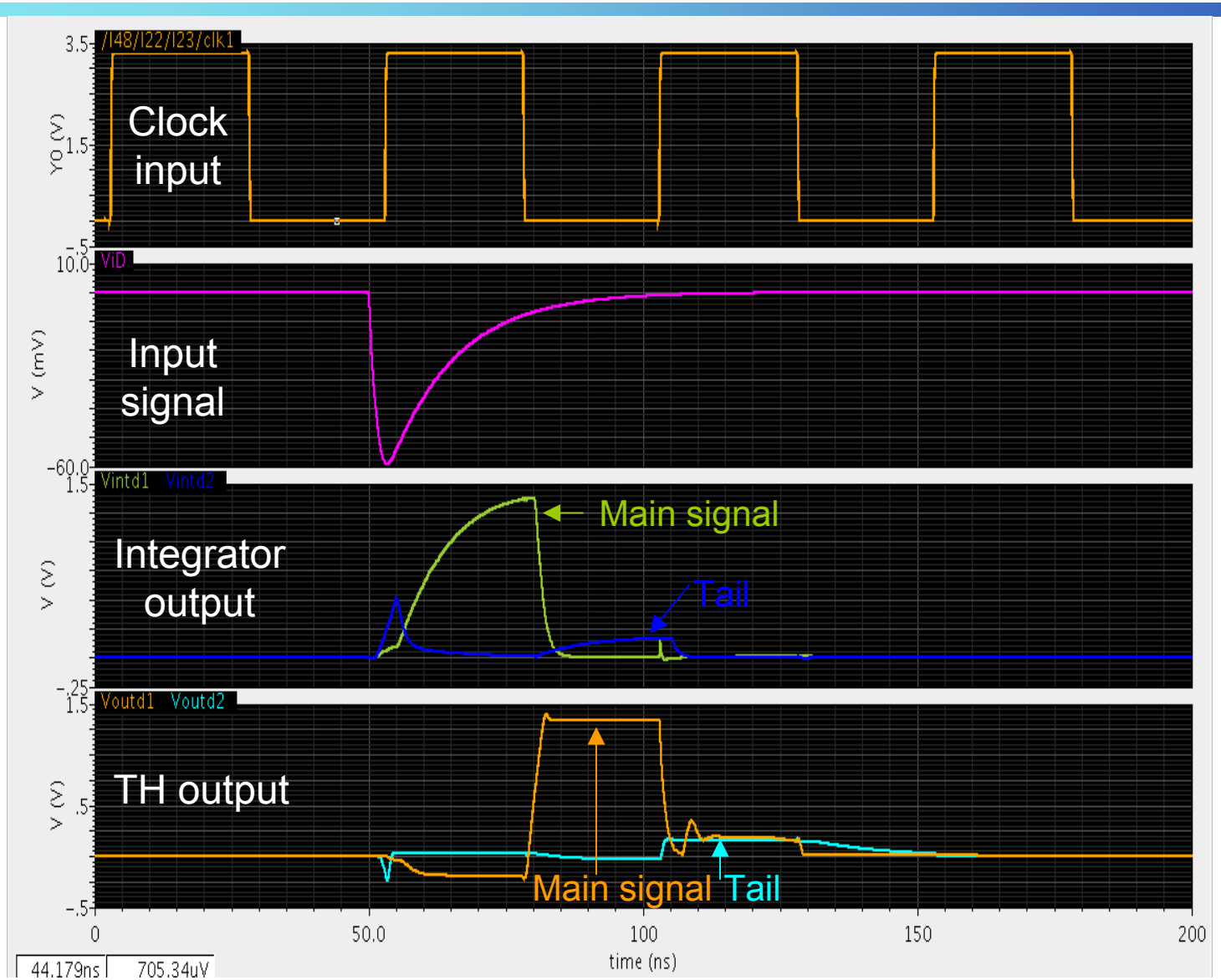
Submitted: June 6th 2011

Received: October 5th 2011

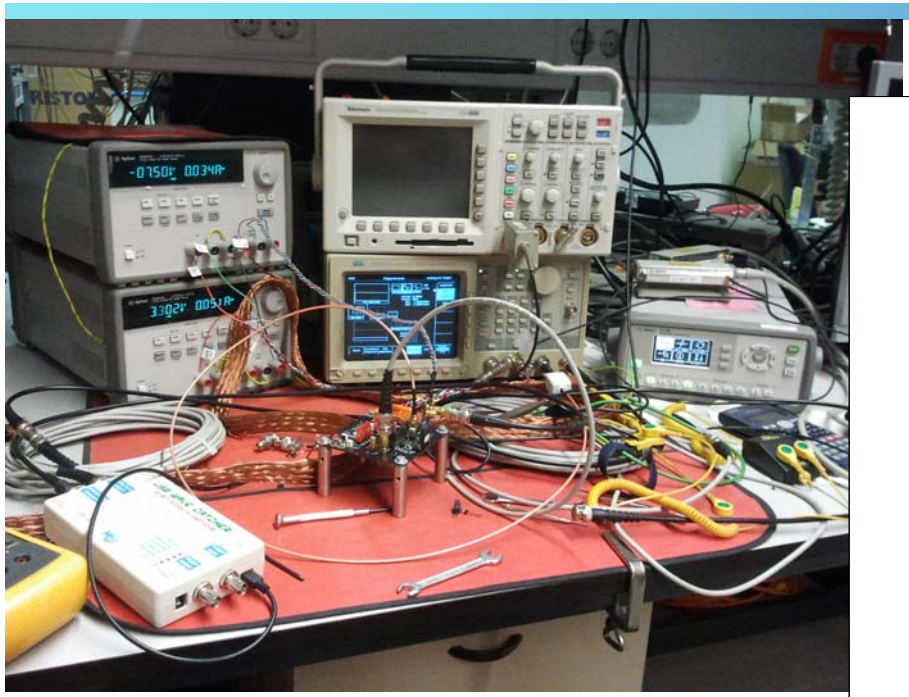


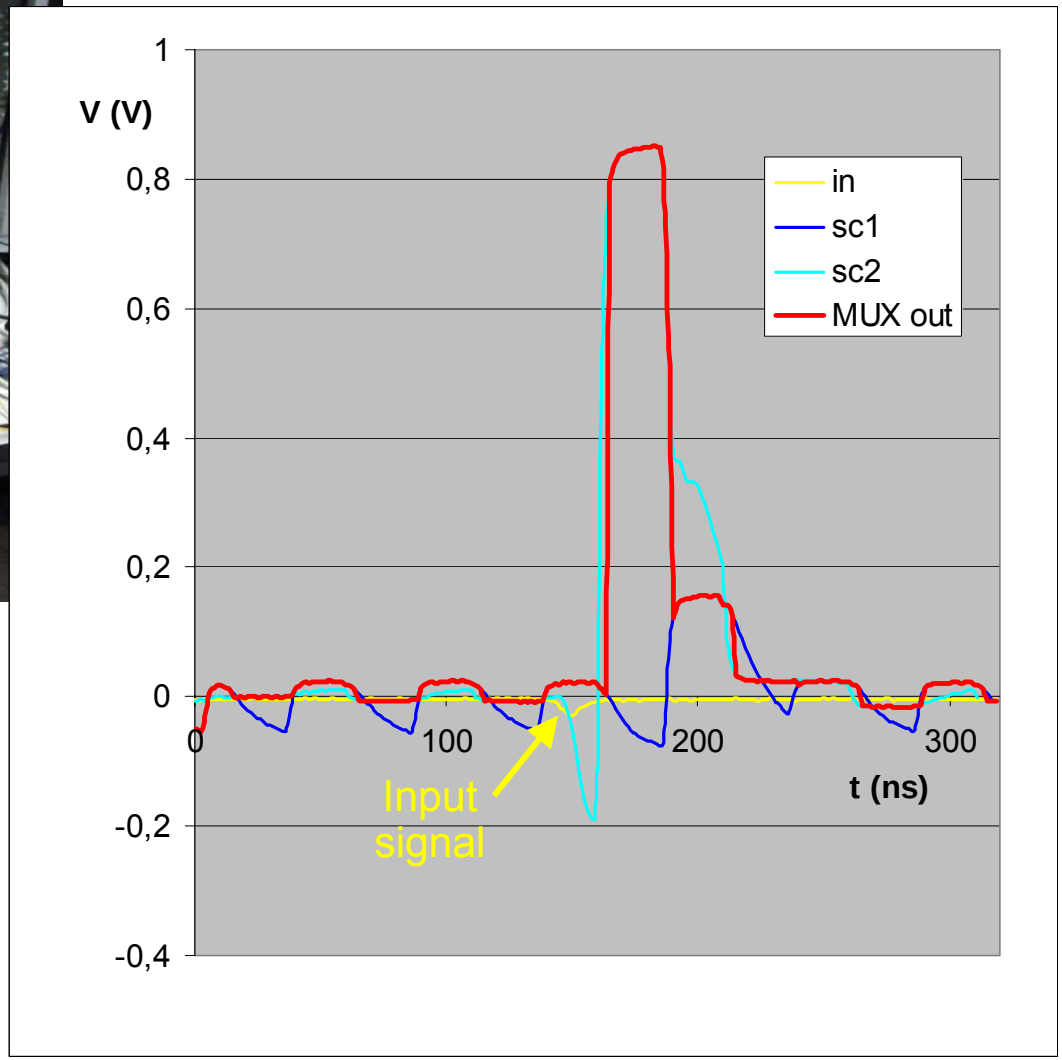
- Purpose: test key points of the circuit
  - Input impedance control by current feedback
  - Low noise performance
  - Dynamic range: Linearity
- Also, to test critical aspects of a switched solution:
  - Offset between subchannels
  - Noise
  - Plateau of the integrator output
    - Effect of the clock jitter versus signal
    - Integrator Rf effect

ICECAL2 Simulations

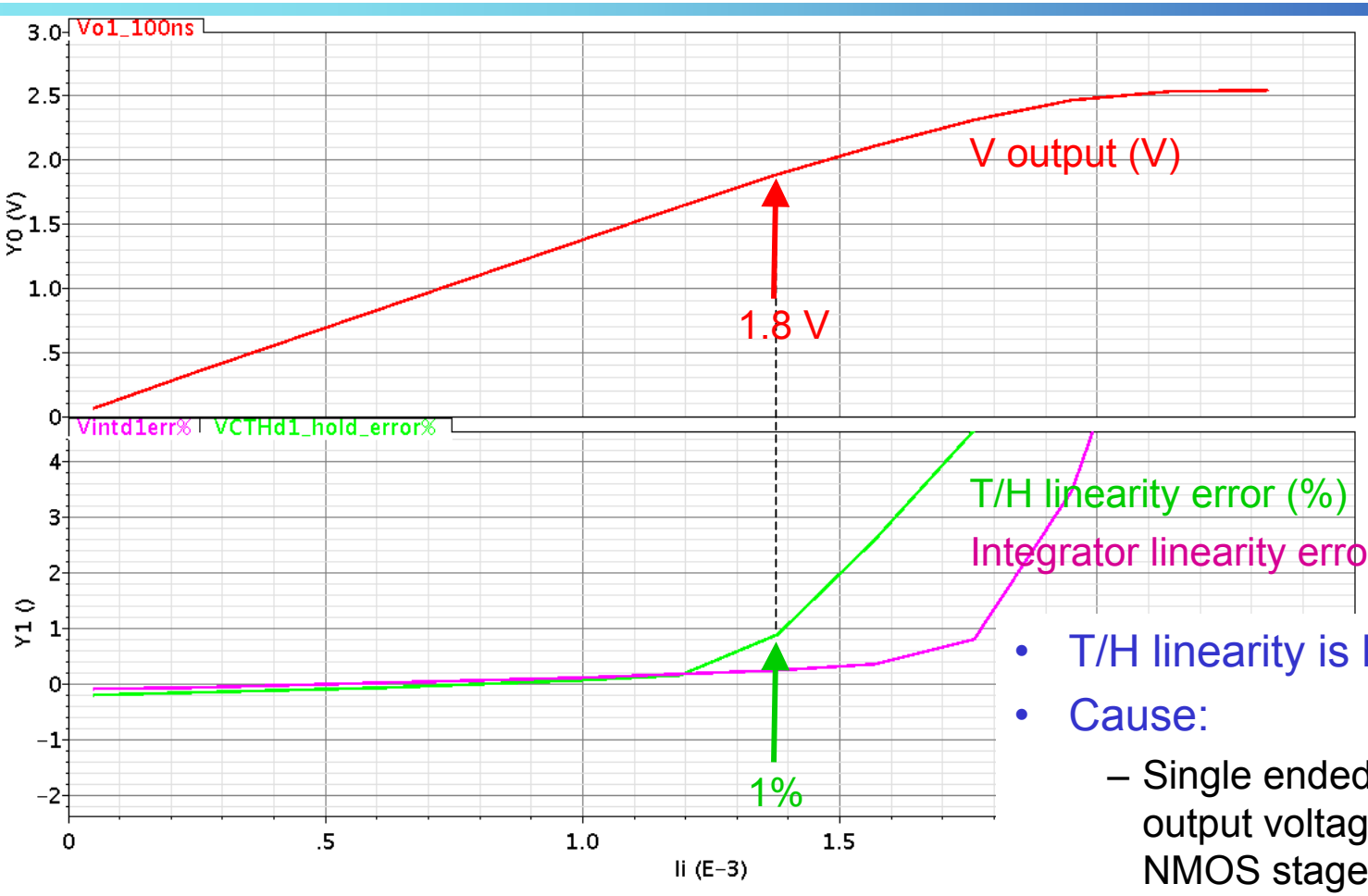


ICECAL2 Preliminary Measurements



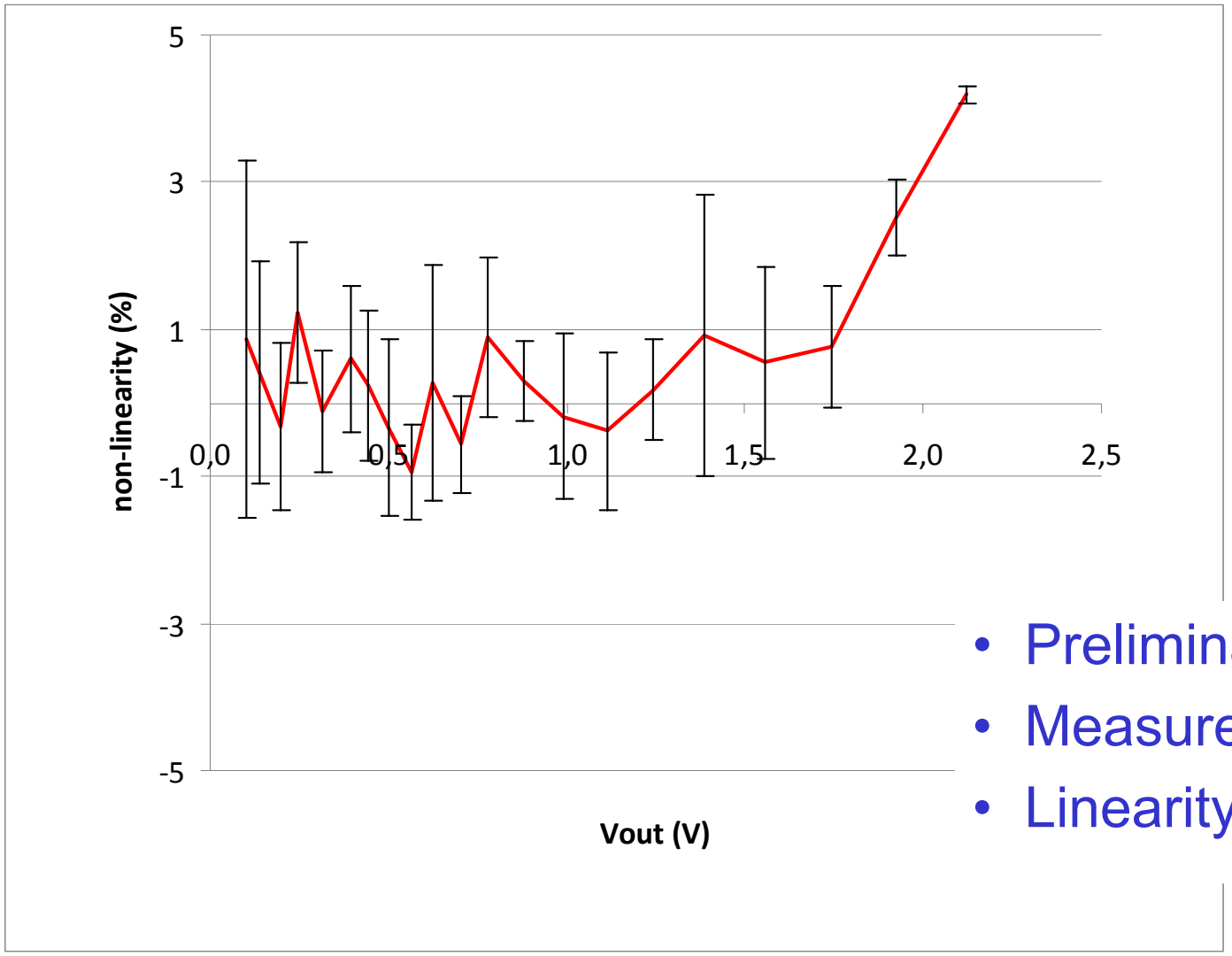


ICECAL2 Linearity Simulations



- T/H linearity is lost at V_{out}~1.8V
- Cause:
  - Single ended limit to maximum output voltage of FDOA at the NMOS stage
- Possible solution:
  - Apply different offset to each pos/neg signal to reduce overall signal excursion

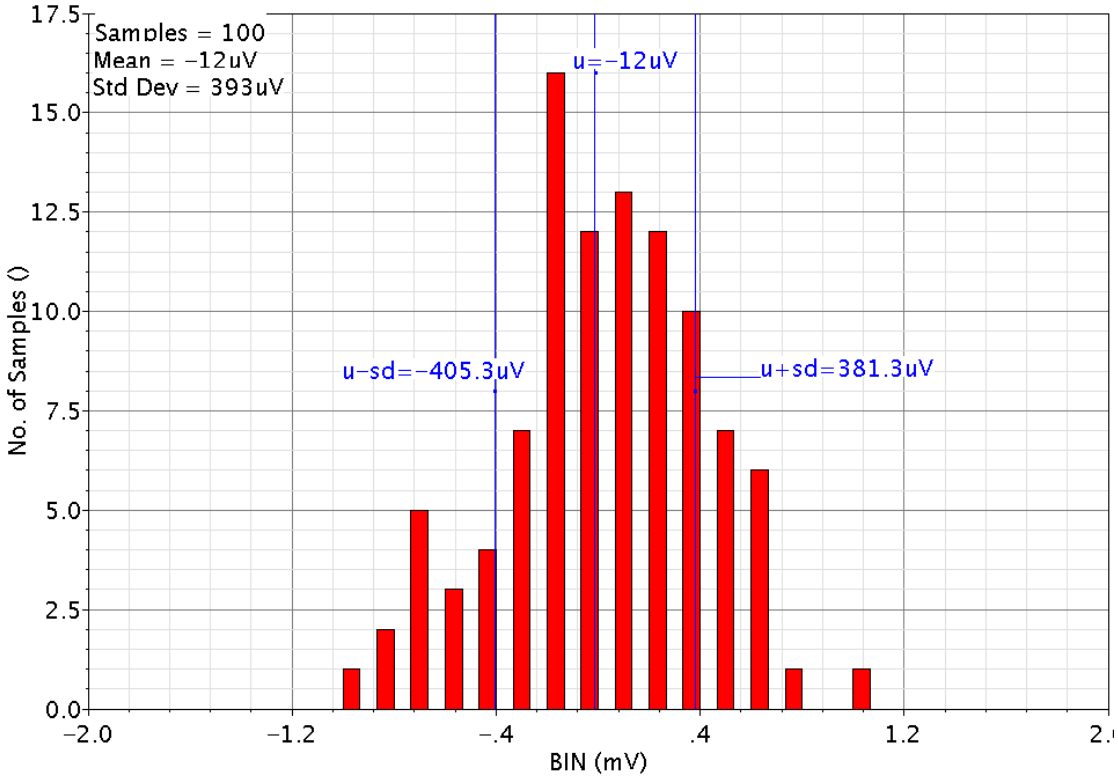
ICECAL2 Preliminary Linearity Measurement



- Preliminary!
- Measurement of 1 chip
- Linearity seems OK

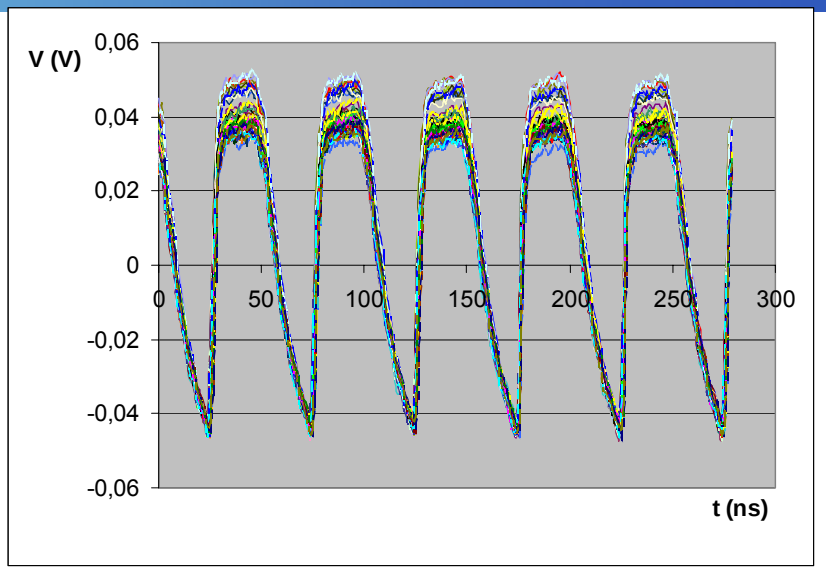
ICECAL2 Noise Simulations

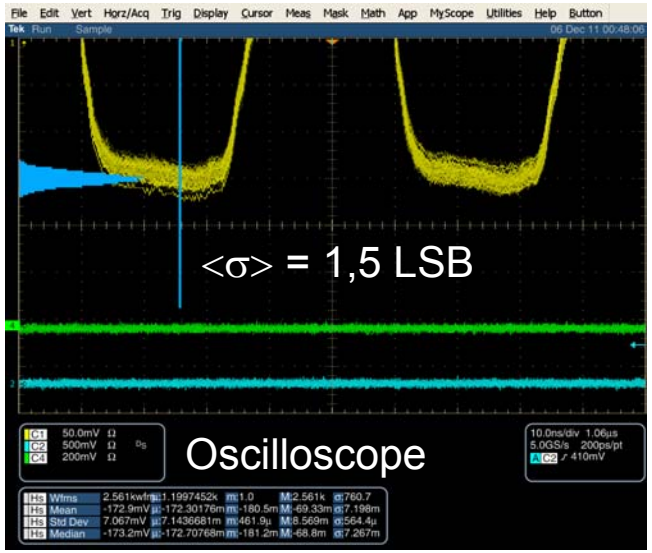
- The noise:
  - Generate a histogram of the voltage value by the end of the cycle (from 100 waveforms).
  - Zero input signal
  - Gaussian fit => standard deviation
  - Noise ≲ 0.8 ADC counts
  - Cable effect not included



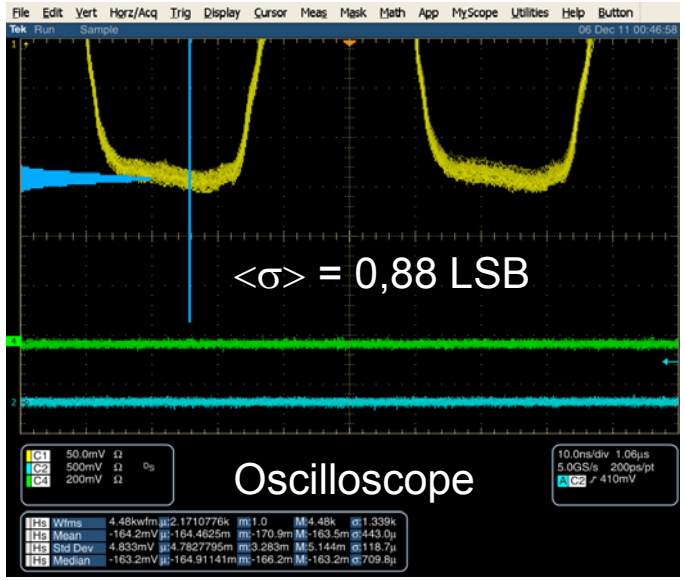
ICECAL2 Noise Measurements

- Setup:
  - includes amp x11.2
  - With/without cable+clipping
  - Oscilloscope: sigma for 1 pt
  - WaveCatcher: sigma for 3 points + CDS



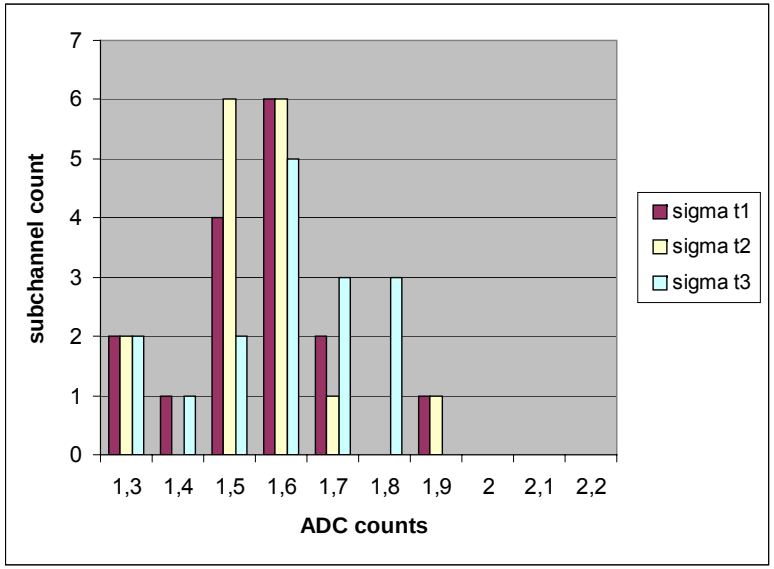


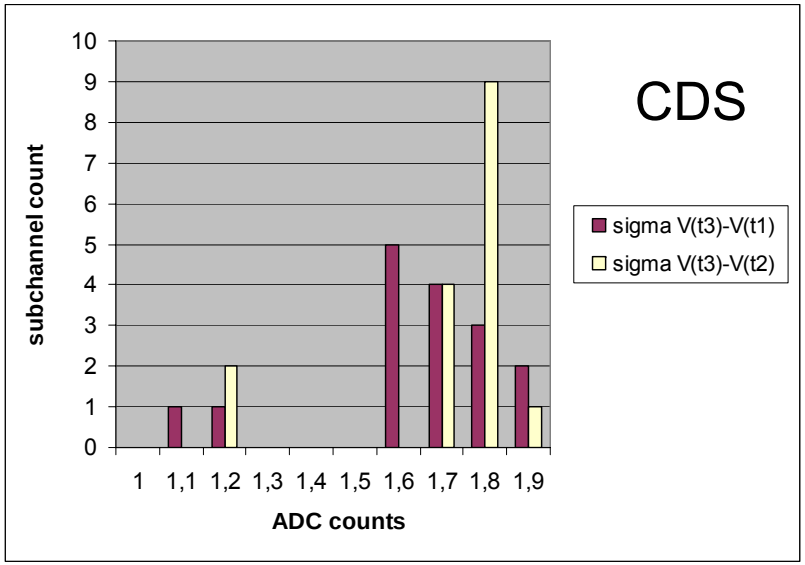
If no cable+clipping



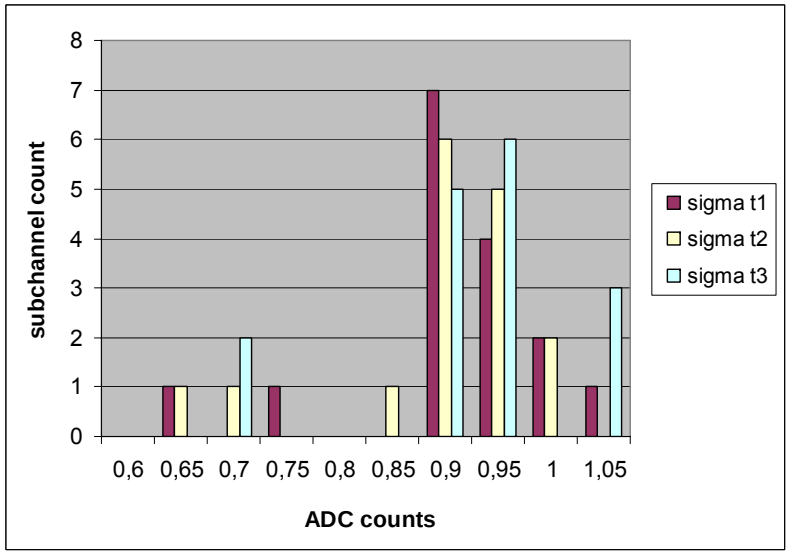
ICECAL2 Noise Measurements

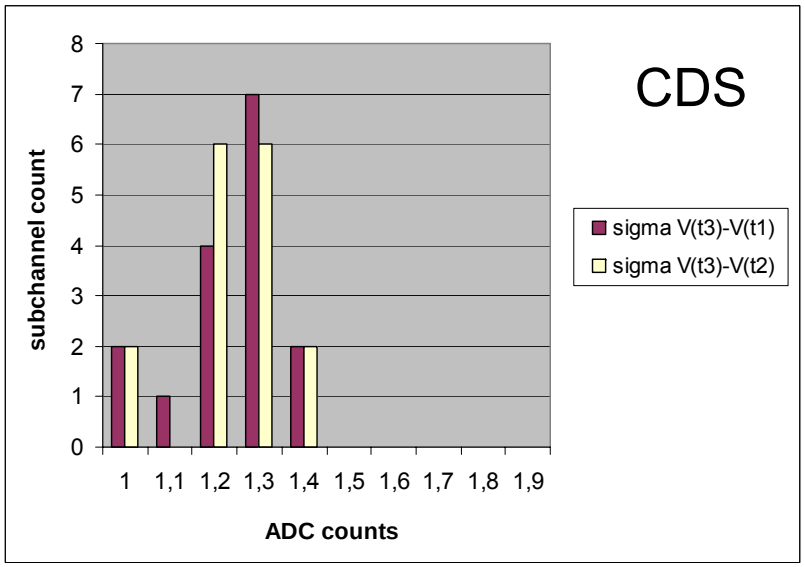
cable+clipping





no cable





Discussion

- Delay chips
  - More than 1 or 2 delay chips per channel
    - 1 for the integrator
    - 1 for the ADC?
  - Only 8 phasers per GBT, maybe some extra phasers can be obtained (extra GBT, CROC…) but anyway it means < 2 per ch!, if more are needed:
    - Re-use existing delay chips
    - Build a new one: no one seems to be planning to do it
    - Integrate 1 phaser/ch in ICECAL
      - Possible if DLL designs done by Dominique's team can be re-used
        - Discuss with Dominique!
        - Any design in AMS 0.35um (either CMOS or BiCMOS) can be reused!
- Slow control interface with GBT-SCA:
  - I2C/JTAG in SCA is 1.5 V CMOS whereas ICECAL I/O is 3.3 V CMOS
    - Design a dedicated pad-level translator
    - Go through FPGA: enough pins? Good I/O bank distribution?

Outlook & plans: short term

- Very short term: finish ICECAL 2 prototype tests before end 2011:
  - Statistic on 10 samples
- Short term: move to common test environment with LAL motherboard **immediately** in 2012
  - New mezzanine for ICECAL V2
  - Develop dedicated CAT software for LAL motherboard:
    - Noise, linearity, time alingment….
  - Test with PMT-base
  - Test with PMT-base + CW base
  - Test with DC-DC converters
    - We have couple of units thanks to G. Blanchot

Outlook & plans: mid term

- Mid term: produce a **final 1 channel chip before end 2012**
  - Main changes
    - Add tunability: input impedance, gain, shaping…
      - Need to decide what's to be tuned and range!
    - Add analog multiplexer and driver
    - Differential LVDS input clock and flip-flop with sync reset (L0-like reset)
    - I2C/JTAG ECS interface
    - **Remarkable deisgn effort: shall start ASAP !!!!**

- ASIC with 1 final channel must be ready by 2013:
  - With beam signal: test beam and/or detector tests
  - But even without beam: study LF pick-up noise immunity, grounding, etc… taking profit of long shutdown in the most realistic scenario: the detector