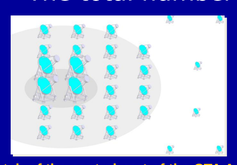
The NECTAr GHz Digitizer ASIC for the Cherenkov Telescope Arrays

D.GASCON[4], E.DELAGNES[1], J.BOLMONT[2], P.CORONA[2], D. DZAHINI [5] ,F.FEINSTEIN[3], J.F. GLICENSTEIN[1],C.L.NAUMANN[2], P.NAYMAN[2], F. RARBI[5],M.RIBO[4], A.SANUY[4], X.SIERO[4], J.-P.TAVERNET[2], F.TOUSSENEL[2], P.VINCENT[2] AND S. VOROBIOV[3]

Contact:
eric.delagnes@cea.fr

Electronics for future Atmospheric Cherenkov Telescope Arrays

The future international very high energy gamma ray observatory, the Cherenkov telescope Array (**CTA**), will consist of an array of 50-100 dishes of various sizes. Each telescope will have a camera with photo-detectors installed in its focal plane and the associated front-end electronics to capture the Cherenkov Light associated with the particle showers produced by gammas photons in the atmosphere. The total number of electronic channels will be larger than 100000.



Sketch of the central part of the CTA Array

The electronics has to be:
-modular (easy replacement of components)
-low cost: goal 300 Euros/channel
-reliable
-easy to calibrate

Main Requirements for the FE Electronics

- short signal ~ 5 ns. Night sky background rate ~ 100 MHz
- short read-out window (5-10 ns) to optimize S/N
- bandwidth in the 200-400 MHz range
- sampling rate S >> 2 Bw to allow proper signal reconstruction
- pixel time resolution < 2 ns
- dynamic range ≥ 14 bits (with single P.E measurement)
- dead time < 5% (< 5 μs for a 10 kHz trigger rate)

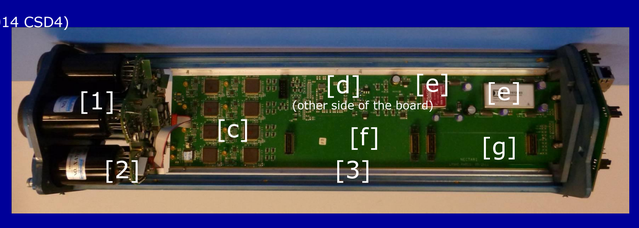
ELECTRONICS BASED ON ULTRAFAST ANALOGUE MEMORIES IS A PROVEN LOW COST SOLUTION FOR THESE REQUIREMENTS (on HESS, HESS-2 [R1] & MAGIC)

The NECTAr Project

Project (Supported by French National Research Agency (ANR-08-BLAN-0014 CSD4)

Development of a camera module reading 7 pixels includes:.
- Photomultipliers [1]
- PMT HV supply and control board [2]
- A single readout/control FE board with ETHERNET link [3]

Everything POWERED BY A SINGLE 12V DC power supply

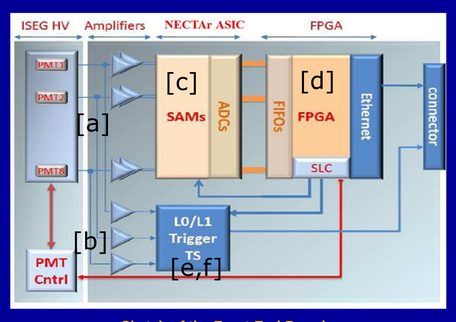


Photography of the NECTAR cluster Protoype

The Front End Board

Front-end board is based on the use of new NECTAR analogue memory and digitizer ASIC

Main components of the front end board:
- 8 dual-channel NECTAr chips [c] (7 used only)
- Level 0 (board level) [e] and Level 1 (camera level) [f] trigger mezzanines
- Altera low cost FPGA [d] for:
  - Control: HV board, NECTAr ASIC, Level 0, Level 1 mezzanines
  - Buffer for the trigged events
  - Calculation (total charge of pixels, timing,…)
  - Communication and transfer (Ethernet with UDP protocol, 1 Gbit/s)
- DC-DC converters to provide the low voltage supplies of the chips [e]

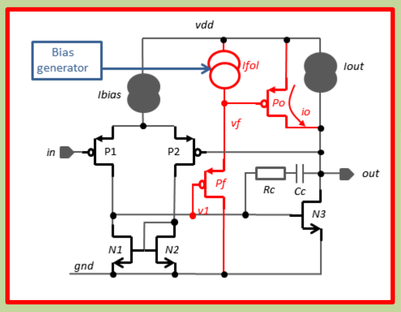


Sketch of the Front-End Board

Operation of the front-end board:
- The signal is amplified, then split into a main path [a] and a trigger path [b].
- The trigger is analogue (with comparators). Mezzanines designed by the CTA collaboration allows to test various trigger algorithms (majority, analogue sum..) [f,g]
- In the main path, the signals are amplified with 2 different gains (high HG and low LG) to achieve the required dynamical range.
- The data are stored inside the analogue memory of the NECTAr ASICs.
- At trigger time, the data are digitized and sent to a FIFO in the Altera FPGA, then to a computer farm by Ethernet.

Tests on the NECTAR0 ASIC prototype have been performed on a prototype of this board

The NECTAR input buffers



Principle of the new slew rate enhanced input buffers

From SAM [R1] to NECTAR: capacitance driven by the input buffers ensuring a high chip impedance is multiplied by 4:
=> New class AB input buffer with high slew rate (>1V/ns) for a moderate static power consumption developed .(design Univ. Barcelona / IRFU)

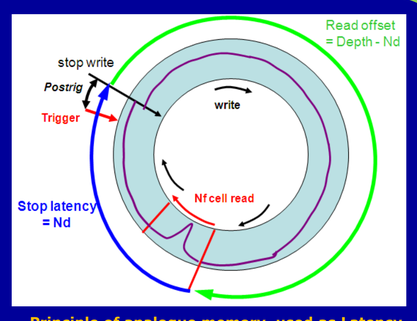
On a falling edge at input: high slewrate ensured by N3.
On a rising edge at input:
- The drain voltage of P1 (v1) decreases,.
- Pf acts as a voltage follower: vf follows v1 with an offset
- => P0 drain current (i0) is drastically increased
- => the current sourced by the output branch normally limited by Iout is boosted => the slew rate is increased

The very low quiescent drain current of Po is controlled by its DC gate voltage. This voltage is adjustable by the gate-source voltage of Pf which is adjustable by the current Ifol. Ifol is set by a bias generator using a servo-control loop based on a replica of the amplifier.

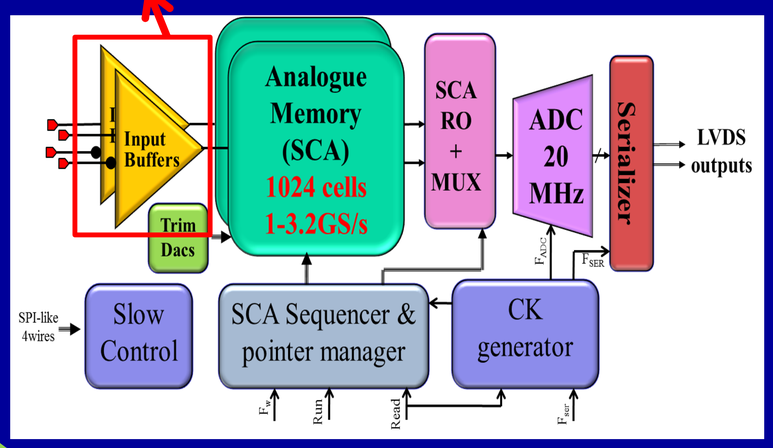
NECTAr0: prototype of the digitizer ASIC

NECTAR0, designed in AMS CMOS 0.35μm technology, integrates:

- **2 fully differential channels** of switch capacitor array analogue memory (SCA)
  - **Sampling DLL Matrix** structure: Extended Version of SAM (HESS2) [1]
  - Programmable sampling frequency (500 to 3.2GS/s)
  - Circular L1 (programmable) latency buffer
  - **1024-cell depth** = up to 500ns latency @ 2GS/s, 2μs @ 0.5GS/s
  - **Region of Interest (ROI) readout** with programmable length (typically Nf=16 cells)
  - Pedestal spread corrected on chip by trim DACs calibrated once for all
    ⇒ Digitized Data directly usable for calculations.
- **1 Pipeline ADC** digitizing the 2 SCA channels data after multiplexing:
  - IP block from LPSC [R2]
  - **12bit 20 MSample/s**
- A configurable 240Mbit/s serial link (2,3 or 4 LVDS links) compatible with a low cost FPGA



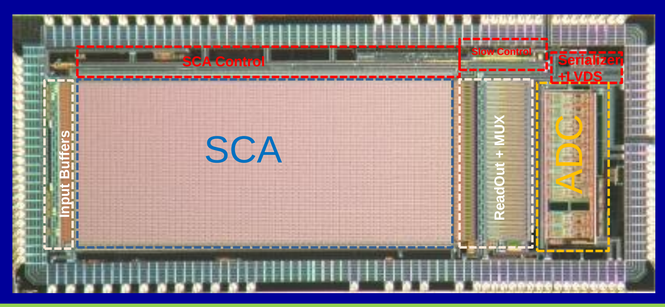
Principle of analogue memory used as Latency buffer with ROI readout



Architecture of the NECTAr0 chip

Power pulsing capability to reduce power consumption:
- Readout part + ADC are off during sampling phase
- Write amplifiers are off during readout

QF128 14mmx14mm
0.4mm pitch package
(real size picture)

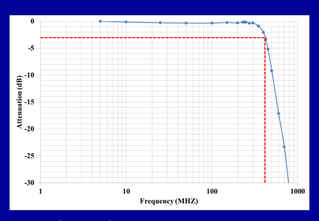


Photography of the NECTAR chip
21mm² die
AMS CMOS 0.35μm

NECTAr0: measured performances on the prototype Front End Board

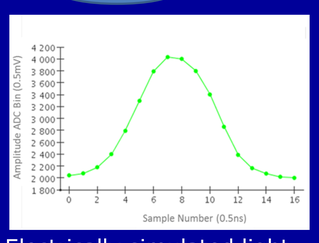
Power consumption

=210mW (10% of the total power consumption for a camera channel).
Can be decreased (with penalty on BW & INL)



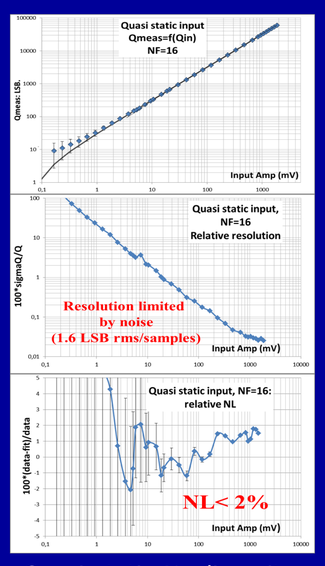
NECTAr0 Frequency response (0.8V peak-peak sine wave input)
⇒ Smooth response, no ringing,
400 MHz -3dB Bandwidth

Reference Pulse Shape for electrical characterization



Electrically simulated light pulse (2.4ns FWHM), half dynamic range) acquired by Nectar @2 GS/s
Fast response, smooth, no ringing.

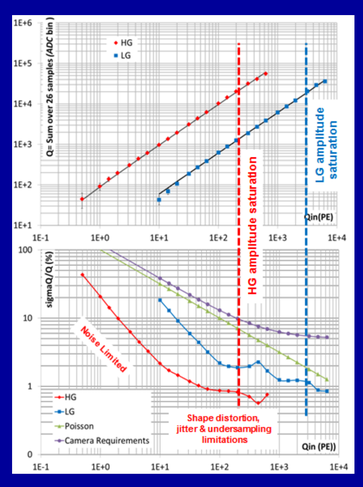
Charge (Q) is calculated only by the FPGA as the sum of Nf samples



Quasi static Nonlinearity & resolution scan for Q (sum of 16 samples @ 1Gs on the flat top of a 50ns long pulse).

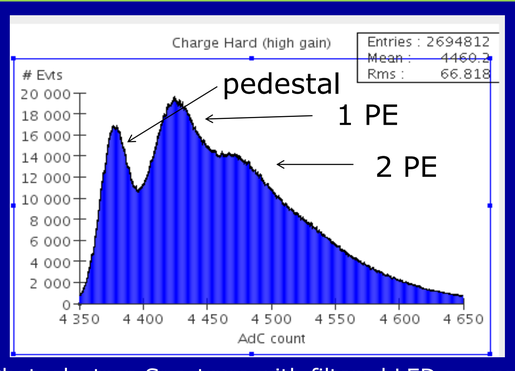
Charge resolution is dominated by noise (0.8mV rms)

Electrical PE = PE signal delivered by a PMT with 2.10⁵ Gain.
BiGain configuration (1,16)
=>0.7mV amplitude on LG
=>11.2mV amplitude on HG

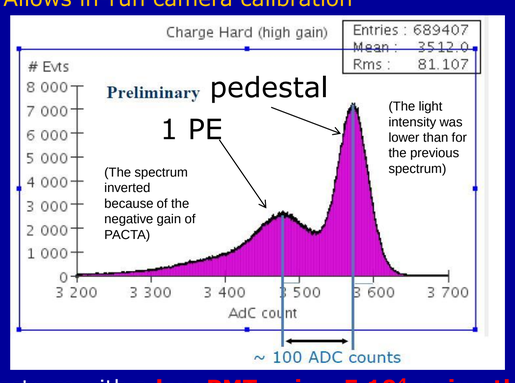


Linearity & Q resolution with electrically simulated PE pulses, 2GS/s, Nf=26 (13ns Window):

- Usable Range > 6000 PE with resolution of 20% for 1 PE
- INL< 3%
- Q resolution far better than fluctuations of Poisson statistics (and requirements)
- Similar results @ 1GS/s



Photoelectron Spectrum with filtered LED source. Hamamatsu R8619mod PMT (2 10⁵ gain), 1GS/s, 13ns Integration Window
- 1 PE peak – baseline =50 ADC count as expected
- Low noise: σ on Baseline = 25% PE.
- Good (1.9) Peak-to-Valley Ratio.
- Allows in-run camera calibration



Spectrum with a **low PMT gain= 5 10⁴ using the PACTA** transimpedance amplifier **[R3]** designed by Barcelona located on the PMT base (gain ~ -35) and with on-board HG decreased to 4 (should be 2 to have the same overall gain than in previous tests). 1GS/s, 13ns integration window .
- 1 PE peak is located @ 100 ADC count as expected.
- σ on Baseline = 25% PE.
- Allows in-run camera calibration

	NECTAr0 Features or Performance	Requirements	Unit
Number of Channels	2		Differential channels
Memory depth	1024		Cells
Power Consumption	< 210	<300	mW
Sampling Freq. Range	0.5 - 3.2	0.5-2	GS/s
Analogue Bandwidth	400	>300	MHz
Read Out deadtime time for an event (2 gains 16 cells)	2	2	μs
Deadtime @ 10 kHz trigger rate	<2%	<5%	
ADC LSB	0.5	0.5	mV
Total noise (unchanged with frequency)	< 0.8	<0.8	mV rms
Maximum signal (limited by ADC range)	2	2	V
Dynamic Range	>11.3	> 11	bits
Crosstalk	4	5	per mil
Relative non linearity (integral)	<3%	<3	%
Sampling Jitter	< 40 (from Q resolution)	<50	ps rms

NECTAR0 already fulfils the main requirements of the CTA Cameras and is usable as it is:

Next Steps:
⇒ full module characterization.
⇒ Study of a new chip prototype (more channels, longer depth, integrated programmable gain input amplifiers)

[R1] Delagnes E. et al., NIM-A 567 (2006), 21-26
[R2] Rarbi F. et al. IEEE ICICDT Proceedings, Grenoble (2008), 135-138
[R3] Gascon D., Sanuy A., talk given at this conference (TWEPP 2011)

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