# KLauS - A Silicon Photomultiplier Readout ASIC

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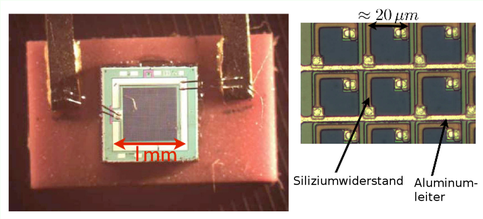
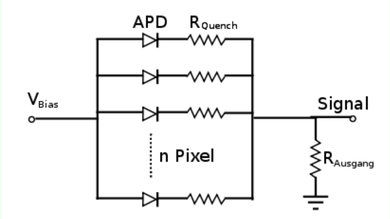
## Silicon Photomultiplier (SiPM)

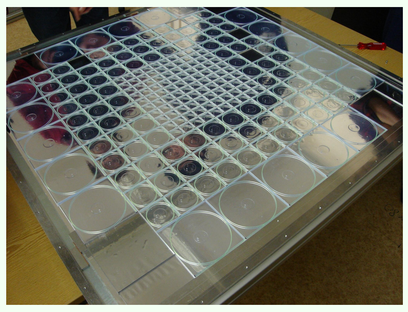


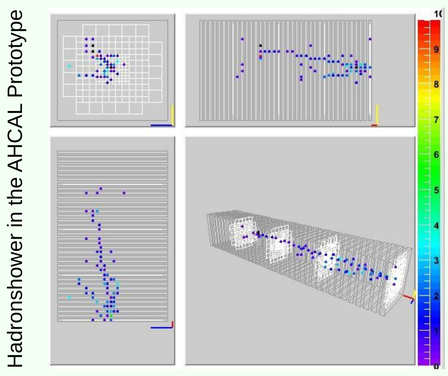




Novel photo detectors:

- High gain ≈ $10^5$ to $10^6$
- Compact design possible
- Low operating voltage ( < 100 V )
- Insensitive to magnetic fields
- Optical crosstalk
- Large temperature dependence
- High dark rate ≈ $10^5$ to $10^6$ Hz

## Silicon Photomultipliers in Calorimetry Applications


CALICE AHCAL Prototype


Hadronshower in the AHCAL Prototype

SiPMs are well suited for the installation inside a calorimeter.

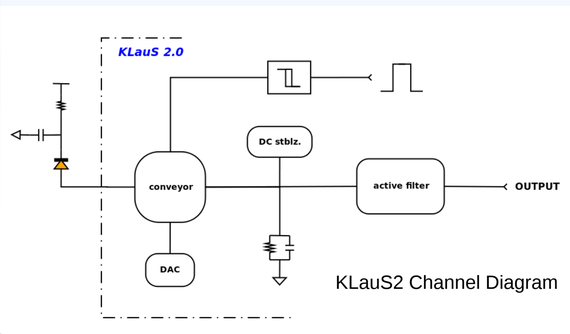
Small size allows to build detectors with high granularity.

Challenges:

| | | |
|---|---|---|
| Energy measurement | → | High dynamic range > 200 pC |
| Precise signal timing | → | Low trigger jitter < 1 ns time resolution |
| Large number of channels | → | Low power consumption < 40μW/channel |
| SiPM variations | → | Tuneable bias voltage |

→ Dedicated readout electronics required

## KLauS2 Overview



KLauS2 Channel Diagram

- Low impedance input stage duplicates input signal current
- DAC allows to control input terminal voltage for bias tuning and temperature compensation
- Discriminator generates precise trigger signals for thresholds corresponding to single or multiple pixels
- Signal charge is integrated by a passive integration unit with DC pedestal stabilization
- Active filter generates output without undershoot using shaping times of 25ns, 50ns or 100ns
- Input stage supports power gating to reduce power consumption
- 12 channels developed in SiGe 0.35μm technology, submitted in Nov. 2010
- Input stage planned to be integrated in the next SPIROC version

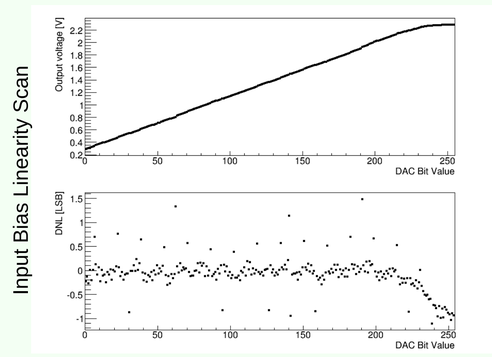
## SiPM Bias Voltage DAC

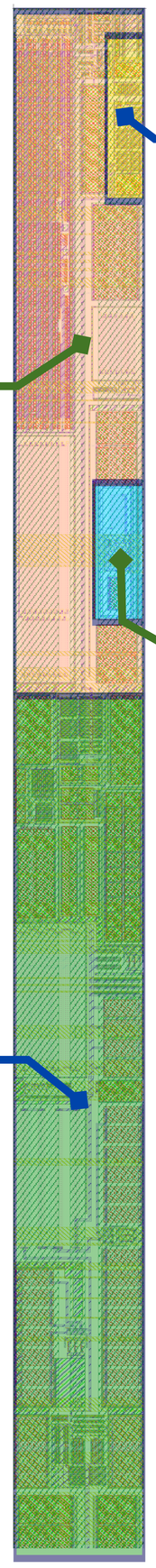
Bias tuning allows for compensation of breakdown voltage variations due to temperature or production fluctuations

Full scale range: ~2V

Linear range: > 1.8 V

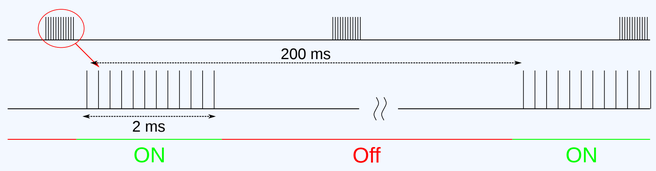
Temperature variations of 36°C can be compensated

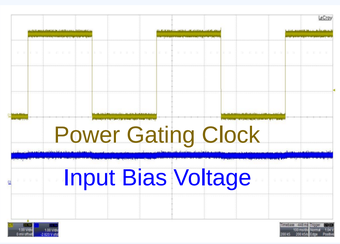


## Power Reduction

Design provides low power consumption < 2.5mW/channel
Use periods between events to put the channel in an idle state and save power



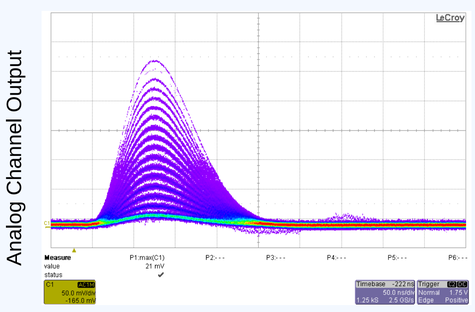



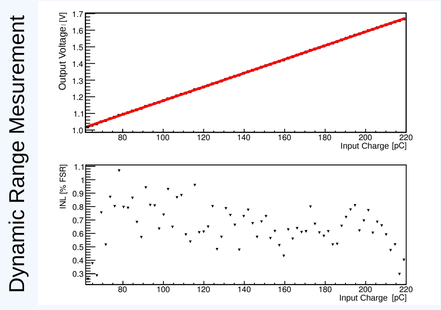

SiPM Bias variation during on/off cycle < 20mV
With 1% duty cycle power gating reduces the power consumption to 25 μW/channel

## Analog Signal Processing

Signal processing for charge measurement

- Passive integration reduces power consumption
- Active filter for undershoot cancellation and different signal shaping times

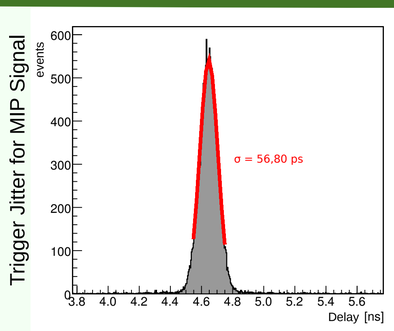


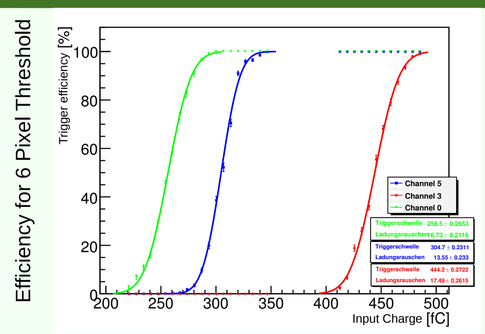




Signal to Noise Ratio > 10 for 40fC input charge

Dynamic Range: 40fC to 220pC with INL < 2.1% for all chip configurations

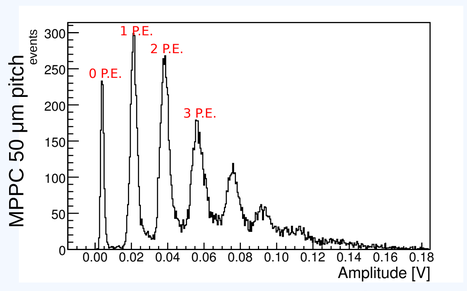
## Low Jitter Trigger Signal

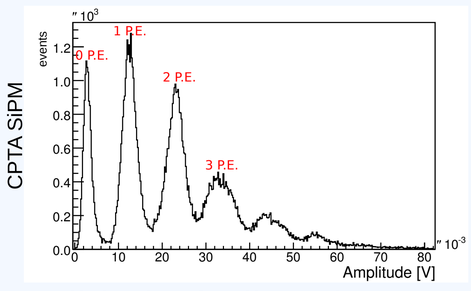



Measurement with charge injection, signal rising time: 5ns
Jitter for MIP signals (15 pixels, SiPM gain: $2.75 \times 10^5$) < 60 ps
Threshold variations due to PCB design, charge noise < 18fC

## SiPM Measurements




Readout of various SiPM sensors possible including detectors with a dark rate up to several MHz

## Contact

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