Arm2 Silicon status

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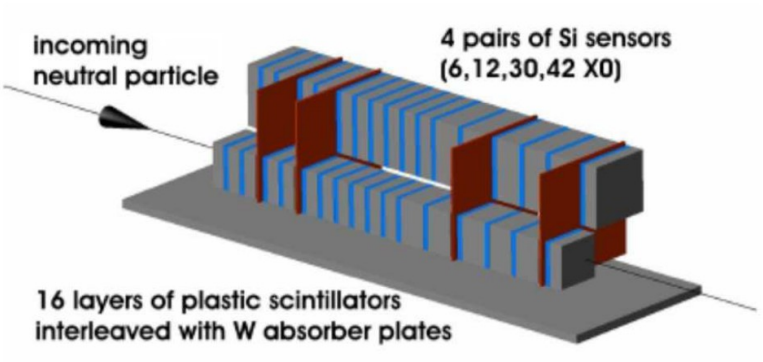
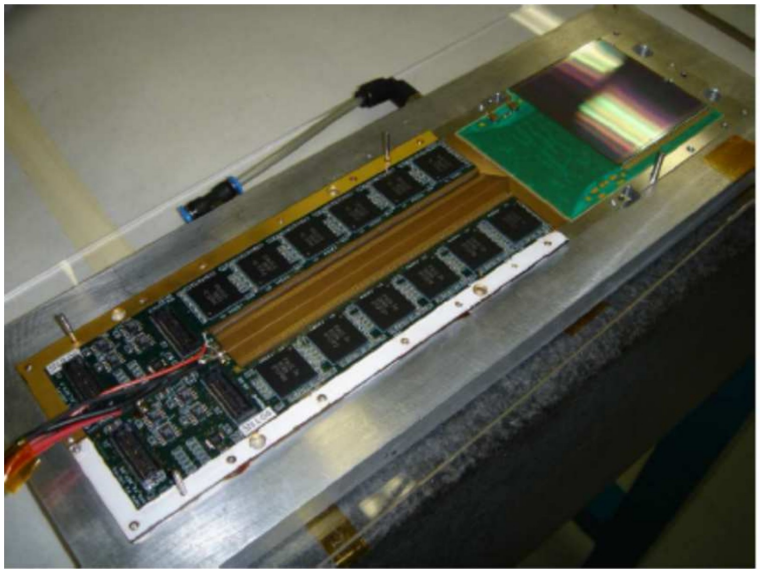
Outline

- The upgraded Arm2 silicon electronic readout
  - Overall scheme
  - The DAQ boards
  - The front-end PACE3 chip
- Results from test-beams and 2022 operation
- PACE3 linearity and calibration

The Arm2 Calorimeter

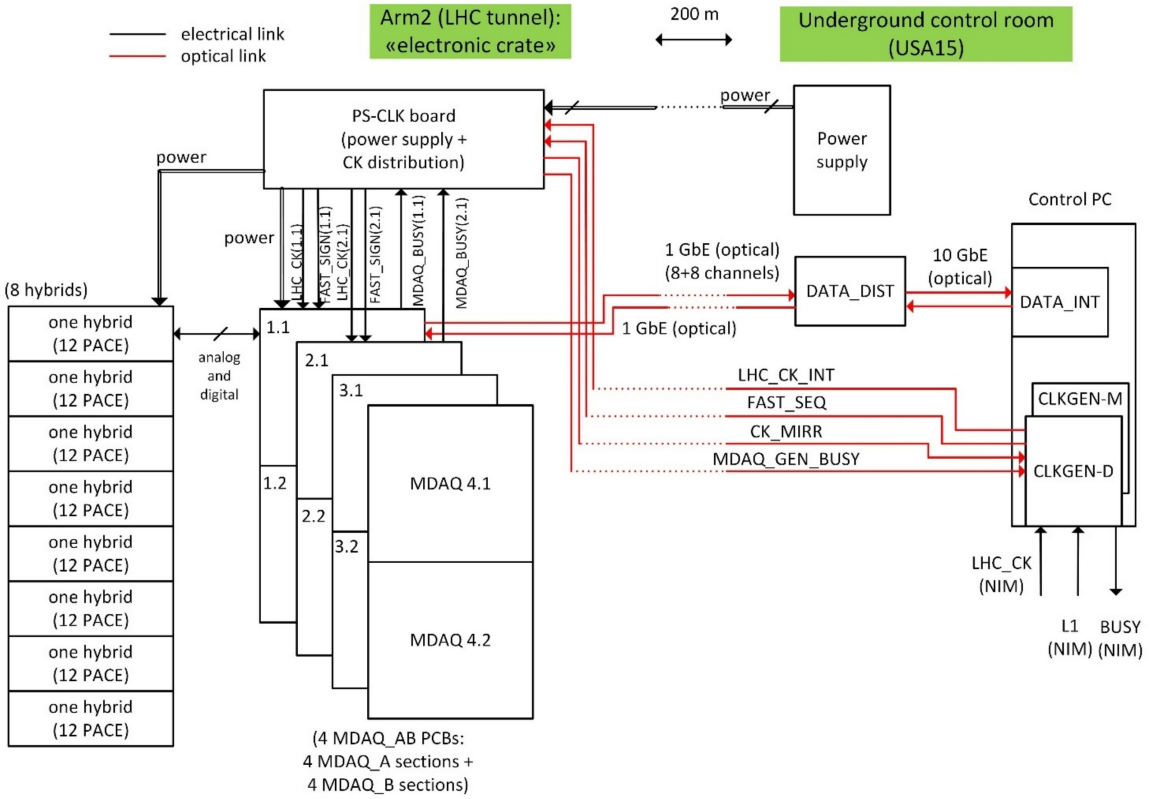
Arm2 calorimeter: contains 4 pairs of Si microstrip sensor planes (1 pair = 1 Si detector module)



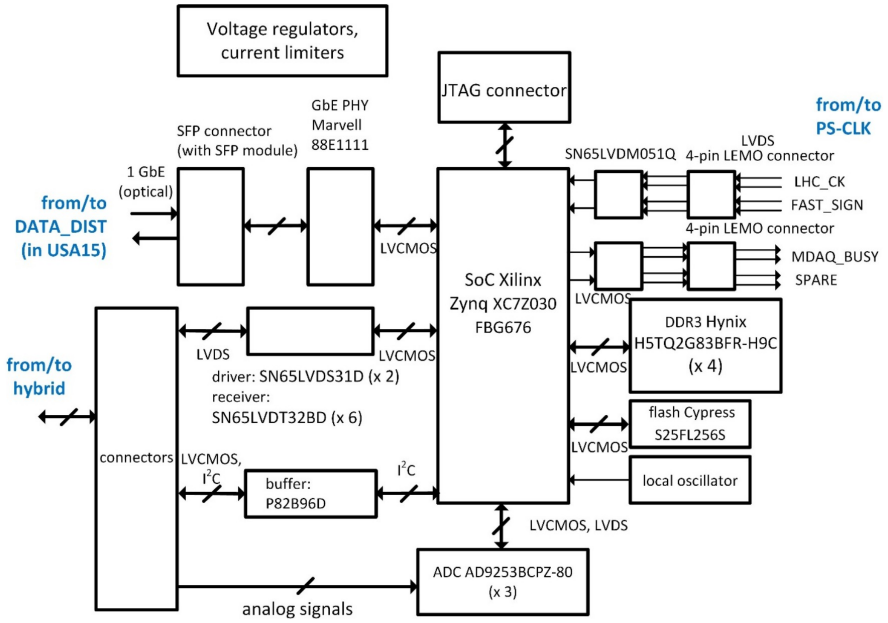


Top side of a Si detector module, showing one Si sensor plane and the corresponding 12 front-end PACE3 chips

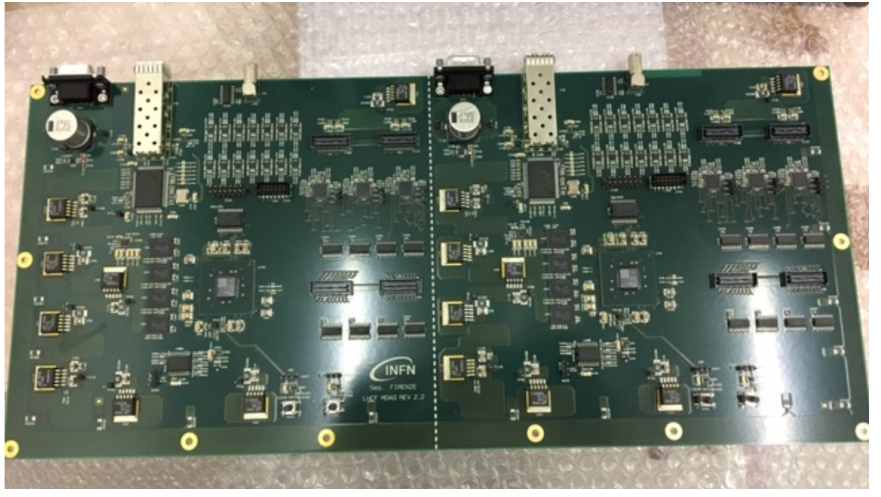
Arm2 Si electronics overall scheme



The MDAQ board

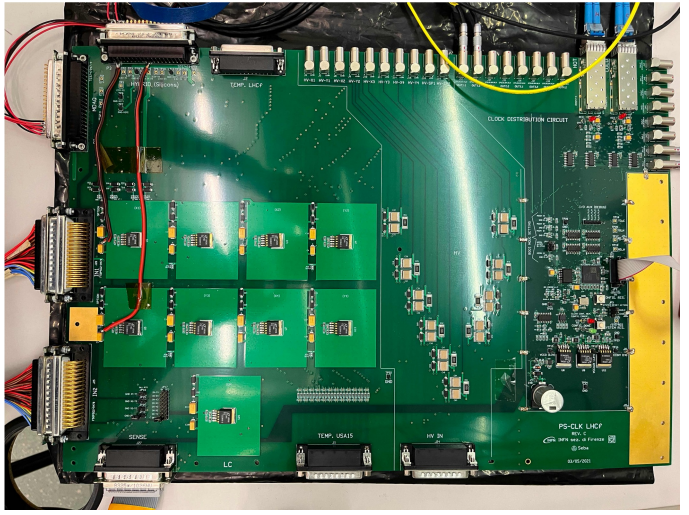


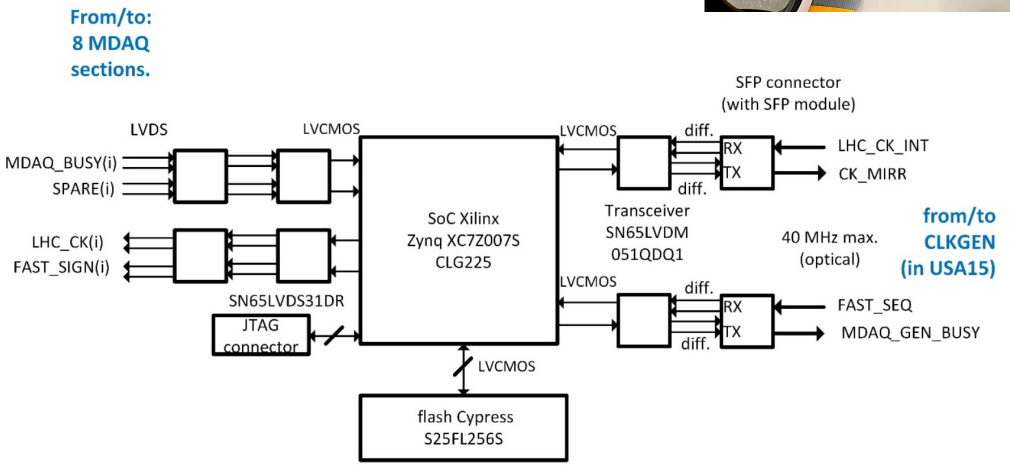
- Zynq XC7Z030 SoC (FPGA + Arm microprocessor)
- 4 GB DDR3 RAM
- Ethernet PHY
- TCP/IP stack implemented in Arm for ethernet connection
- ADC interface (AD9253, quad 14 bit)



The PS-CLK board

- Distributes power supply:
  - LV for hybrids (regulators on boards)
  - LV for MDAQ boards
  - HV for silicon detectors
- Distributes clock signals and fast commands
- Generates busy signal

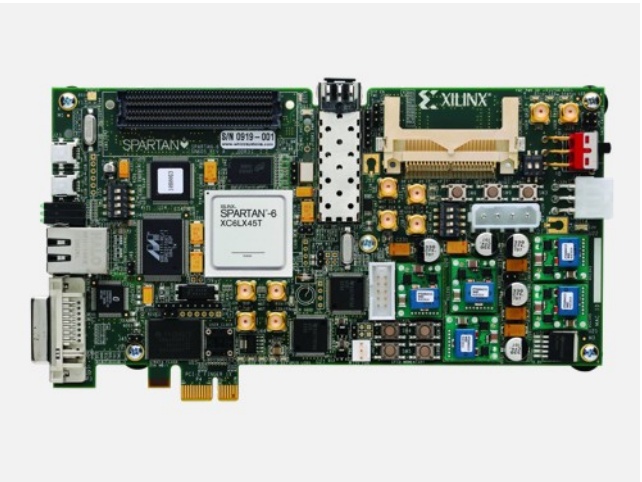




The CLKGEN board

CLKGEN-M

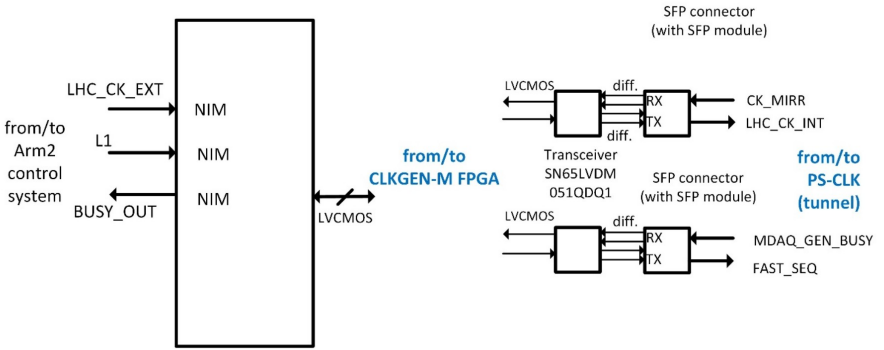
Xilinx Spartan6 evaluation board with PCIe connectivity

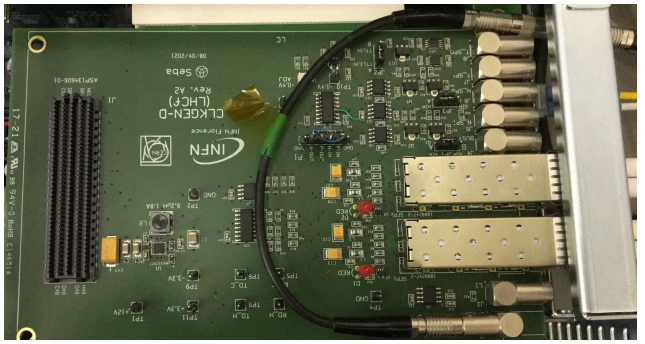


Low latency through custom pcie driver

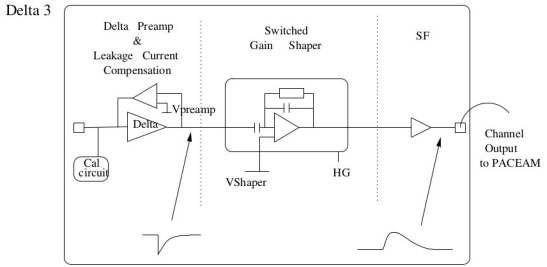
CLKGEN-D

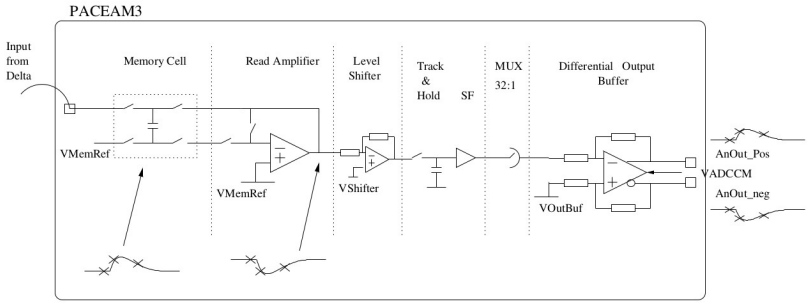
Custom “mezzanine” board

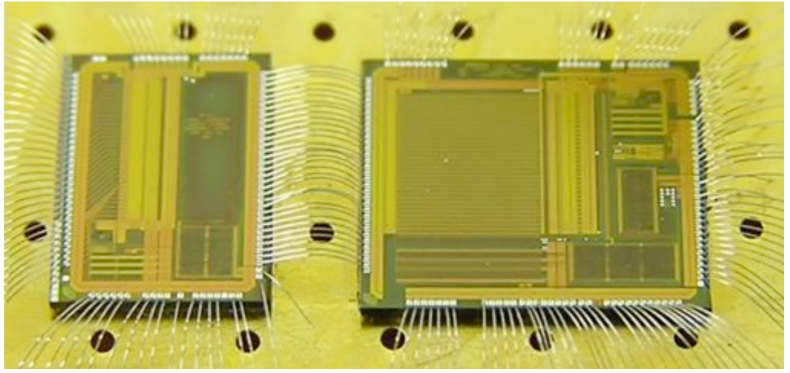




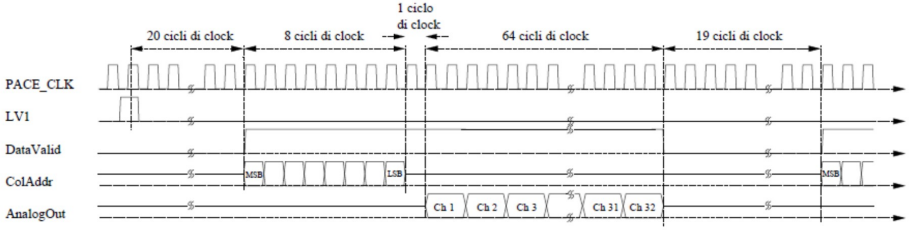
The PACE3 chip

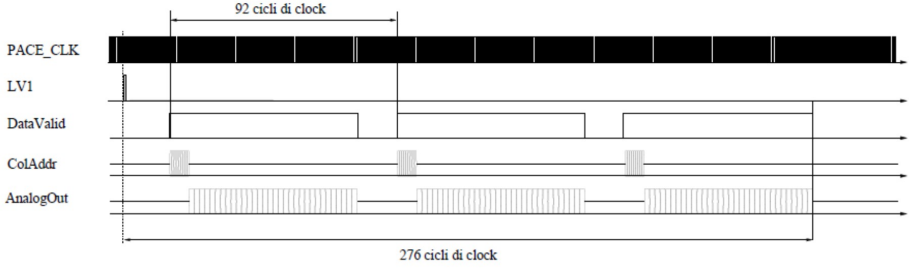






- 32 channel with charge pre-amp + shaper
- 192 cells pipeline analog memory
- I2C interface for slow control
- Analog signals sampled with LHC clock
- For each L1 trigger 3 consecutive samples are sent out
- The depth in the analog memory is set by the latency parameter





Internal registers

I2C over ethernet

Delta I2Cslave address 125

Delta Reg. Name	Sleep setting	Sleep value	Reg. Add.	Reg type
Cont.Reg⟨0⟩	0000 0000		0	W/R
Cont.Reg⟨1⟩	0000 0000		1	W/R
ChipID⟨0⟩			2	RO
ChipID⟨1⟩			3	RO
CalChan⟨0⟩	0000 0000		4	W/R
CalChan⟨1⟩	0000 0000		5	W/R
CalChan⟨2⟩	0000 0000		6	W/R
CalChan⟨3⟩	0000 0000		7	W/R
VCal	1000 0000	$\sim 1V$	8	W/R
VoPreamp	1000 0000	$\sim 1V$	9	W/R
VoShaper	1000 0000	$\sim 1V$	10	W/R
VSpare	1000 0000	$\sim 1V$	11	W/R
IPreamp	0000 0001	$\sim 1\mu A$	12	W/R
IShaper	0000 0001	$\sim 1\mu A$	13	W/R
ISF	0000 0001	$\sim 1\mu A$	14	W/R
ISpare	0000 0001	$\sim 1\mu A$	15	W/R

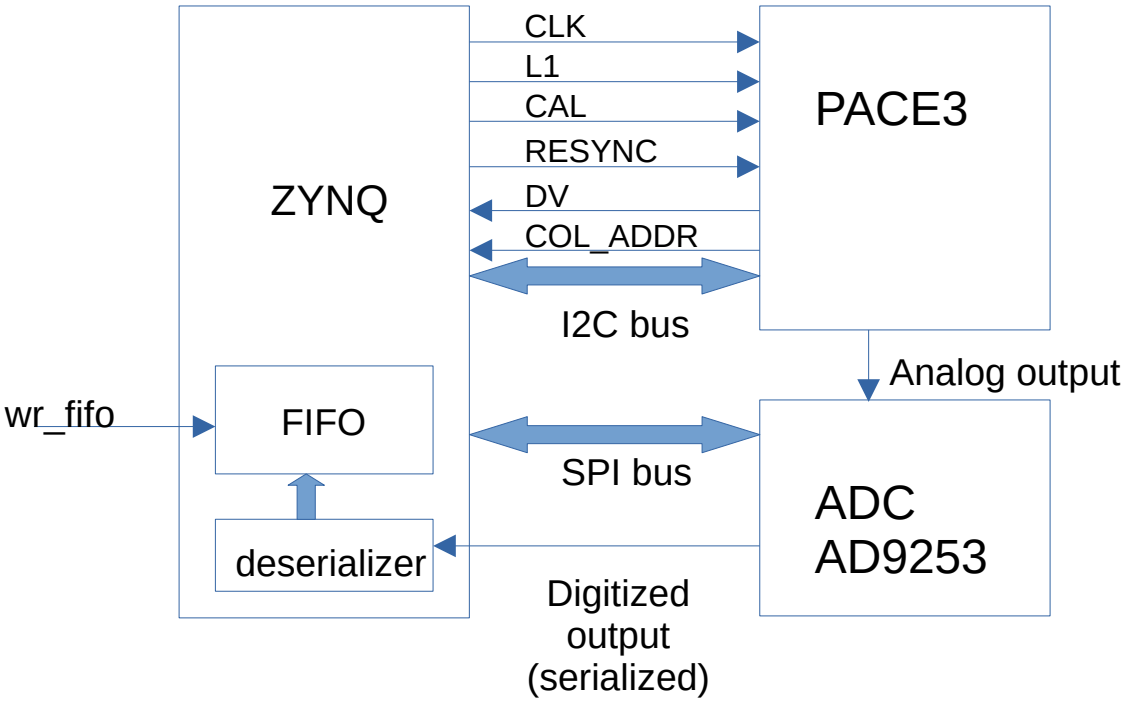
Table 12: The Delta Register Sleep settings

PACE AM I2C slave address 127

PACE-AM Reg. Name	Sleep setting	Sleep value	Reg. Add.	Reg type
Cont.Reg.	0000 0000		0	W/R
Lat	1000 0000		1	W/R
ChipID⟨0⟩			2	RO
ChipID⟨1⟩			3	RO
VMemRef	0000 0001	$\sim 10mV$	4	W/R
VShift	1000 0000	$\sim 1V$	5	W/R
VOutBuf	1000 0000	$\sim 1V$	6	W/R
IReadAmp	0000 0001	$\sim 1\mu A$	7	W/R
IShift	0000 0001	$\sim 1\mu A$	8	W/R
IMuxBuf	0000 0001	$\sim 1\mu A$	9	W/R
IOutBuf	0000 0001	$\sim 1\mu A$	10	W/R
ISpare	0000 0001	$\sim 1\mu A$	11	W/R
UpsetReg.	0000 0000		12	R

Table 17: The PACE-AM Register Sleep settings

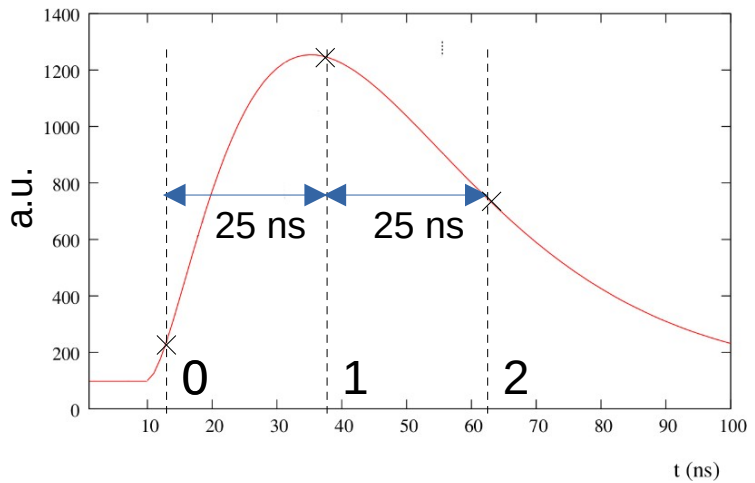
Interface with ZYNQ device



- Data valid and column address signals are checked for consistency in the FPGA logic, errors are embedded in the event data
- The wr_fifo signal is set by considering the additional delay introduced in the AD conversion

Latency considerations

- “coarse latency” in steps of 25 ns: parameter set in the latency PACE register. To compensate the delay between the crossing of the particle and the L1 trigger arriving to the chip.

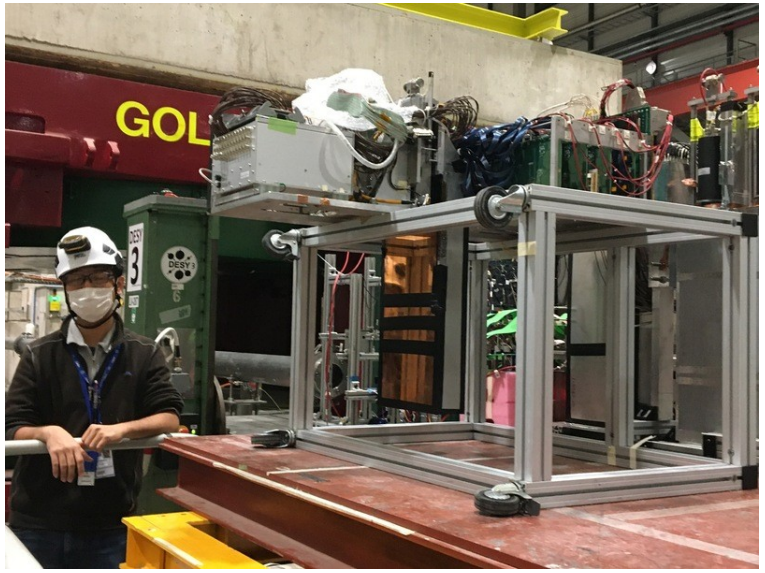


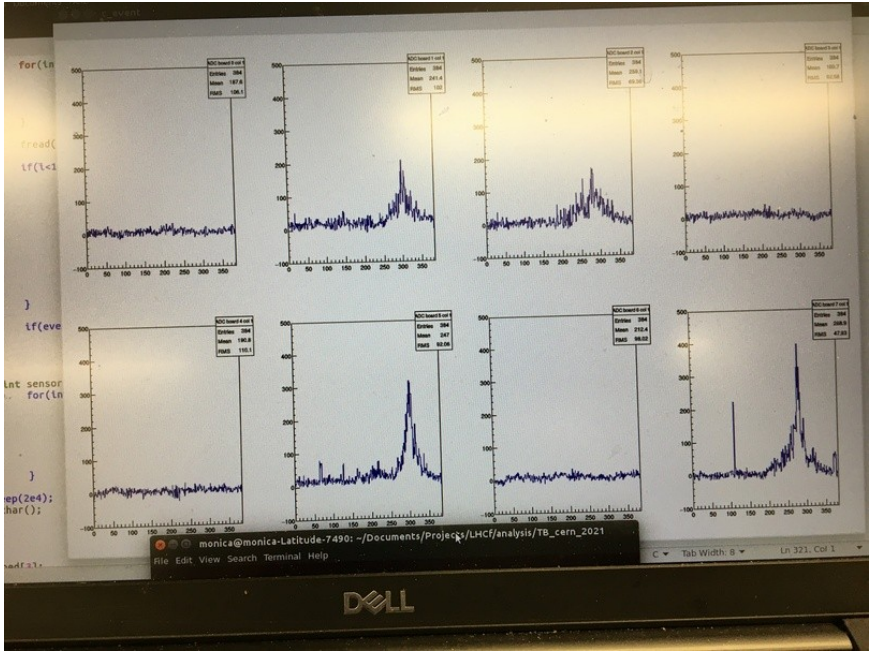
- “fine latency” in steps of 15ps: additional phase shift to the ADC clock implemented in the ZYNQ device

The fine latency is usually adjusted in order to have an average ratio between sample 0 and sample 1 of around 0.1 - 0.15

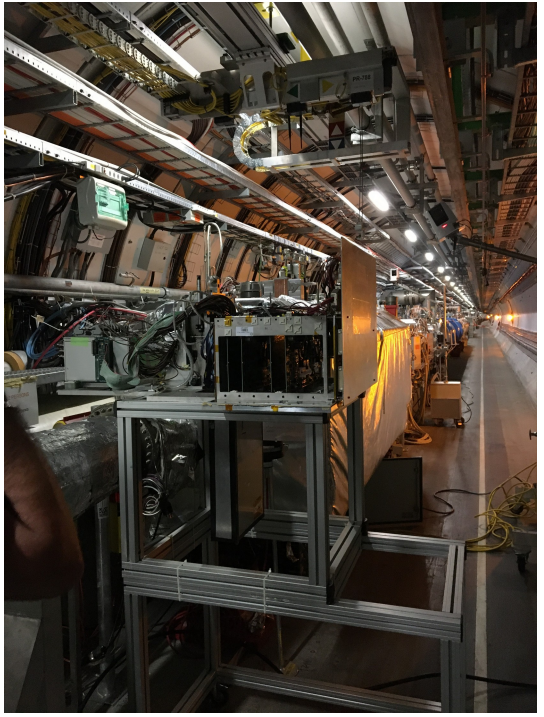
Both coarse and fine latency have been set with the same value for all the sections but can regulated independently

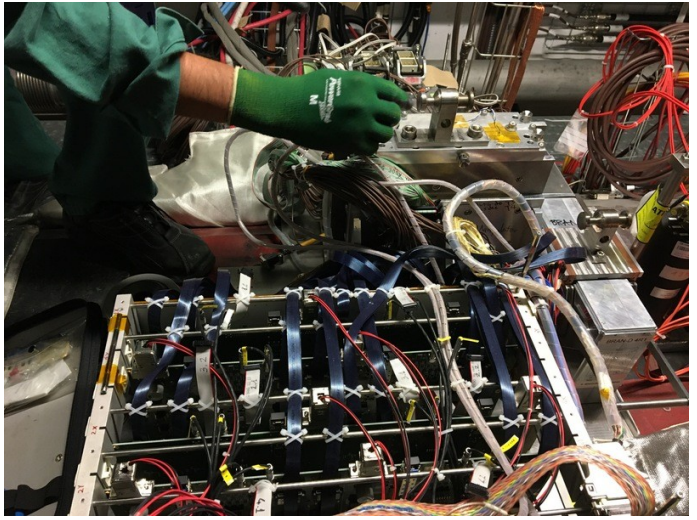
SPS 2021 Beam Test





LHC 2022 installation





Check <dE> in Beam event

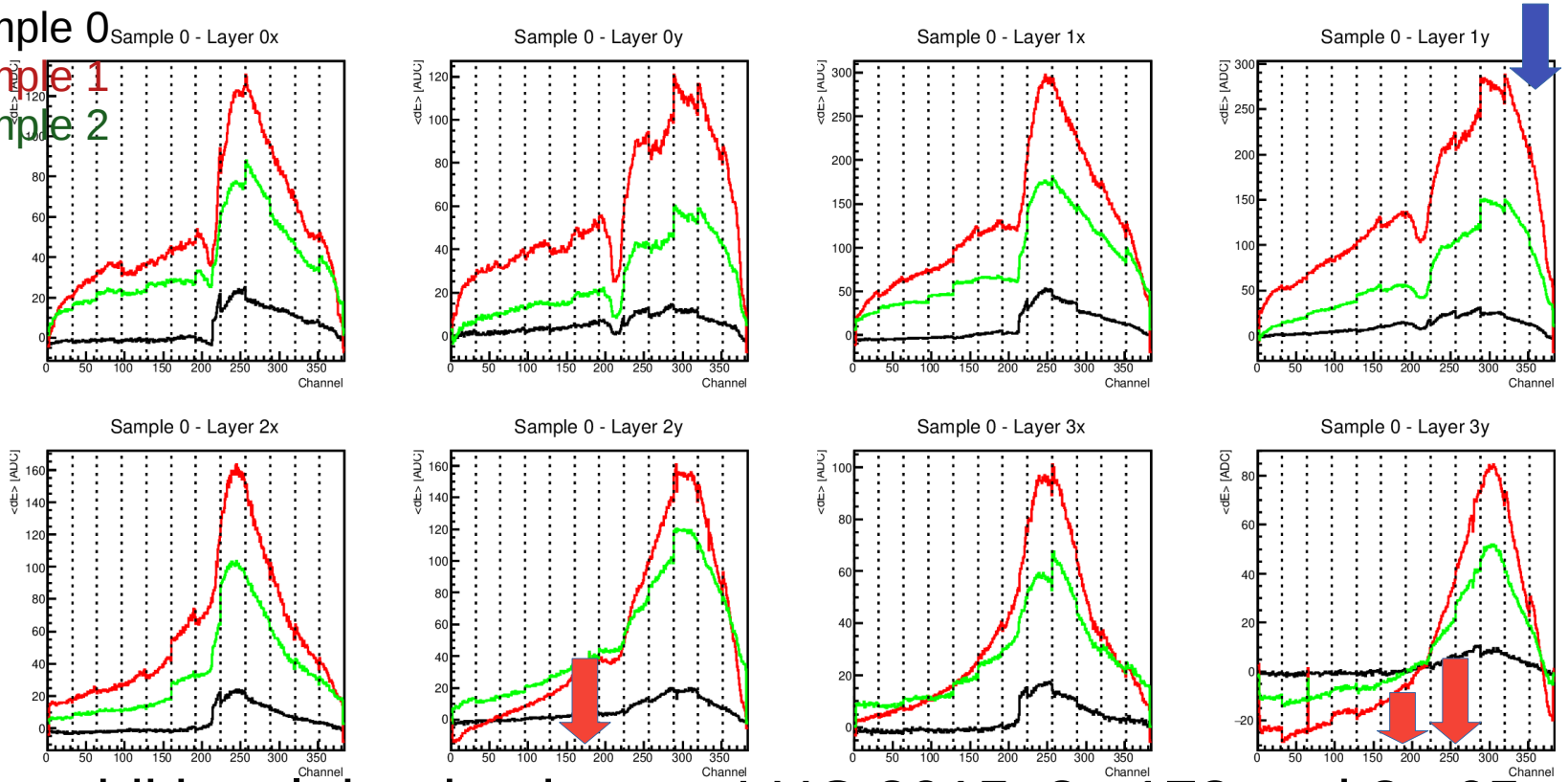
25000 events
from Run 80246

From Eugenio's talk
March 9th 2023

No energy deposit selection

All PACE chips seem correctly working

Sample 0
Sample 1
Sample 2



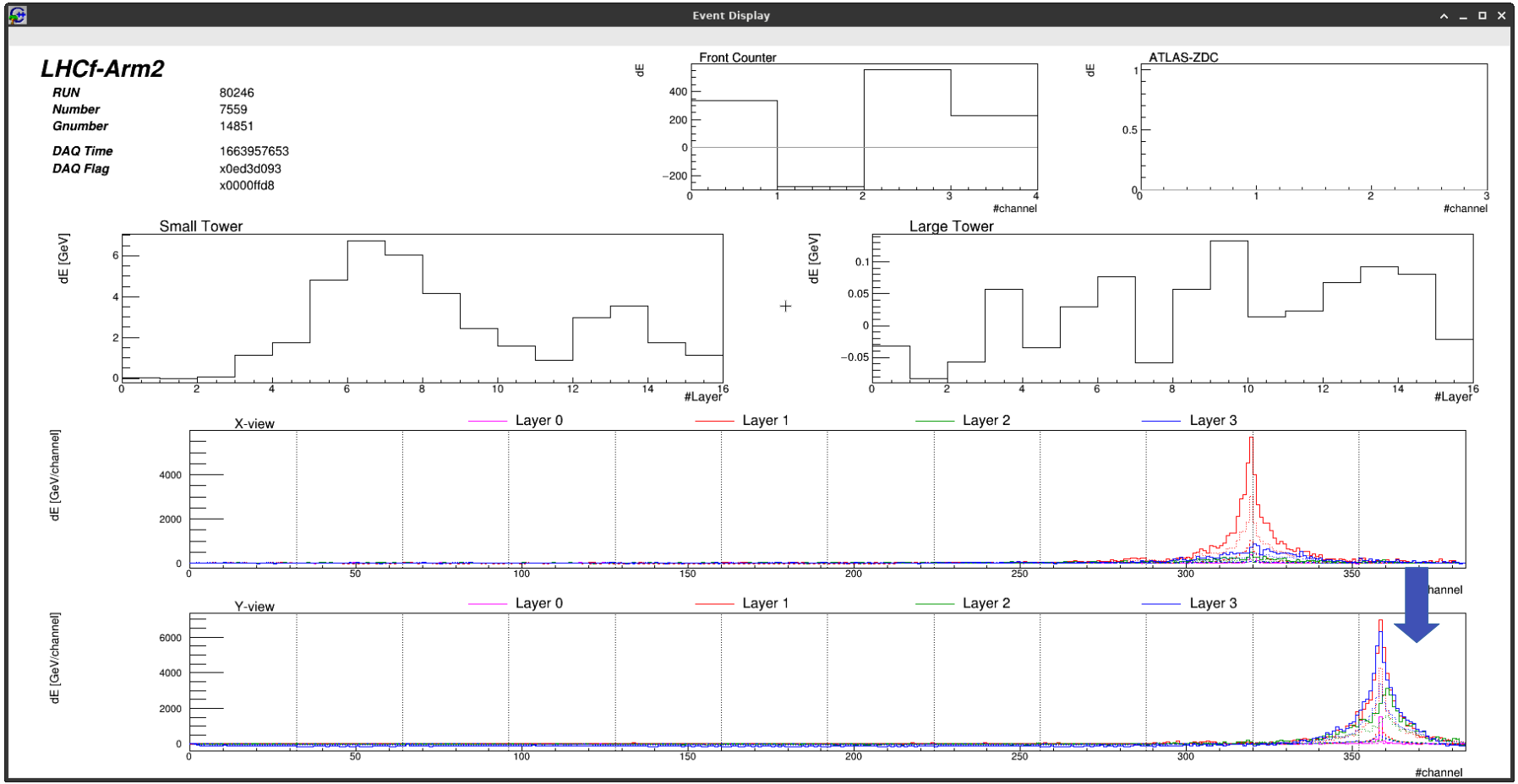
No additional dead strips wrt LHC 2015: 2y-178 and 3y-65

Detected errors

	SPS 2021	LHC 2022	
Section 3	DVA(7) CAA CAD error chip 1	DVA(7) Layer 2y Strip 256-287	Section 3
Section 6	DVA(6), DVA(10) CAA CAD error chip 0	DVA(7), DVA(11) Layer 3y Strip 256-287 Layer 3y Strip 192-223	Section 7
Section 7	CAA CAD error chip 1	CAA CAD error chip 1 Layer 1y Strip 352-383	Section 6

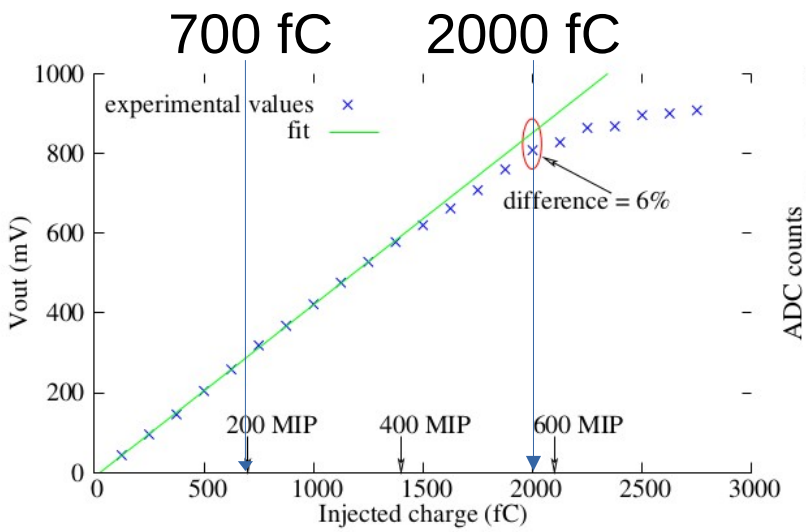
These warnings were commented in the reconstruction software to avoid large amount of output to terminal

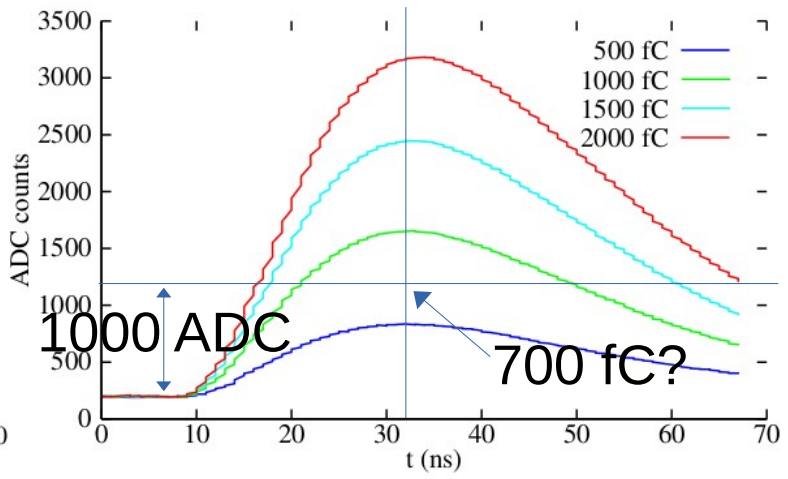
Event View


Event Display
LHCf-Arm2
RUN 80246
Number 7559
Gnumber 14851
DAQ Time 1663957653
DAQ Flag x0ed3d093
x0000ffd8
Front Counter
dE
#channel
ATLAS-ZDC
dE
#channel
Small Tower
dE [GeV]
#Layer
Large Tower
dE [GeV]
#Layer
X-view
Layer 0
Layer 1
Layer 2
Layer 3
dE [GeV/channel]
Y-view
Layer 0
Layer 1
Layer 2
Layer 3
dE [GeV/channel]
#channel

PACE3 saturation

Old electronics: saturation threshold was set to 1000 ADC



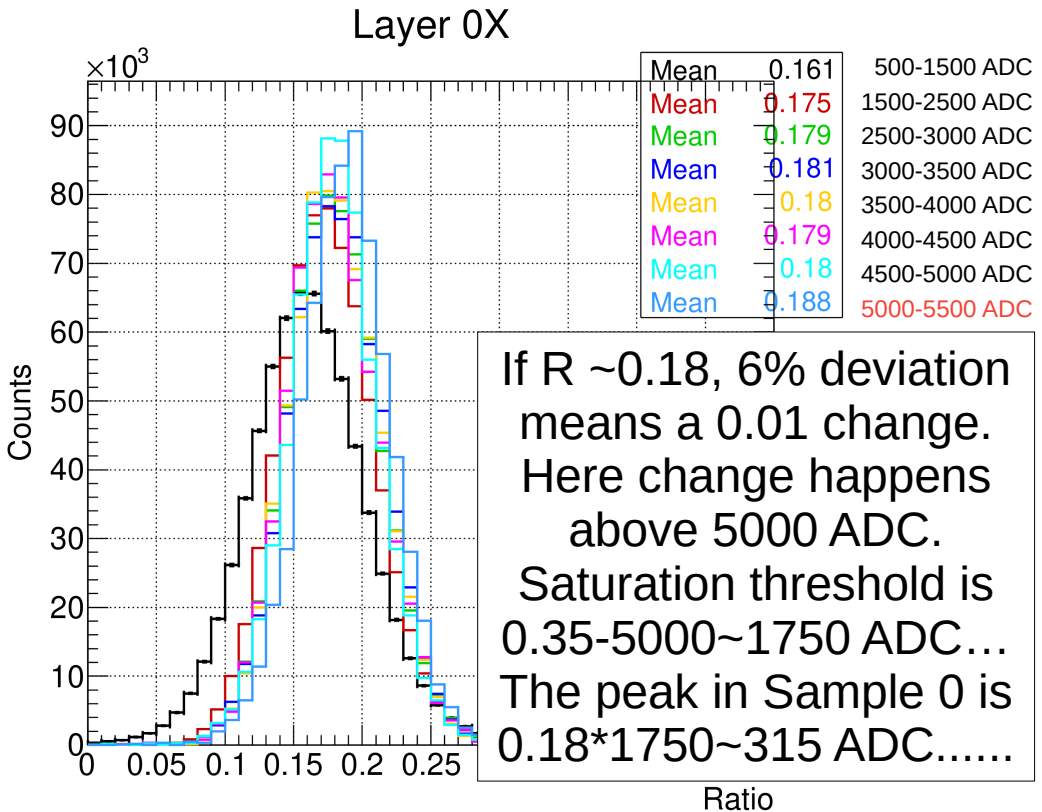


From Eugenio's talk
March 9th 2023

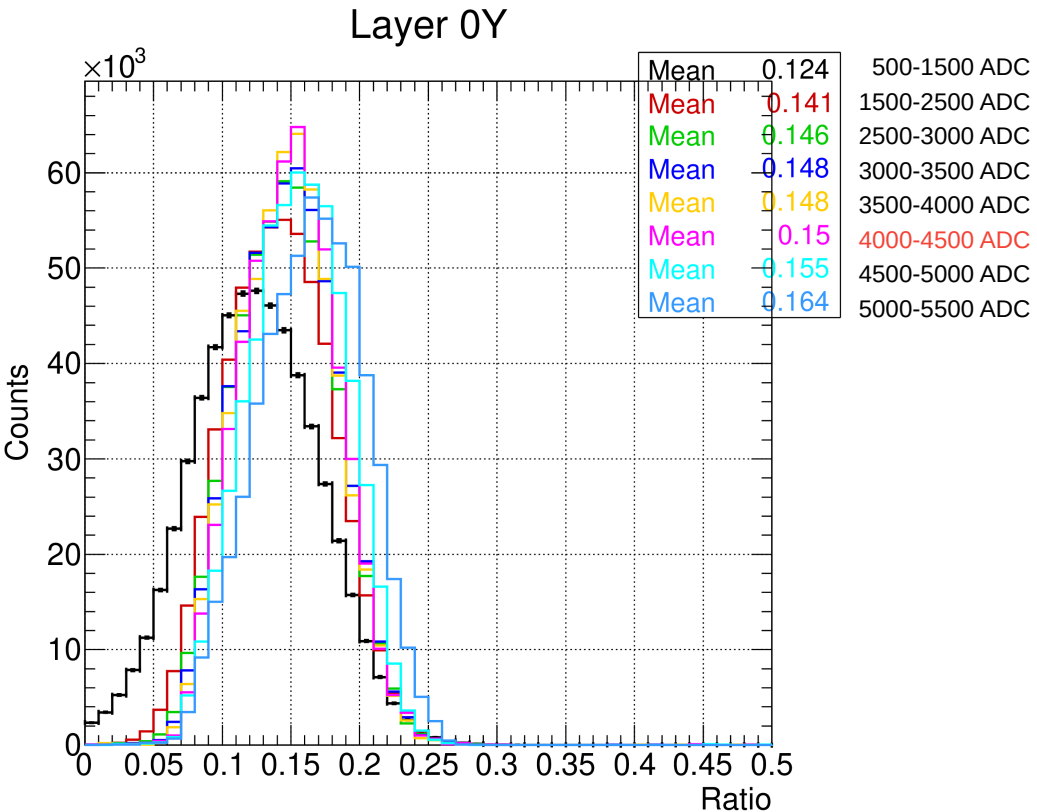
From a rough estimation the saturation threshold in the new electronics should be about 700/2000~0.35 times the deposit for which non linearity is 6%

R = Ratio between sample 0 and sample 1

From Eugenio's talk
March 9th 2023



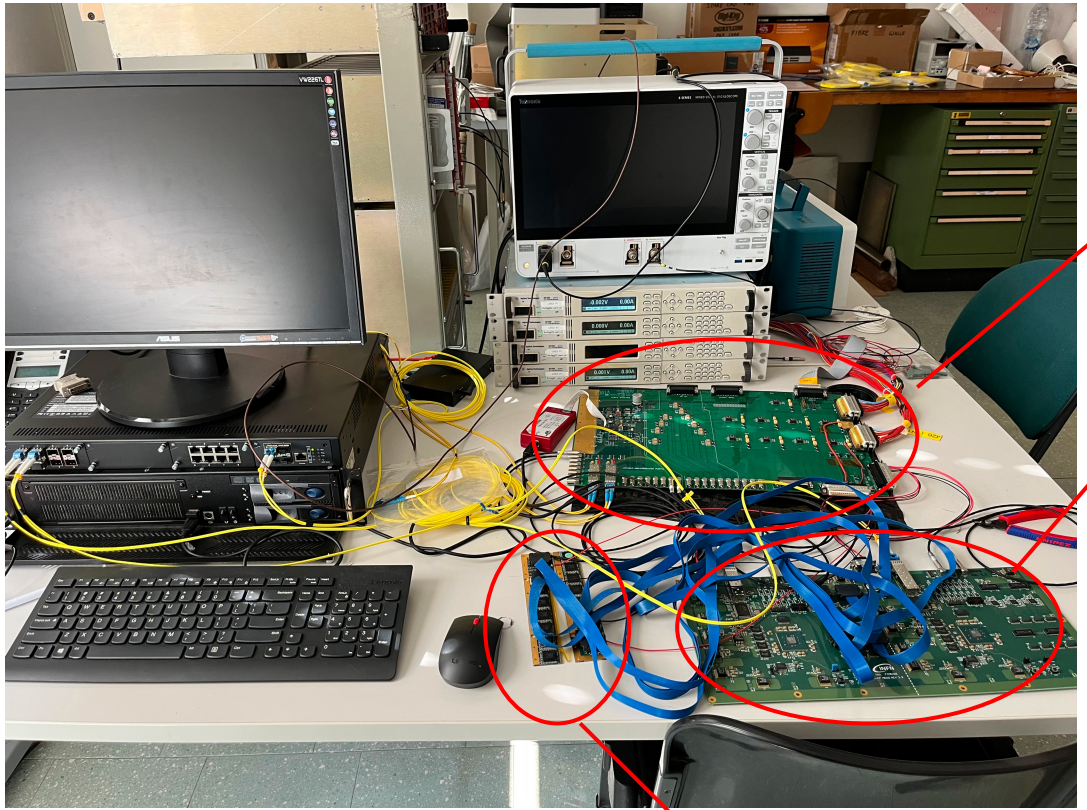
If R ~0.18, 6% deviation means a 0.01 change. Here change happens above 5000 ADC. Saturation threshold is 0.35-5000~1750 ADC… The peak in Sample 0 is 0.18*1750~315 ADC.....



PACE3 calibration

- Each channel has an internal calibration input capacitance (1.275 pF)
- Two modes of calibration, selected through Delta control register
  - External: the calibration pulse is sent externally to the CAL input of the chip
  - Internal: the calibration pulse is generated internally with an amplitude set by an internal register, triggered by the CAL logic pulse
- For each event a command is sent from the software through the CLKGEN board to the MDAQ boards where a sequence of CAL and L1 pulse is generated
- The delay between the two signals is set through a register, according to the latency value

PACE3 calibration setup in Florence



Spare PS-CLK board

Spare MDAQ board

Setup for calibration studies is ready, measurements will start soon!

Spare Hybrids

Next steps

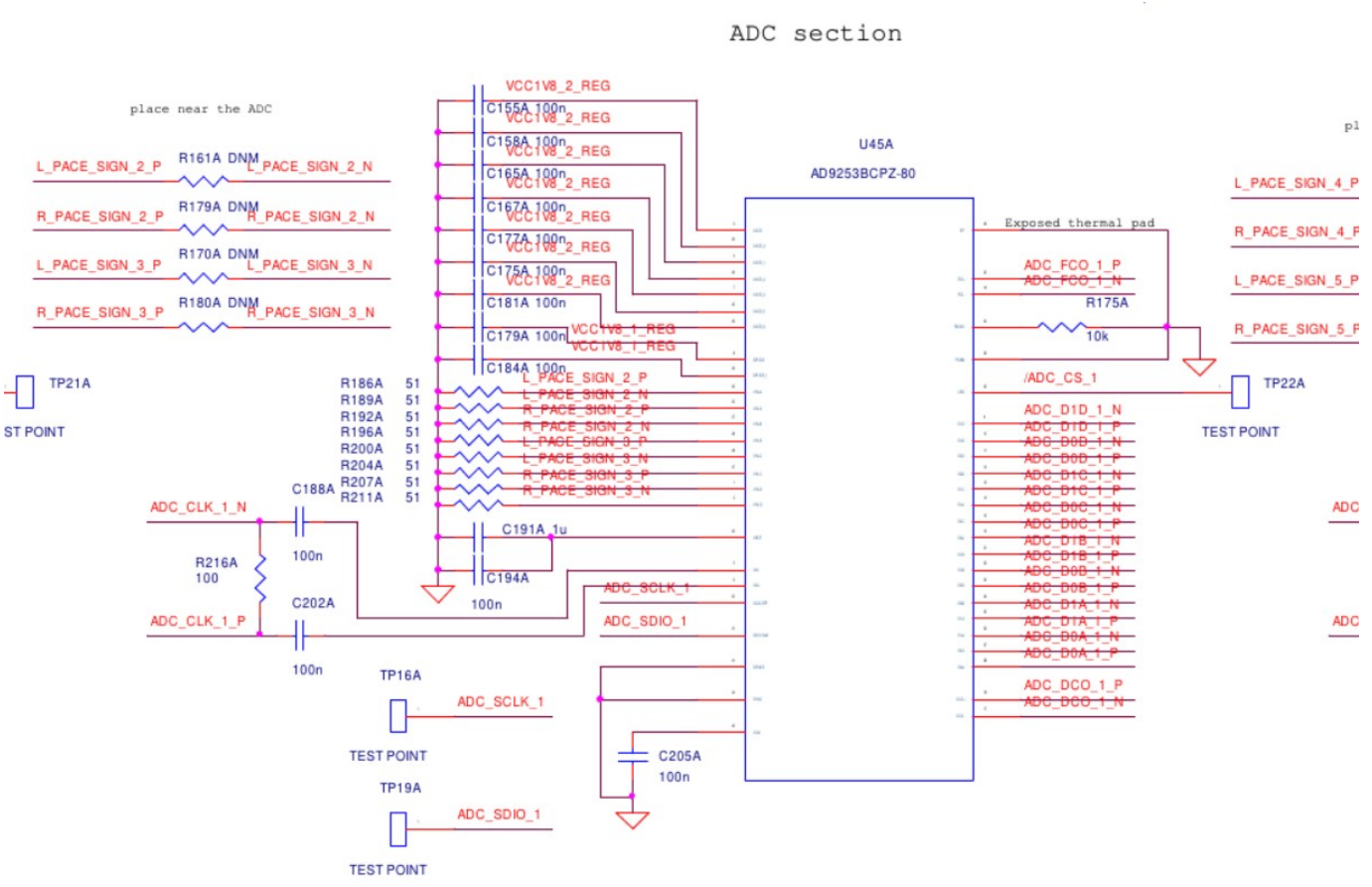
- Perform calibration on spare DAQ boards and hybrids
  - Fine tune the clock delay of each section to get the maximum at sample 1
  - Perform a set of acquisitions by scanning the input charge to determine the saturation curve
  - Investigate possible effects of saturation on neighbours channels
  - Repeat calibration after setting R to the value used during acquisition
- Perform calibration on ARM2 electronic boards at CERN (next February)

Conclusions

- A new back-end electronics for the ARM2 electronics has been designed, produced and tested
- Operation during SPS BT in 2021, LHC and SPS BT show that the performance of the system is good
- Some issues were found on saturation of front-end PACE3 chip: these will be addressed by a calibration procedure on the detector front-end
- An experimental set-up for calibration using spare boards has been prepared, measurements will start soon

spares

ADC schematic



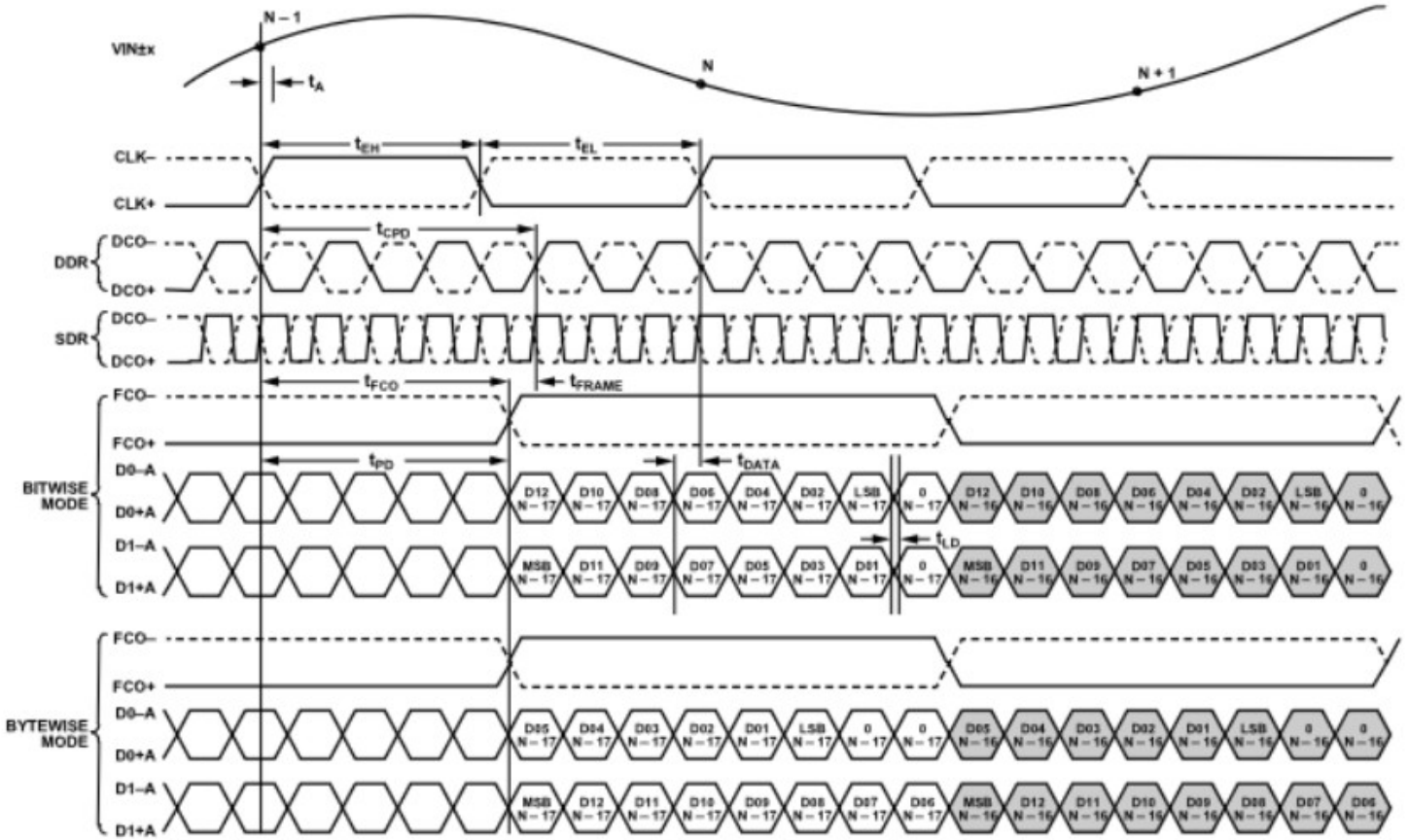


Figure 4. 16-Bit DDR/SDR, Two-Lane, 2× Frame Mode