Wojciech.Dulinski@ires.in2p3.fr

EUDET Beam Telescope: status of sensors and PCBs for the demonstrator

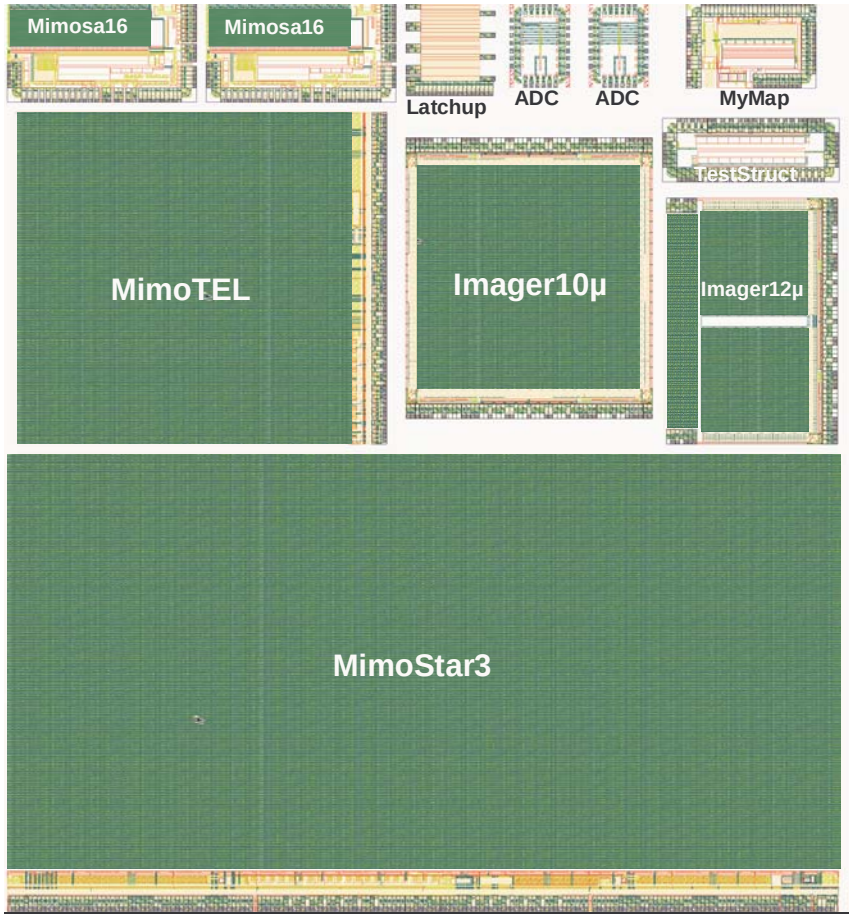
Wojciech Dulinski on behalf of IPHC

Outline

- **Engineering run AMS-035 OPTO**
- **MimoTEL tests and availability status**
- **Mimosa18 tests and availability status**
- **Status of re-processing**
- **PCBs status**
- **Conclusions and the status summary**

Wojciech.Dulinski@ires.in2p3.fr

Layout of the reticle of the engineering run AMS-035 OPTO 07/2006 on 14 µm (standard) and 20 µm epi substrate



Several devices of direct interest for EUDET: MimoTEL (256x256, 30 µm pitch), HRTracker (512x512, 10 µm pitch), Mimosa16 (binary readout prototype), MimoSTAR3L, ADC, test structures…

Wojciech.Dulinski@ires.in2p3.fr

Tests of two initial wafers from July submission

- End of October, reception of engineering run
- From November to end of 2006, two tests in parallel
  - Probe station setup preparation for wafer with 14 µm EPI
  - Laboratory test for circuits with 20 µm EPI
- End of 2006 to Jan. 2007, dicing 14µm EPI wafer
  - Laboratory test for circuits with 14 µm EPI

➔AMS did not respect one of specification: high-res poly

➔Biasing DACs out of range

➔difficult to make circuit working at nominal conditions

- No effect on Mimosa18 (High Resolution Tracker)
- Small modification on the PCB board: MimoTEL can be set "near" nominal conditions

Wojciech.Dulinski@ires.in2p3.fr

MimoTELs availability status (March 29)

Sensor #	Epi thickness	Status	Holding institution	Comments
1	20 µ	OK	IPHC	
2	20 µ	OK	IPHC	missing
3	20 µ	OK	IPHC	
4	20 µ	OK	Ferrara	
5	20 µ	OK	DESY	
6	20 µ	AVDD shorted	DESY	PCB problems?
7	20 µ	OK	DESY	
8	20 µ	OK	DESY	
9	14 µ	Pixel yield?	DESY	
10	14 µ	Pixel yield?	DESY	

Wojciech.Dulinski@ires.in2p3.fr

Mimosa18 availability status (March 29)

Sensor #	Epi thickness	Status	Holding institution	Comments
1	20 µ	OK	IPHC	
2	20 µ	OK	IPHC	
3	20 µ	OK	IPHC	
4	20 µ	OK	IPHC	
5	20 µ	OK	DESY	
6	14 µ	OK	IPHC	

Wojciech.Dulinski@ires.in2p3.fr

General remarks concerning two first wafers

- The dark current on rad-tol diodes (MimoSTAR, MimoTEL) factor of 5 to 10 higher than expected

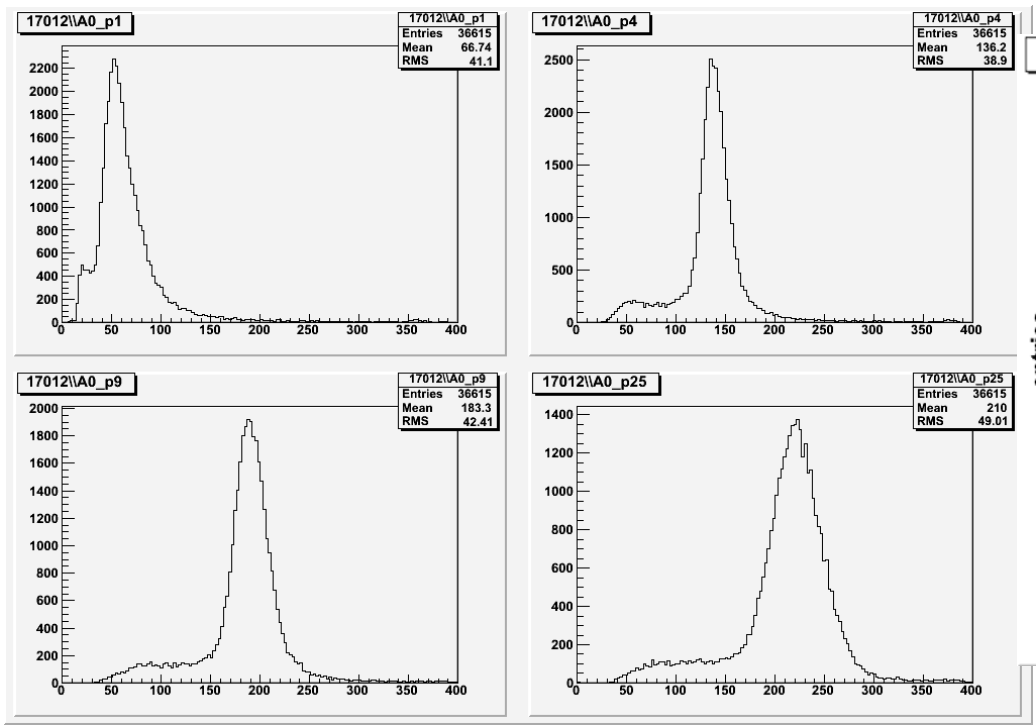
- The dark current on non rad-tol diodes (Mimosa18) factor of 5 to 10 lower than expected…

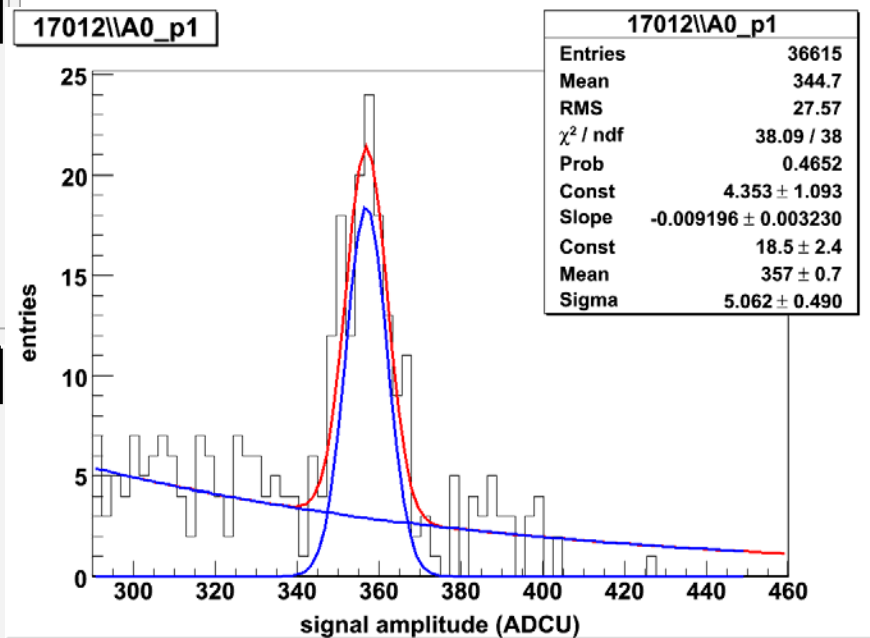
- Yield problems observed on many devices from14 µm wafer (but an excellent yield on 20 µm wafer!)

Mathieu Goffe
Mathieu.goffe@ires.in2p3.fr

Chip mimotel epitaxial 20um

Chip	Run	Temp °C	Frequence MHz	A0			A1			A2			A3			Gain chip
				Noise	Pic	e-	Noise	Pic	e-	Noise	Pic	e-	Noise	Pic	e-	
1	17010	20	16	3.33	354.2	15.41	3.43	365.8	15.37	3.37	360.2	15.34	3.37	360.1	15.34	5
3	17011	20	16	3.35	355.5	15.45	3.32	359.3	15.15	3.3	358.8	15.08	3.27	359.3	14.92	5
4	17012	20	16	3.34	357	15.34	3.36	360.3	15.29	3.23	360.3	14.7	3.24	356.8	14.89	5
5	17013	20	16	3.42	352.9	15.89	3.38	358	15.48	3.35	355.7	15.44	3.32	355.6	15.31	5





Mathieu Goffe
Mathieu.goffe@ires.in2p3.fr

Chip mimosa18 epitaxial 20um

Chip	Run	Temp °C	Frequence MHz	A0			A1			A2			A3		
				Noise	Pic	e-	Noise	Pic	e-	Noise	Pic	e-	Noise	Pic	e-
2	18012	20°C	10	2.01	302.2	10.90	2.00	299.9	10.93	2.03	304	10.95	2.00	298.6	10.98
5	18017	20°C	16	1.92	295.7	10.64	1.93	298.8	10.59	1.94	302	10.53	1.93	300.8	10.52
5	18019	10°C	16	1.85	297.7	10.19	1.85	301.2	10.07	1.86	305.1	9.99	1.86	303.3	10.05
5	18020	0°C	16	1.81	300.4	9.88	1.82	304.1	9.81	1.82	306.7	9.73	1.82	305.1	9.78
5	18021	30°C	16	2.06	291.7	11.58	2.06	296.4	11.39	2.08	299.2	11.40	2.07	297.8	11.39
5	18022	40°C	16	2.31	288.5	13.13	2.32	291	13.07	2.34	292.8	13.10	2.33	293.3	13.02
5	18023	20°C	25	1.95	285.1	11.21	1.94	290.9	10.93	1.95	293.6	10.89	1.94	292.1	10.84

At 16,6 MHz Ti = 4 ms chip 5

	0 °C				10 °C				20 °C				30 °C				40 °C			
Noise Uadc	1.81	1.82	1.82	1.82	1.85	1.85	1.86	1.86	1.92	1.93	1.94	1.93	2.06	2.06	2.08	2.07	2.31	2.32	2.34	2.33
Pic	300.4	304.1	306.7	305.1	297.7	301.2	305.1	303.3	295.7	298.8	302	300.8	291.7	296.4	299.2	297.8	288.5	291	292.8	293.3
Noise e-	9.88	9.81	9.73	9.78	10.19	10.07	9.99	10.05	10.64	10.59	10.53	10.52	11.58	11.39	11.40	11.39	13.13	13.07	13.10	13.02

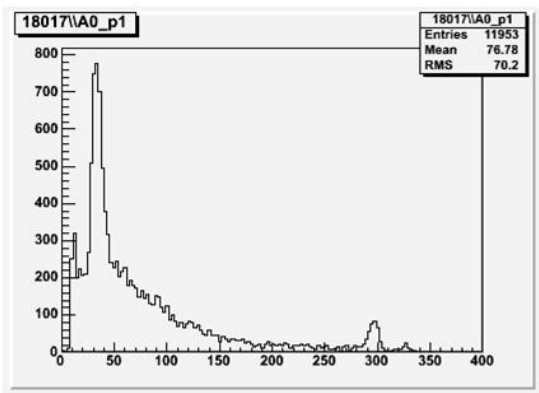
10 MHz Ti = 6.5 ms

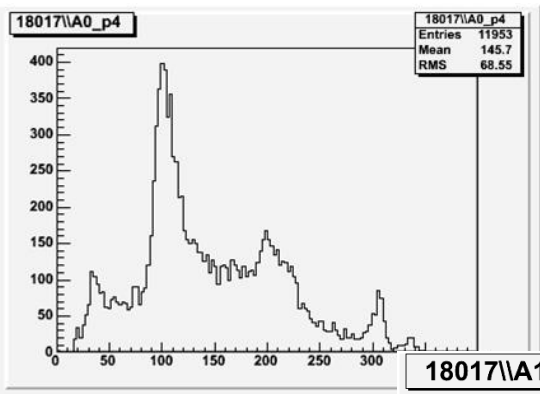
2.01	2.00	2.03	2.00
302.2	299.9	304	298.6
10.90	10.93	10.95	10.98

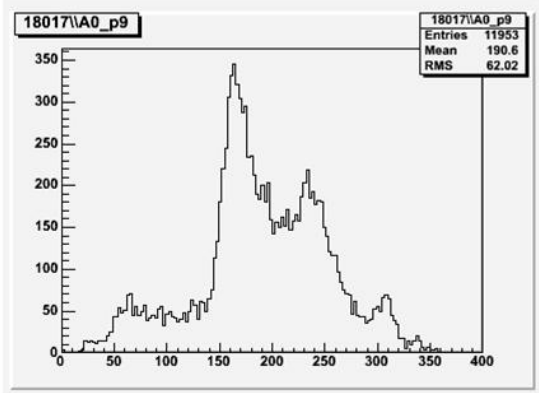
25 MHz Ti= 2.6 ms

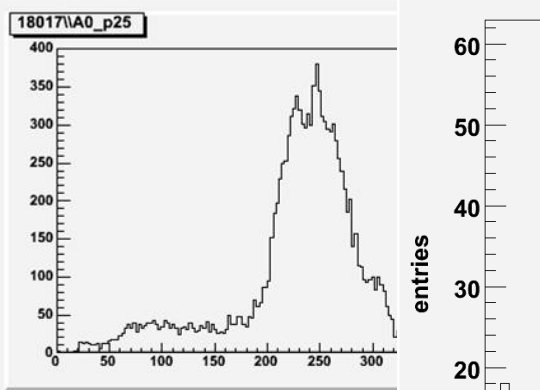
1.95	1.94	1.95	1.94
285.1	290.9	293.6	293.3
11.21	10.93	10.89	10.84

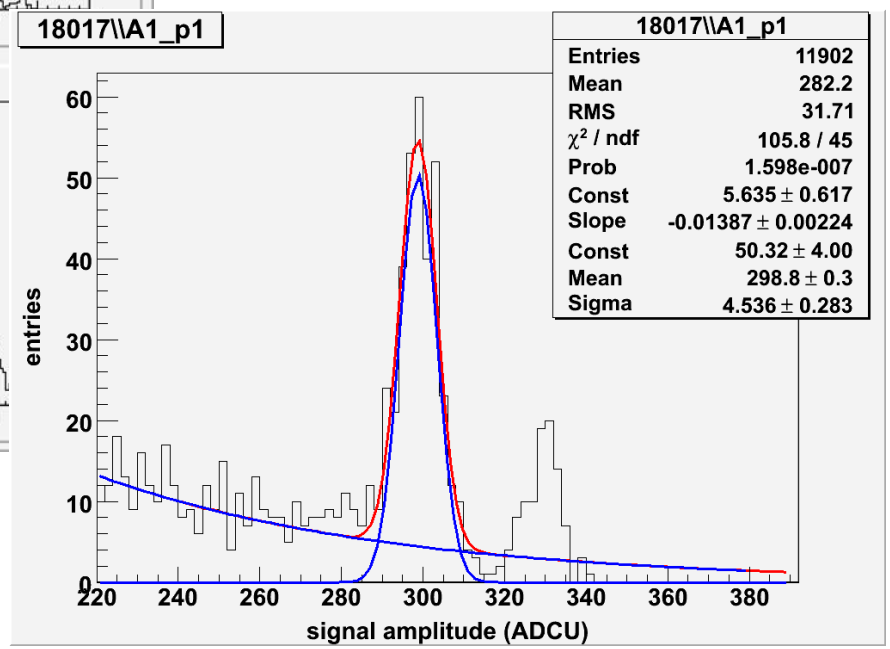
Mathieu Goffe
Mathieu.goffe@ires.in2p3.fr











IPHC, 23 rue du Loess BP 28, 67037, Strasbourg Cedex 02, France

Wojciech.Dulinski@ires.in2p3.fr

Status of re-processing

- End of February, re-processing finished

➔One of parameters (VTFPP) out of specification

➔AMS statement:

` »VTFPP is the threshold voltage of a parasitic p-channel field transistor with a poly-gate on top of the field oxide. The function of this element is to isolate adjacent transistors from each other. Therefore this transistor must not turn at a gate voltage which is near the maximum supply voltage of the chip. Those wafers are with this value around 14 Volts which is still more than 2 times above the supply voltage and therefore from that point of view there is no risk of a malfunction of the circuit. The root cause for this lower values on this lot has been found in a higher variation of the poly1 to active area overlay data. As this parasitic transistor is quite sensitive to overlay variations we have got this out of spec values on this lot. As the root cause is only an overlay issue, there is absolutely no relation to an enhanced nwell to substrate leakage or Latch-up behavior possible. »

NO Problem???

Wojciech.Dulinski@ires.in2p3.fr

Status of re-processing

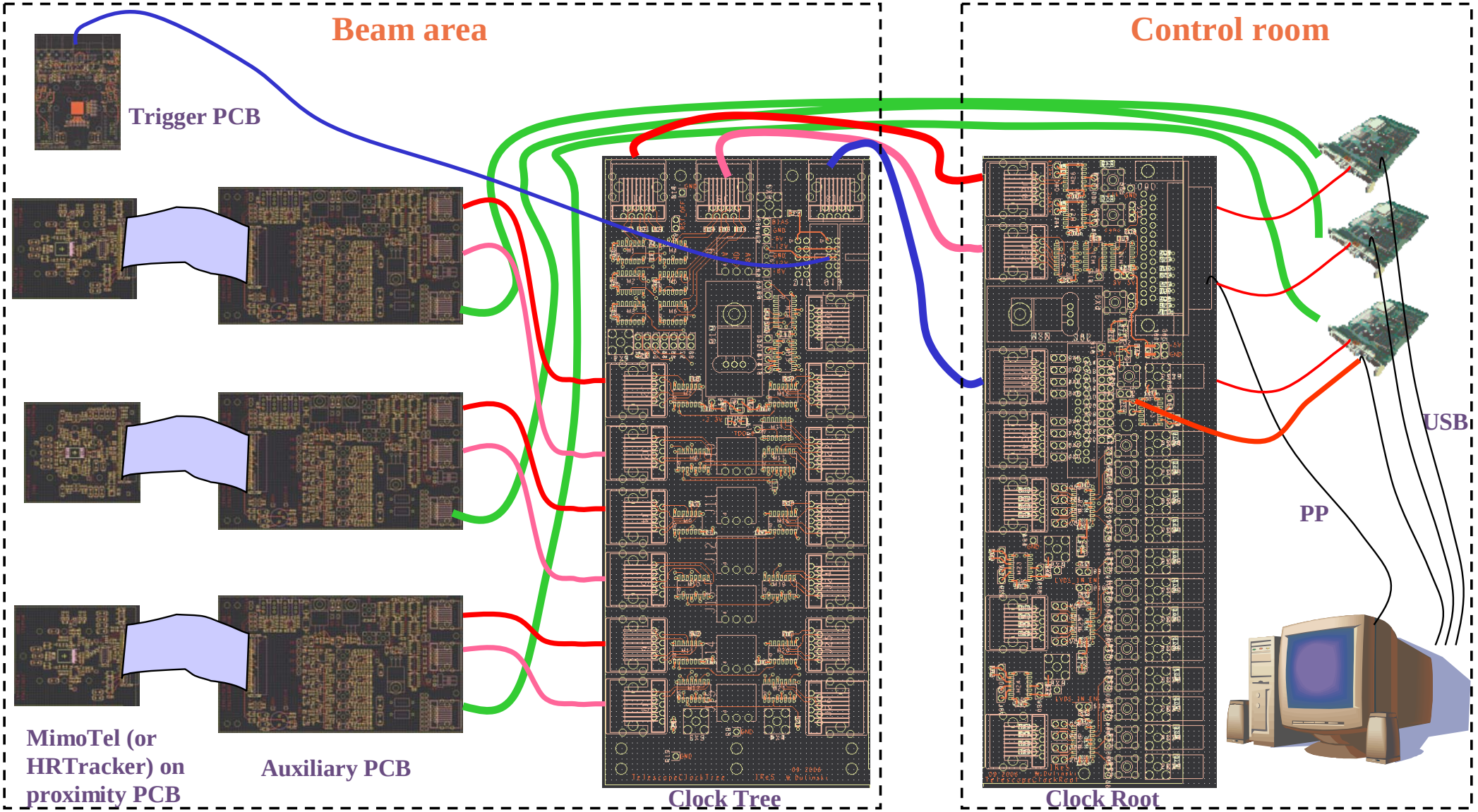
- Consequences of VTFPP on our device performance not clear yet…

Run #	Chip	VTFPP	Ipixel@ 25°C
>> A35C5_1	Mimosa11	-24V	5fA
>> A35C5_4	MimoStar2	-25V	5fA
>> A35C5_5	Mimosa15	-24V	5fA
>> Run Eng	MimoStar3 20µ	-20V	>50fA
>> Run Eng	MimoStar3 14u	""	20fA
>> re-RunEng	MimoStar3	-14V	????

In discussion, possible design reviewing at AMS, leakage current measurements before any decision seems feasible, possible re-processing (at AMS cost)…

Wojciech.Dulinski@ires.in2p3.fr

Telescope PCBs and cables



Wojciech.Dulinski@ires.in2p3.fr

PCB's status

- Twenty PCB front-sets (MimoTEL + HRTracker + Auxiliary) ordered, 5 fully assembled at IPHC, 5 fully assembled at DESY

- Some bonding problems (on the PCB side), in particular on DESY assembled series

- Ten sets returned to PCB supplier for cleaning and surface re-metallization

- First samples expected back this week

- Bonding tests, re-metallization of remaining will follow shortly

Do we need more PCBs?
Who feels responsible for the clock concentration/distribution PCBs?

Wojciech.Dulinski@ires.in2p3.fr

Conclusions/present status

-Two wafers (14 µm and 20 µm epi) delivered and diced (wafer NOT thinned)

- Preliminary tests demonstrated non-conformity of process with the option specified for this run (missing HiRes layer)

- Serious consequences (however not fatal) for MimoTEL sensors

- Delivery of sensors for the demonstrator phase to EUDET collaboration follows initial planning

- New run (re-processing using the same mask set) and new problems…

- The only consequences may be early availability of thinned sensors