Final Sensors for EUDET Telescope: Progress Report

Progress since January '07 — Plans for coming 2 years

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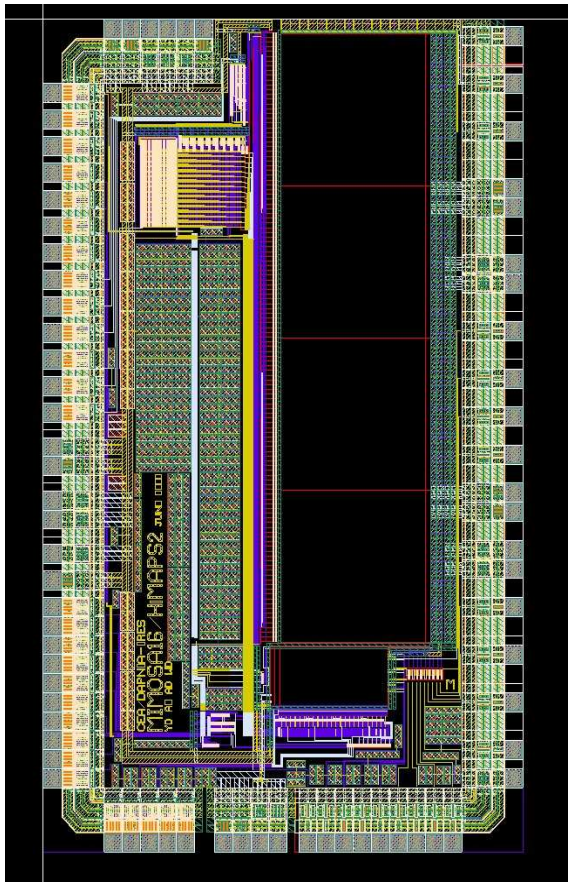
on behalf of DAPNIA-Saclay & IPHC-Strasbourg

OUTLINE

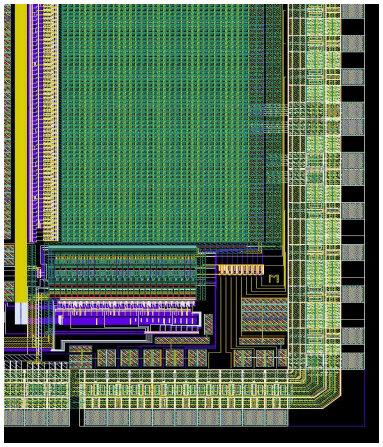
- MIMOSA-16 tests : results (CCE !) and status $\rightarrowtail$ next steps
- $\emptyset$ micro-circuit : status of 1st prototype design
- Milestones until Final Sensor
- Sensor fabrication plans for 2007 – 2009
- Summary

Tests of MIMOSA-16

- **MIMOSA-16 design features :**
  - **AMS-0.35 OPTO translation of MIMOSA-8**
    $\hookrightarrow \sim$ **11–16** μm **epitaxy instead of** $\lesssim$ **7** μm
  - **32 // columns of 128 pixels (pitch: 25** μm**)**
  - **on-pixel CDS (DS at end of each column)**
  - **24 columns ended with discriminator**
  - **4 sub-arrays :**
    - **S1 : like MIMOSA-8 (1.7x1.7** μm^2 **diode)**
    - **S2 : like MIMOSA-8 (2.4x2.4** μm^2 **diode)**
    - **S3 : S2 with ionising radiation tol. pixels**
    - **S4 : with enhanced in-pixel amplification**
      (against noise of read-out chain)



$\Rightarrow$



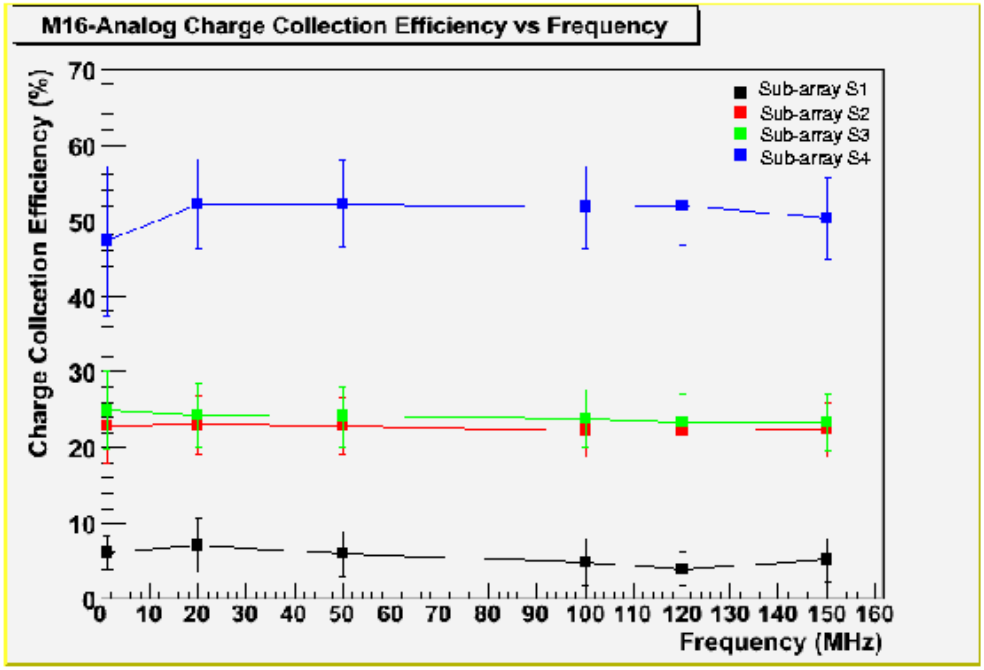
- **Preliminary tests of analog part (”20** μm**” epitaxy) performed in Saclay (shown in January):**
  - **sensors illuminated with** ^{55}**Fe source and** $F_{r.o.}$ **varied up to** $\gtrsim$ **150 MHz**
  - **measurements of N(pixel), FPN (end of column), pedestal variation, CCE (3x3 pixel clusters) vs** $F_{r.o.}$
- **Tests of analog part (”14** μm**” epitaxy) started in Saclay** $\rightarrowtail$ **first results (CCE)**
- **Next steps :**
  - **digital part** $\geq$ **May at IPHC**
  - **beam tests** $\gtrsim$ **4 Septembre at CERN (T4 – H6)**
- **Hanging : tests of wafers produced in 2nd batch**

Tests of MIMOSA-16

Charge Collection Efficiency vs Frequency

Chip#0 (old mezzanine board)

Columns 28-31



⇛ **Poor charge collection efficiency for S1 (1.7x1.7 μm^2) and S2/S3 (2.4x2.4 μm^2)**

↪ **already observed with MIMOSA-15 (suspected origin: diffusion of P-well, reducing the contact surface between N-well and epitaxy) ⟶ seems confirmed by S4 (4.5x4.5 μm^2 diode)**

⁂ **"14 μm" epitaxy expected to exhibit $\sim$ 30 – 40 % higher CCE (based on MIMOSA-9,-11,-14,-15)**

MIMOSA-16 : CCE for "14" and "20" μm Epitaxy

MIMOSA16#EPI14 (@f_{CK}=10MHz)*				
	CVF (µV/e-)	**Temporal Noise (e-)**	**FPN (e-)**	**CCE (for 9 pixels)**
S1 diode: (1.7µm)²	-	-	-	-
S2 diode: (2.4µm)²	62.5	**10.4**	2.8	37 %
S3 diode: (2.4µm)² rad-tol	56	12.5	2.3	42 %
S4 diode: (4.5µm)² improved gain	57	15	2.6	62 %

MIMOSA16#EPI20 (@f_{CK}=20MHz)**				
	CVF (µV/e-)	**Temporal Noise (e-)**	**FPN (e-)**	**CCE (for 9 pixels)**
S1 diode: (1.7µm)²	67	12.0	3.6	9 %
S2 diode: (2.4µm)²	61	12.5	3.3	23 %
S3 diode: (2.4µm)² rad-tol	55	13.0	3.0	26 %
S4 diode: (4.5µm)² improved gain	60	14.5	2.2	49 %

* temperature $\approx$ 30°C (without cooling system !)
** temperature $\approx$ 20°C (with cooling system)

Y. Degerli, Y. Li, F. Orsini, P. Lutz, 27/03/2007

- MIMOSA-16 ("14" and "20" μm epitaxy) illuminated with ^{55}Fe $\longrightarrow$ charge collected in 3x3 clusters
  $\longrightarrow$ CCE ("14" μm) $\sim$ 30–60 % higher than CCE ("20" μm) (15 % rel. uncertainty ?)

MIMOSA-20 : CCE for ”14” and ”20” μm Epitaxy

IPHC Institut Pluridisciplinaire Hubert CURIEN STRASBOURG

Réunion Capteurs CMOS, lundi 26 fevrier 2007

Mathieu Goffe
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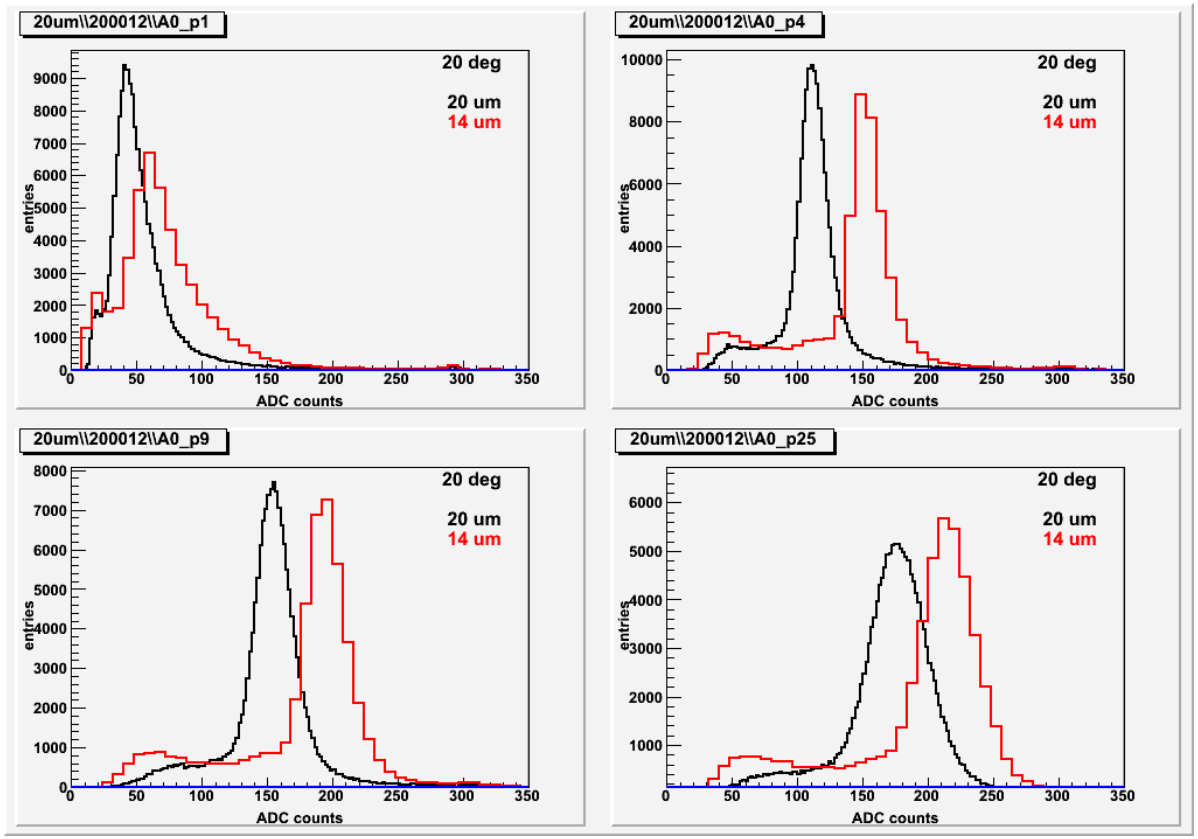
Comparaison pour Mimosa20 entre les deux types de couches épitaxie



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- MIMOSA-20 (”14” & ”20” μm epitaxy) illuminated with ^{55}Fe
  - $\longmapsto$ charge collected in seed pixel, 2x2, 3x3 and 5x5 clusters
    - $\longmapsto$ CCE (”14” μm) $\sim$ 30–40 % higher than CCE (”20” μm)

- MIMOSA-9, -11, -14, -15 & -20 : CCE for ”14” μm Epitaxy

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Epitaxial 14 um

capteur	chip	RUN	Temp C	Freq MHz	Ti ms	Seed	1*1	2*2	3*3	5*5	pitch	remarque
Mi9	1	9499	20	10	0,4 1	212	65 30%	150 70%	182 85%	190 89%	20	Grande diode 6*6 (A0_S1)
Mi9	1	9499	20	10	0,4 1	306	70 22%	176 57%	218 71%	245 80%	20	Petite diode 3,4*4,3 (A0_S0)
Mi11	4	11666	20	2,5	0,7	260	54 20%	136 52%	171 65%	186 71%	30	Diode Star RadTol (A3_S0)
Mi11	4	11666	20	2,5	0,7	301	65 21%	168 55%	216 71%	242 80%	30	Diode Star Std (A0_S1)
Mi14	2	14350	20	2	4	235	48 20%	125 53%	159 67%	180 76%	30	Rad Tol
Mi14	2	14350	20	2	4	269	59 22%	146 54%	188 69%	212 78%	30	Standart
Mi 15	5	15354	20	2,5	0,7	235	54 23%	135 57%	176 74%	194 82%	30	Pixel type Star (A0_S0)
Mi20	5	200105	20	50	2	290	64 22%	153 52%	195 67%	216 74%	30	Rad Tol

- CCE reproduced by all 5 sensors within a few per-cent

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Epitaxial 20 um

capteur	chip	RUN	Temp C	Freq MHz	Ti ms	Seed	1*1	2*2	3*3	5*5	Pitch	remarque
Mi17	2	17670	20	10	1,6	377	60 16%	150 40%	205 54%	230 61%	30	Mise en route
Mi17	4	17012	20	16	1	357	52 14,5%	139 39%	189 53%	224 62,7%	30	Gain final carte aux_eudet
Mi18	1	18011	25	10	6,5	291	33 11%	97 34% 196 68%	158 54% 230 80%	220 75% 240 83%	10	Mise en route
Mi18	5	18017	20	16	4	298	33 11%	102 34% 198 66%	163 54% 233 78%	228 76% 246 82%	10	Gain final carte aux_eudet
Mi20	2.1	200012	20	50	2	289	44 15%	112 38%	153 52%	176 60%	30	Rad Tol

- CCE substantially lower than for ”14” μm epitaxy

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CCE : Preliminary Test Conclusions

- **"14" μm epitaxy (= default version of AMS-0.35 OPTO) :**
  - ⁂ **MIMOSA-16 (3x3 pixel clusters) reproduces behaviour of MIMOSA-9, -11, -14, -15 $\sim$ well :**
    similar (or larger !) CCE for the ranges of temperature and integration time considered

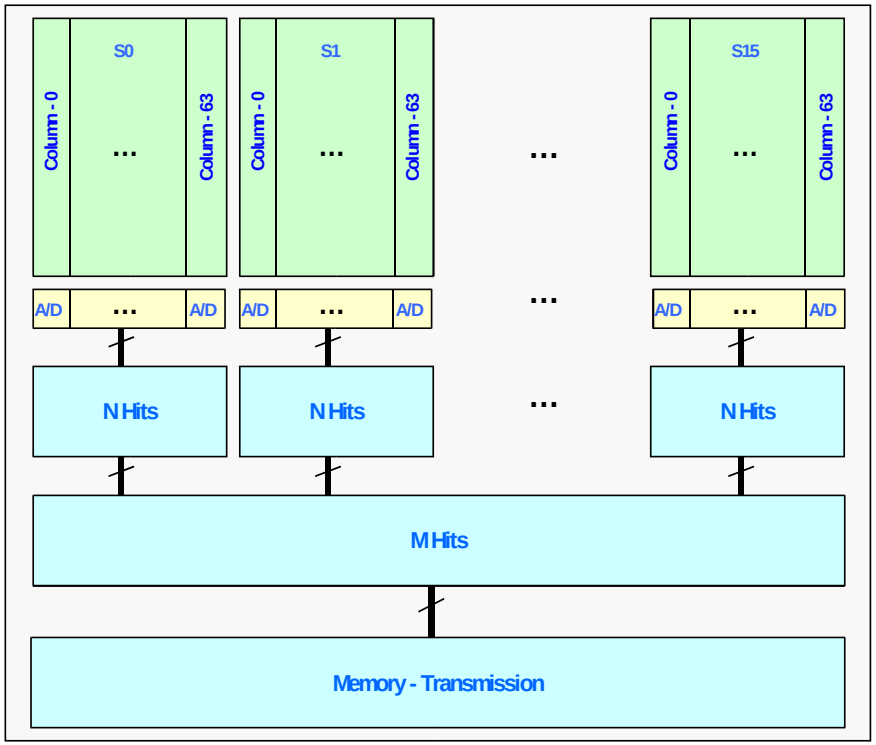
- **"20" μm epitaxy (= new option) :**
  - ⁂ **MIMOSA-20, -16 (-17) sensors with "20" μm epitaxy exhibit only $\sim$ 2/3 CCE of chips with "14" μm epi**

- **Refabricated wafers :**
  - ⁂ **1 production parameter slightly out of spec. $\longmapsto$ possibly negligible consequences but ...**
    - ⁂ **negociations with AMS under way :**
      more info on prod. parametres, availability of 2 wafers for quality tests, a.s.o.

Integrated ∅ Suppression

Zero Suppression : Block Diagram

Chip readout architecture including digitization and zero suppression



Block diagram of readout architecture

- Pixel array : 1024x1024 pixels Readout row by row The row is divided into 16 groups
- Analog to digital conversion at the bottom of each column (Discriminator or ADC)

Zero suppression algorithm :

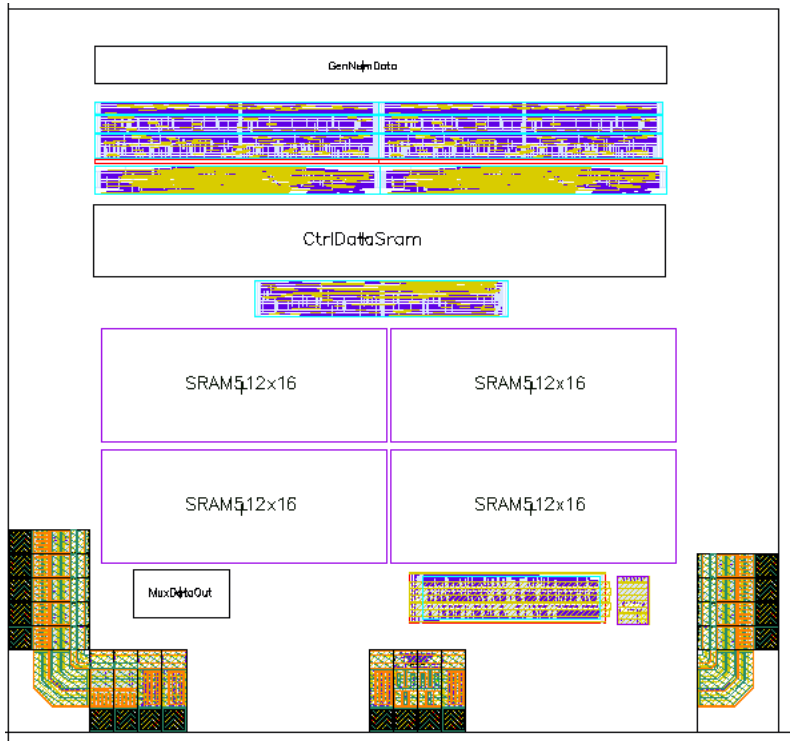
- Find N Hits for each group
  Find M Hits for each row
  (With N and M determined by pixel array occupancy rate)
- Memory wich stores M hits and serial transmission

- Submission of a small size fully digital prototype in AMS 0.35 µm in June 2007

Zero Suppression Micro-Circuit : Floor Plan

1st chip (SUZE-01) with integrated $\emptyset$ and output memories (no pixels) :

- 2 step, line by line, logic :
  - ◇ step-1 (inside blocks of 64 columns) :
    identify up to 6 series of $\leq$ 4 neighbour pixels per line
    delivering signal $>$ discriminator threshold
  - ◇ step-2 : read-out outcome of step-1 in all blocks
    and keep up to 9 series of $\leq$ 4 neighbour pixels
- 4 output memories (512x16 bits) taken from AMS I.P. library
- surface $\sim$ 3 x 3 mm^2 $\longrightarrow$ $\sim$ 6 keuros (EUDET budget)



Status :

- design under way
- submission scheduled for end of June
  $\hookrightarrow$ back from foundry end of Septembre
- tests completed by end of year

PLANS for 2007–2009

- Milestones bridging the gap with the Final Chip

Pixel design :

- adapt existing pixel architectures from 25 μm to $\gtrsim$ 16 μm pitch
- adapt sensing diode dimensions to maximise CCE (surface $\nearrow$) & gain (surface $\searrow$) : optimum $\sim$ 10–15 μm^2
- ▶ find optimal pixel pitch : single point resolution (pitch $\searrow$) against reliable design (pitch $\nearrow$)

Column read-out architecture :

- adapt existing S&H and discriminators from 25 μm to $\gtrsim$ 16 μm pitch
- integrate $\emptyset$ and output memories

Raw and pixel steering (consequences of large surface) :

- adapt pixel steering (speed) inside column to avoid capacitance due to large nb of switches $\rightarrowtail$ pixel design
- adapt raw steering to their length (2 cm)

Sensor autonomy and testability :

- JTAG + bias DAC $\rightarrowtail$ programmable chip steering
- 2 or 3 additionnal DC voltages to emulate pixel's output for independent discriminator performance assessment

Means needed to deliver final chip commissioned by 2009 :

- human resources for designs ($\gtrsim$ 4 – 5 FTE) and tests ($\gtrsim$ 2 – 3 FTE)
- equipment for designs and tests (presently essentially at IPHC ...)
- funding : $\lesssim$ 100 keuros (devt) & $\gtrsim$ 100 keuros (prod.) $\rightarrowtail$ EUDET : 36 keuros (devt) & 70 keuros (prod)

- Next prototype with column // architecture : MIMOSA-22

♣ **Extension of MIMOSA-16 ⟼ larger surface, smaller pitch, optimised pixel, JTAG, more testability**

Pixel characteristics (still under study) :

- ✳ pitch : 18.4 μm (compromise resolution/pixel layout)
- ✳ diode surface : $\sim$ 10–15 μm^2 to optimise charge coll. & gain
- ✳ 64 columns ended with discriminator
- ✳ 4–8 columns with analog output for test purposes
- ✳ $\geq$ 6 sub-matrices : $\geq$ 3 pixel designs w/o ionising rad. tol. diode

  ⇛ active digital area : 64 x 384–576 pixels (8.3–12.5 mm^2)

Testability (still under study) :

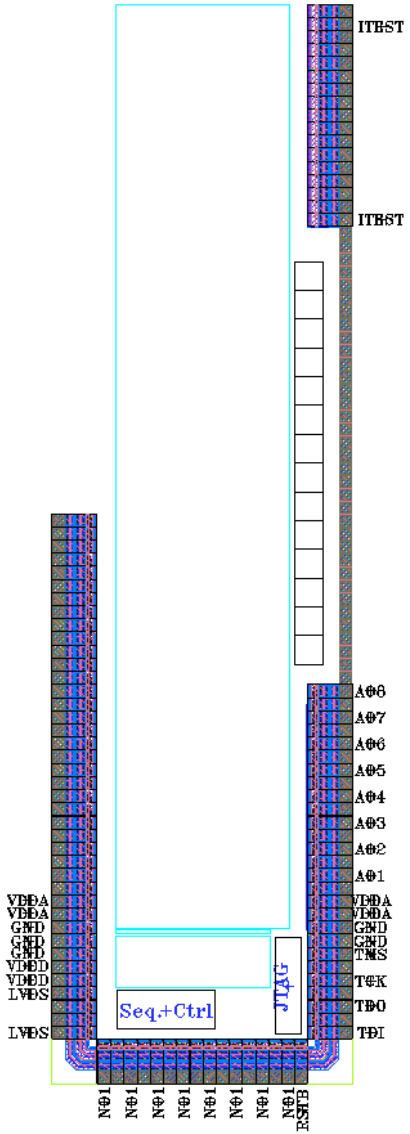
- ✳ JTAG + bias DAC ⟼ programmable chip steering
- ✳ 2 additionnal DC voltages to emulate pixel's output

  for independent discriminator performance assessment
- ✳ output frequency $\leq$ 40 MHz

Status :

- ✳ Design under way at IPHC (soon also at DAPNIA ?)

  ↪ submission end of Sept. '07 (?)
- ✳ Funding (20–30 keuros) via IPHC ressources for STAR & CBM

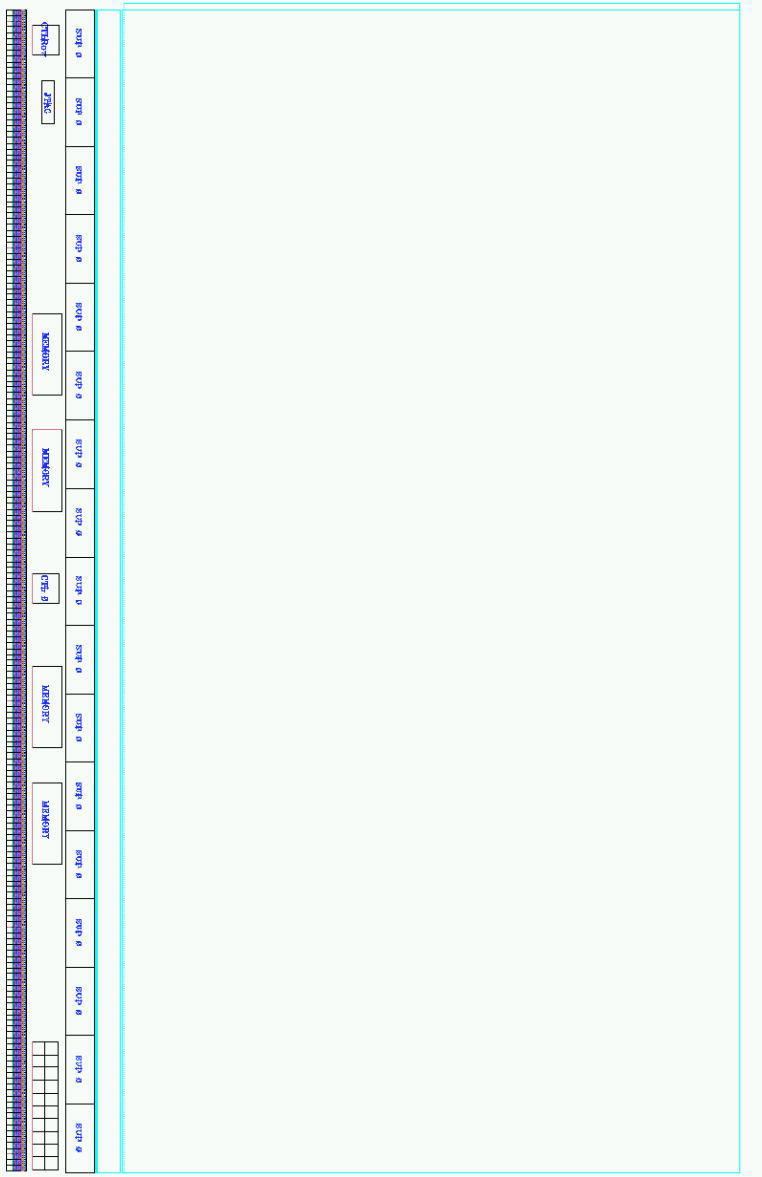


Spring 2008 : MIMOSA-22+

- MIMOSA-22 complemented with $\emptyset$ (SUZE-01)
- 1 or 2 sub-arrays (best pixel architectures of MIMOSA-22)
- larger surface : active surface $\sim$ 0.5 cm^2
  - final column depth (576 pixels)
  - $\gtrsim$ 1/4 of final number of columns ($\geq$ 256 / 1088)
- total surface $\lesssim$ 5.5 x 12 mm^2 $\rightarrow$ 50 – 55 keuros

  $\hookrightarrow$ available funding : EUDET (27 keuros) $\&$ STAR/CBM (rest)

- ▶ opportunity for engineering run (100 keuros) combining various chips



End 2008 / early 2009 : Final chip

- Extension of MIMOSA-22+
- Active surface : 1088 columns of 576 pixels (20.0 x 10.5 mm^2)
- Read-out time $\gtrsim$ 100 μs
- Chip dimensions : 20 x 12 mm^2
- Engineering run : $\sim$ 120 keuros for 6 diced and thinned wafers

  $\hookrightarrow$ available funding : EUDET (70 keuros) & STAR/CBM (50 keuros)

SUMMARY

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- MIMOSA-16 tests under way :
  - analog part (epi-14) : tests started at DAPNIA $\rightarrowtail$ CCE (epi-14) $\lesssim$ 3/2 CCE (epi-20)
  - digital part (epi-20 & -14) : $\geq$ May at IPHC
  - beam tests : $\gtrsim$ 4 Septembre at CERN (T4 - H6)
  - 2nd wafer production finished : small doubts about quality $\rightarrowtail$ negociations with AMS
- $\emptyset$ suppression micro-circuit :
  - design under way at IPHC (sets of 64 columns, tolerates close to 10^3 hits/cm^2/frame)
  - submission to foundry by end of June
  - test completed by end of year $\rightarrowtail$ in time for integration in final prototype (MIMOSA-22+)
- Milestones until final chip well identified :
  - MIMOSA-22 : pitch, surface, testability, JTAG $\rightarrowtail$ subm. end Sept. '07
  - MIMOSA-22+ : surface, $\emptyset$ $\rightarrowtail$ subm. Spring 2008
  - Final sensor (20x10.5 mm^2, $\sim$ 100 μs) : end 2008 / early 2009
- Resources :
  - manpower : design OK – tests (what outside IPHC ?)
  - chip + PCB fab. funding ($\sim$ 200 keuros): 106 keuros (EUDET) + rest (IPHC + ?)