# Vertex detector @ ILC

## Monolithic technologies for pixel detectors

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# Content

- Physics requirements for the ILC vertex detector
- Technologies and architectures
  - DEPFET
  - CCD
  - CMOS
  - SOI / 3D
- Conclusion

# Main goal of the ILC vertex

- **Determination of the branching ratios of the Higgs boson to fermions and bosons**
  - ☐ Particularly critical is the measurement of the coupling to charm in a very large b background
  - ☐ Precise measurement of the $\Gamma_{bb}/\Gamma_{cc}$ is discriminating among SM or SUSY Higgs

$$\sigma_{ip} = a + b \,/\, p\sin^{3/2}\theta$$

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# How to get there

$$\sigma_{ip} = a + b \,/\, p\sin^{3/2}\theta$$

a ≤ 5 μm
b ≤ 10 μm

- **Parameter a:**
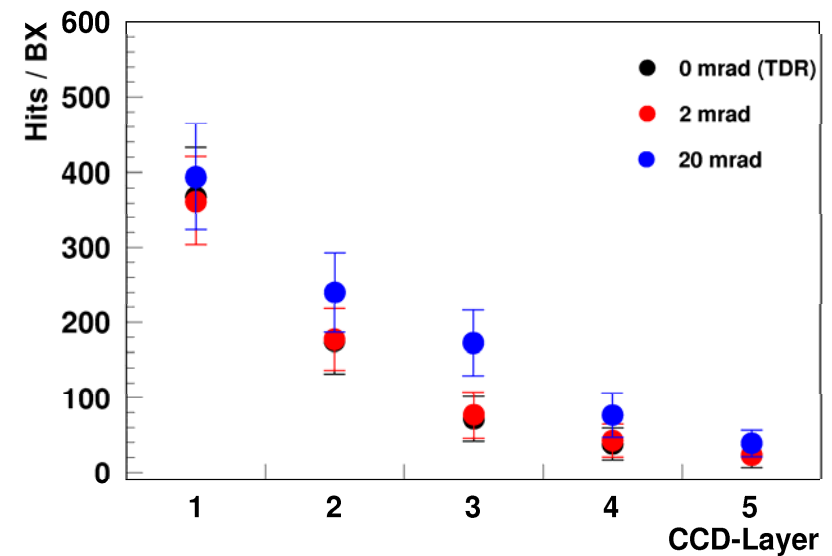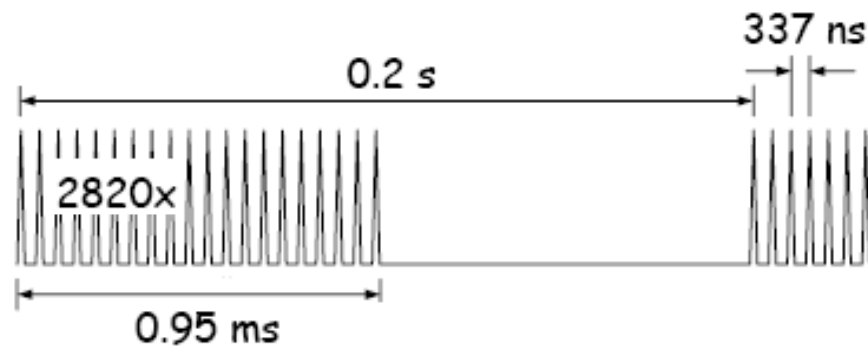  - Pixel pitch       20 μm x 20 μm
  - Inner and outer layer radii      1.5 cm x 6.0 cm
- **Parameter b:**
  - Material budget of the inner layer      0.1% $X_0$ / layer
  - Beam pipe material      0.4% $X_0$

**In other words it has to be monolithic!!!**

# Machine related constraints / 1



- **Triggerless**
  - 1 high energy event every 10 train
  - This is also physics driven, since nothing has to be wasted
- **One train every 200 ms**
- **3000 bunch per train lasting 1 ms**
  - Reasonably short inter-bunch and long inter-train time
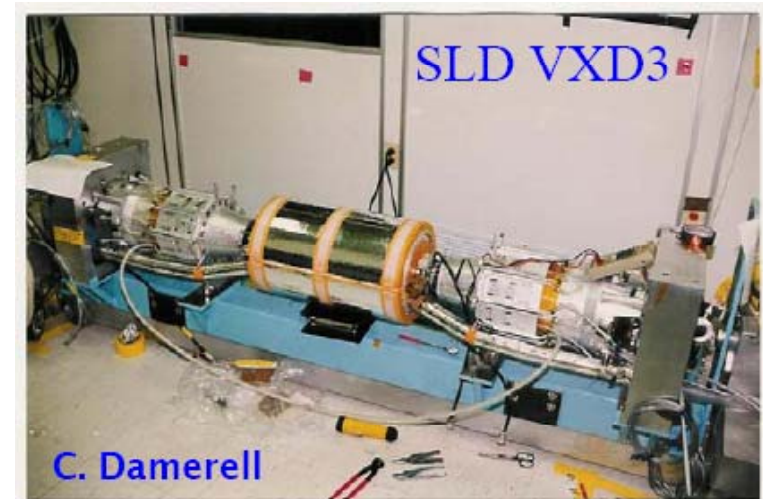- **Machine background**
  - Deeply investigated

# Machine related constraints / 2

- **Radiation hardness**
  - $10^9$ n/cm$^2$/year
  - $5 * 10^{12}$ e$^-$/cm$^2$/year
- **EMI compliant**



SLD VXD3

C. Damerell
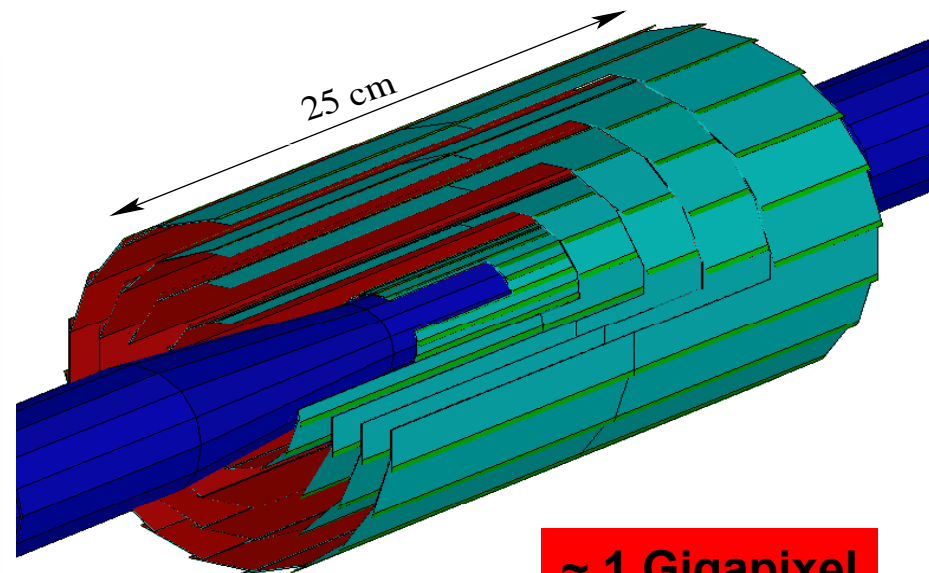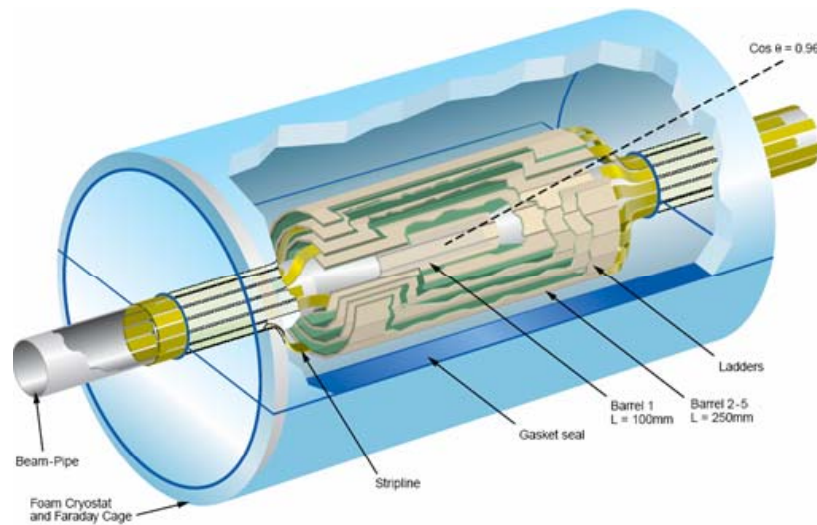
  - According to previous experience, EMI can disallow the readout in the inter-bunch time
  - If the Faraday cage is not enough, an In Situ Storage architecture might be required.

# General vertex design

- Considering all these constrains we end up with a vertex detector that is design independent but technology dependent!



~ 1 Gigapixel

# Technology and architecture R&D

- There are several teams working on different (monolithic) detector technologies trying to implement architectures suitable for the ILC environment

| Arch/Tech | Parallel Column | In situ storage | Sparse data scan |
|---|---|---|---|
| CCD | LCFI (UK) | ★ LCFI-ISIS | - |
| CMOS | ★ IRES (Strasbourg) | RAL-FAPS | ★ Not impossible |
| DEPFET | ★ MPI-Bonn et al | - | - |
| 3D / SOI | ★ MIT / INFN & Hamamatsu | Possible | Possible |

**Credits slide at the end…**

# DEPFET working principle

- A **p-FET** transistor is integrated in every pixel
- A **potential minimum for electrons** is created under the channel by **sideward depletion**
- Electrons are collected in the „internal gate" and **modulate the transistor current**
- Signal charge is removed via a clear contact
- **Fast** signal collection in **fully depleted** bulk
- **Low noise** due to small capacitance and first amplification
- Transistor can be **switched off** by external gate – charge collection is then still active !
- Readout can be at the source ('voltage signal') or at the drain ('current signal') – **ILC uses drain readout**



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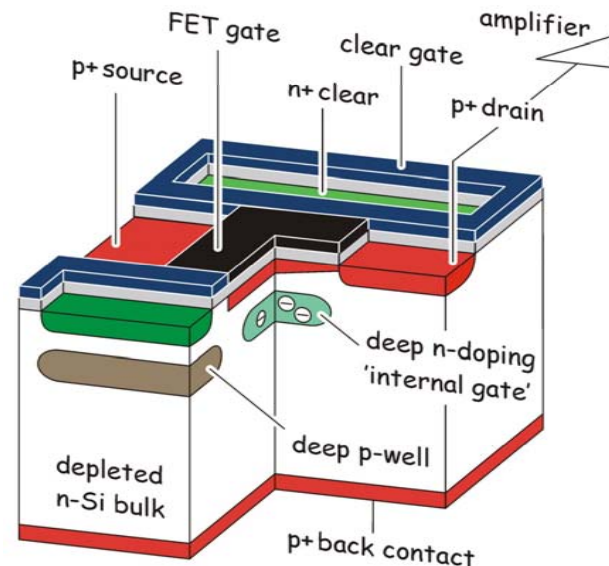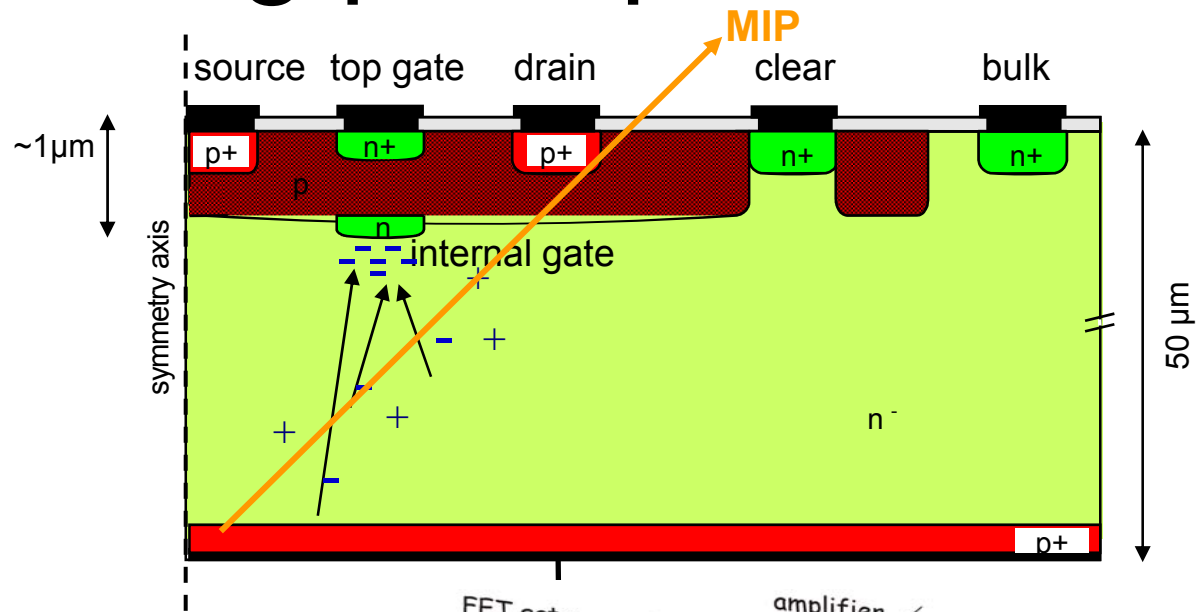
# DEPFET proto

- ## Not really monolithic!
  - □ Gate and clear switcher need for pixel addressing and reset.
  - □ Two wire bondings for each row and one for each column are required
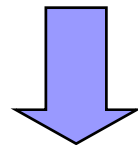  - □ Resetting (clear) may require "high" voltage

- ## CUrrent Read Out chip
  - □ With real time zero suppression
  - □ Each pixel charge is read locally and not shifted



Gate Switcher

DEPFET Matrix
64x128 pixels, 36 x 28.5μm$^2$

Clear Switcher

Current Readout
CURO II
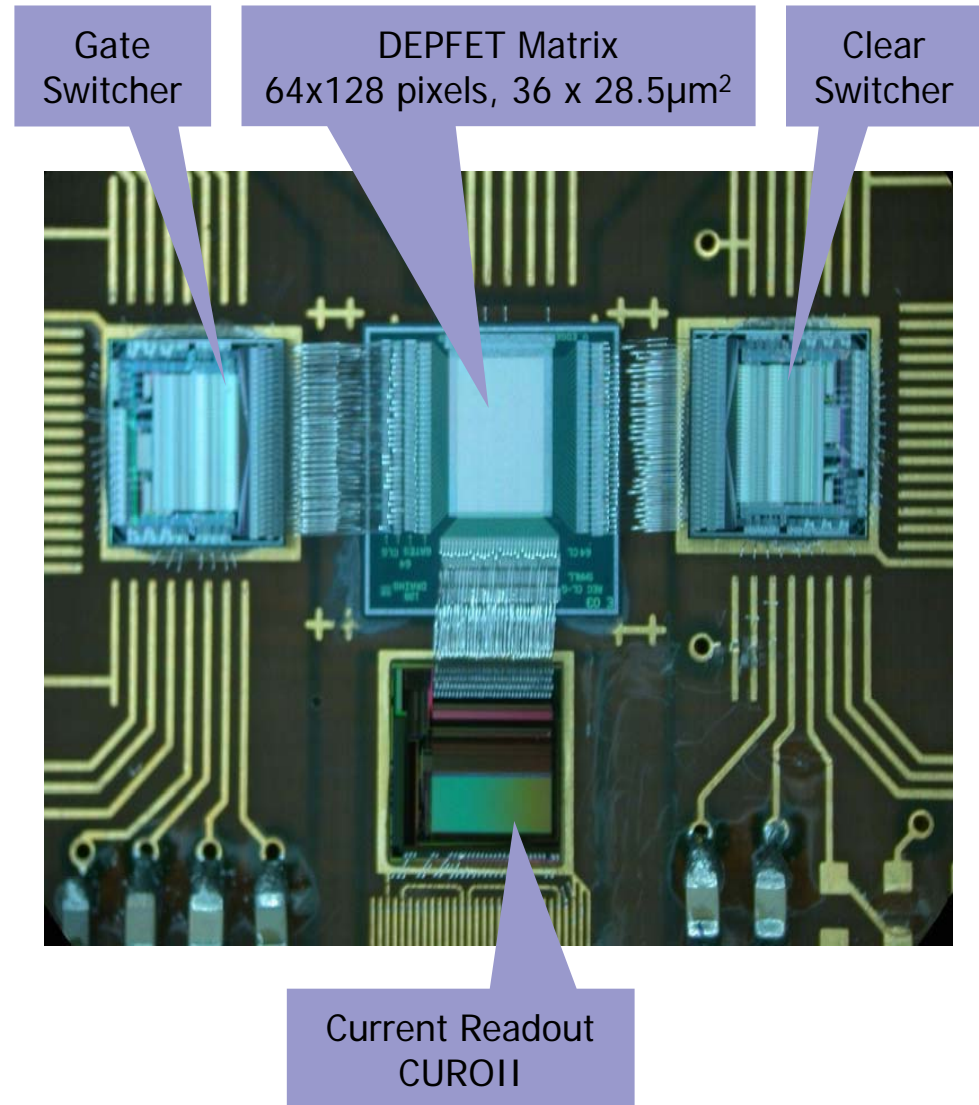
# DEPFET test beam @ DESY

- 4GeV e- beam (multiple scattering ☹)
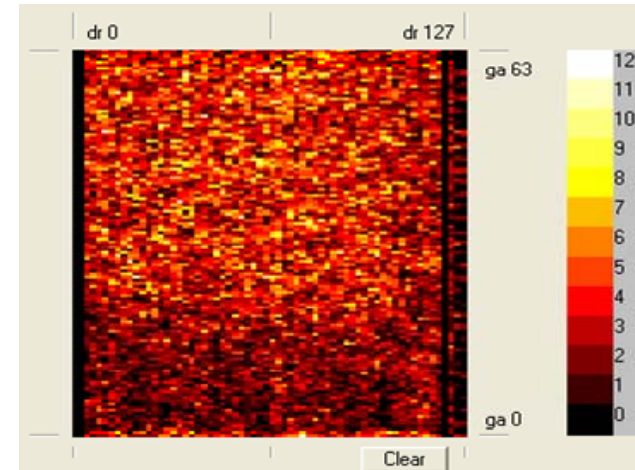- Reference Si strip telescope
- Tested matrices with 64 x 128



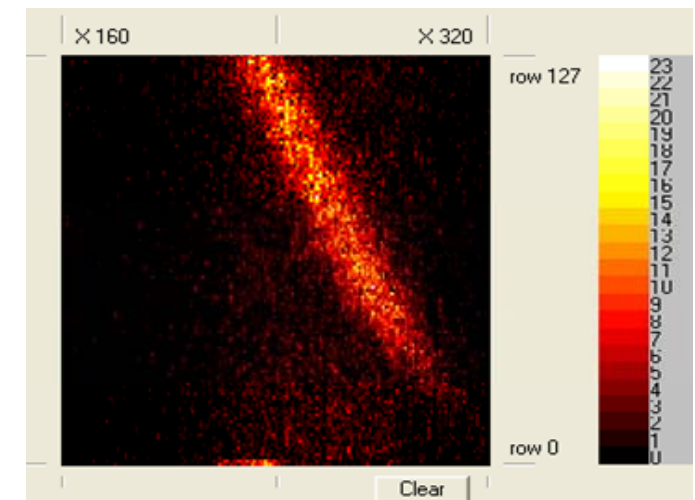Beam spot on (small) DEPFET

**400** μm thick sensor!

## RESULT SUMMARY

- Resolution x = 4.2μ, y = 1.5μ
- Efficiency    = 99.75% with a 5σ seed cut
  = 99.96% with a modest $\chi^2$ selection cut
- Using this number in a Geant4 simulation for the vertex you get:



correlation telescope x ⟺ DEPFET x

$$\sigma_{ip} = 2.4\mu m + 7.2\mu m / p\sin^{3/2}\theta$$

# DEPFET thinned sensor



1. implant backside on sensor wafer
2. bond wafers with $SiO_2$ in between
3. thin sensor side to desired thick.
4. process DEPFETs on top side
5. etch backside up to oxide/implant
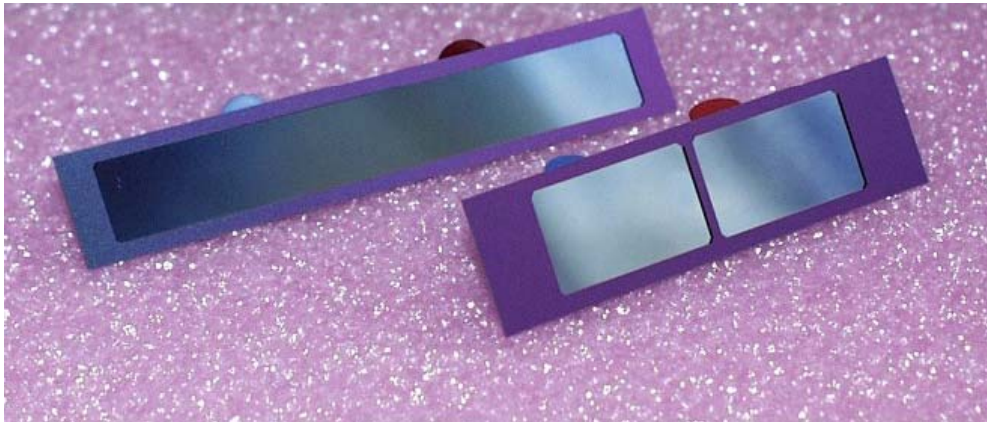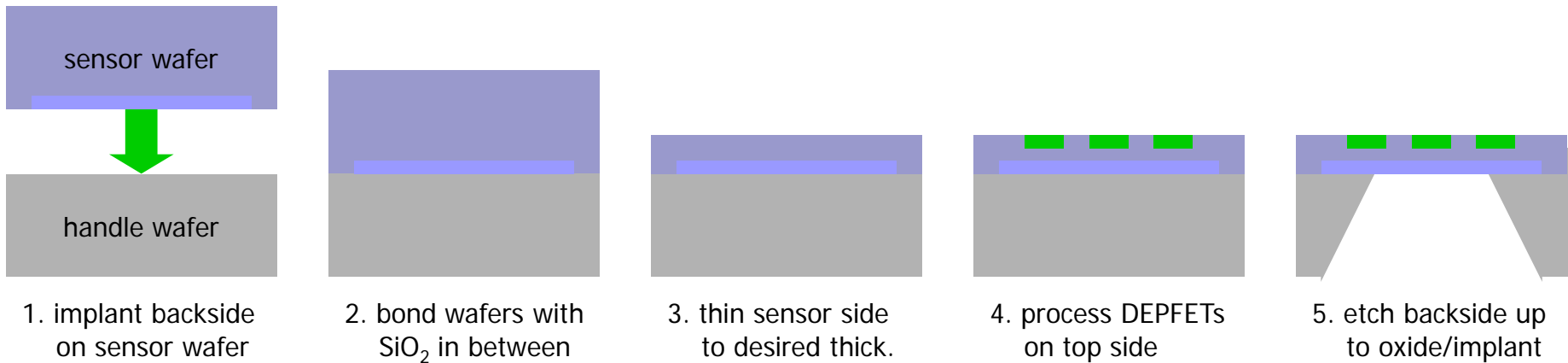


first 'dummy' samples:
50μm silicon with 350μm frame
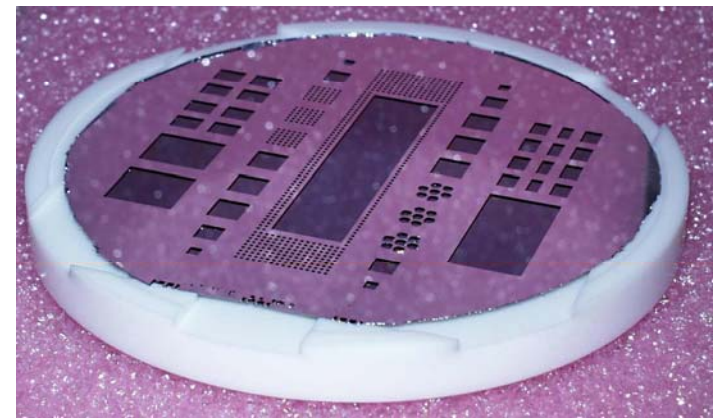


thinned diode structures:
leakage current: <1nA /cm²

# DEPFET conclusion & outlooks

- Most mature technology and very well advanced

- Verify the performance after thinning down to the target thickness

- Simplifying the hybridization scheme

# CCD for the ILC

- CCD sensor was used in the SLD experiments were an impact parameter resolution similar to the ILC required one was obtained.

$$\sigma_{ip} = 8\mu m + 33\mu m/p\sin^{3/2}\theta$$

- There are two main groups working on CCD
  - □ LCFI (UK) on parallel column and ISIS
  - □ GLD (Japan) on fine pitch CCD (5μm x 5μm)
- Even if the CP-CCD is still the most active topic, I will give you some hints about the ISIS
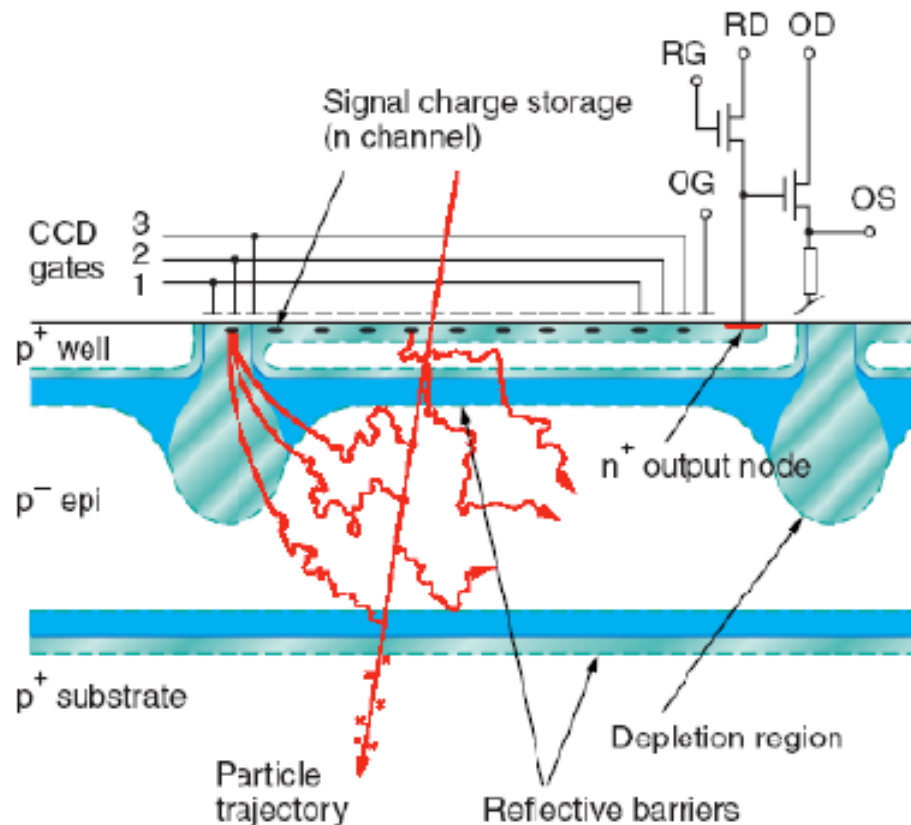
# In-situ Storage Imager Sensor

- Signal production and collection in solid state detector is a very process
- The long lasting procedure is the signal readout
- So, store the signals in the sensor and transfer of all them afterward
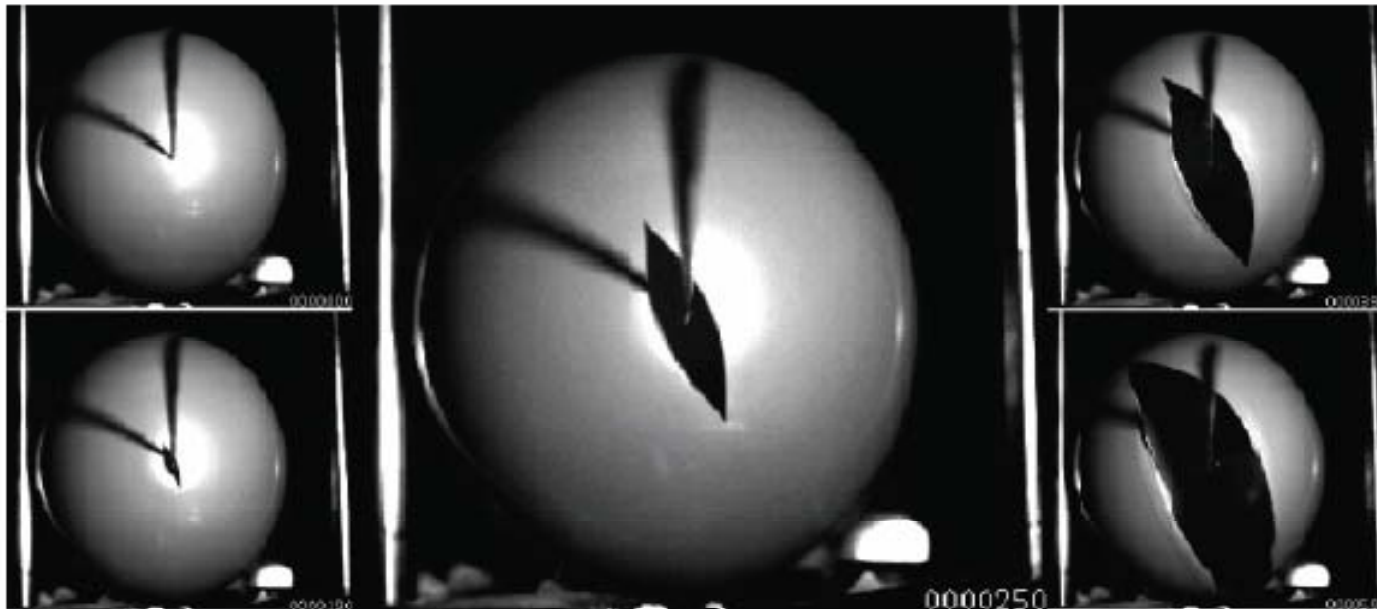


- **2003: Dart bursting a balloon: 100 consecutive frames at 1M frame/sec**
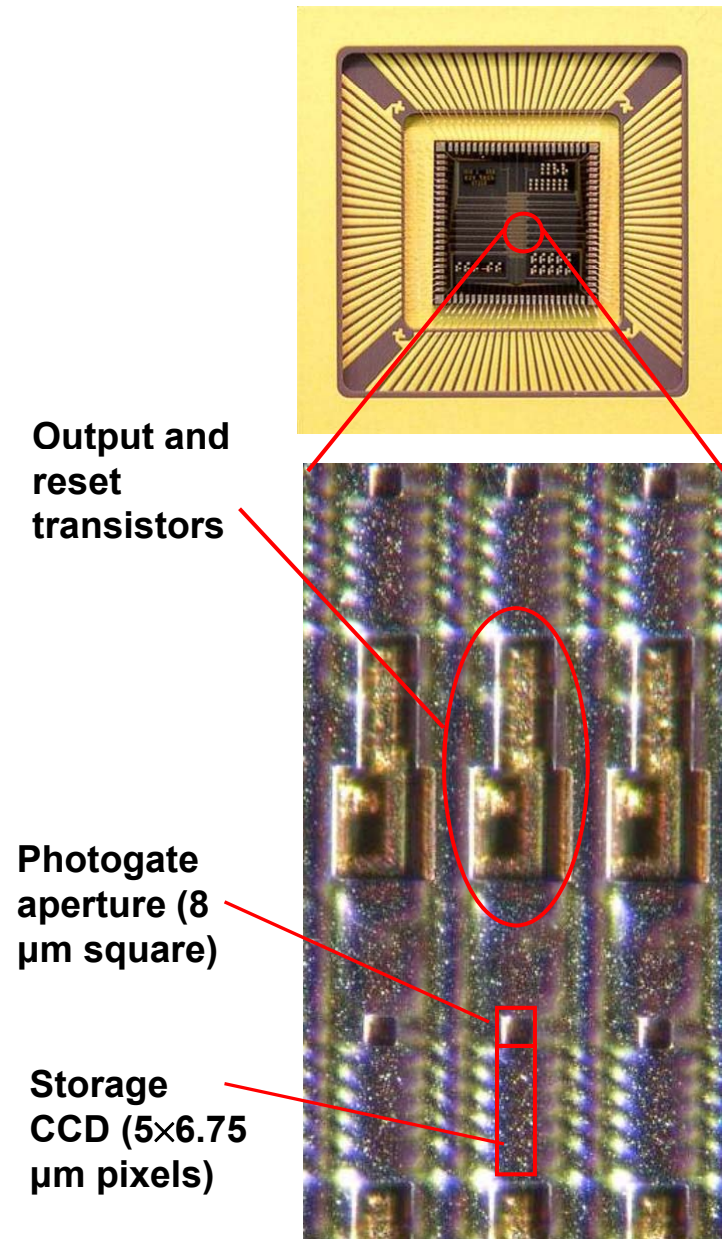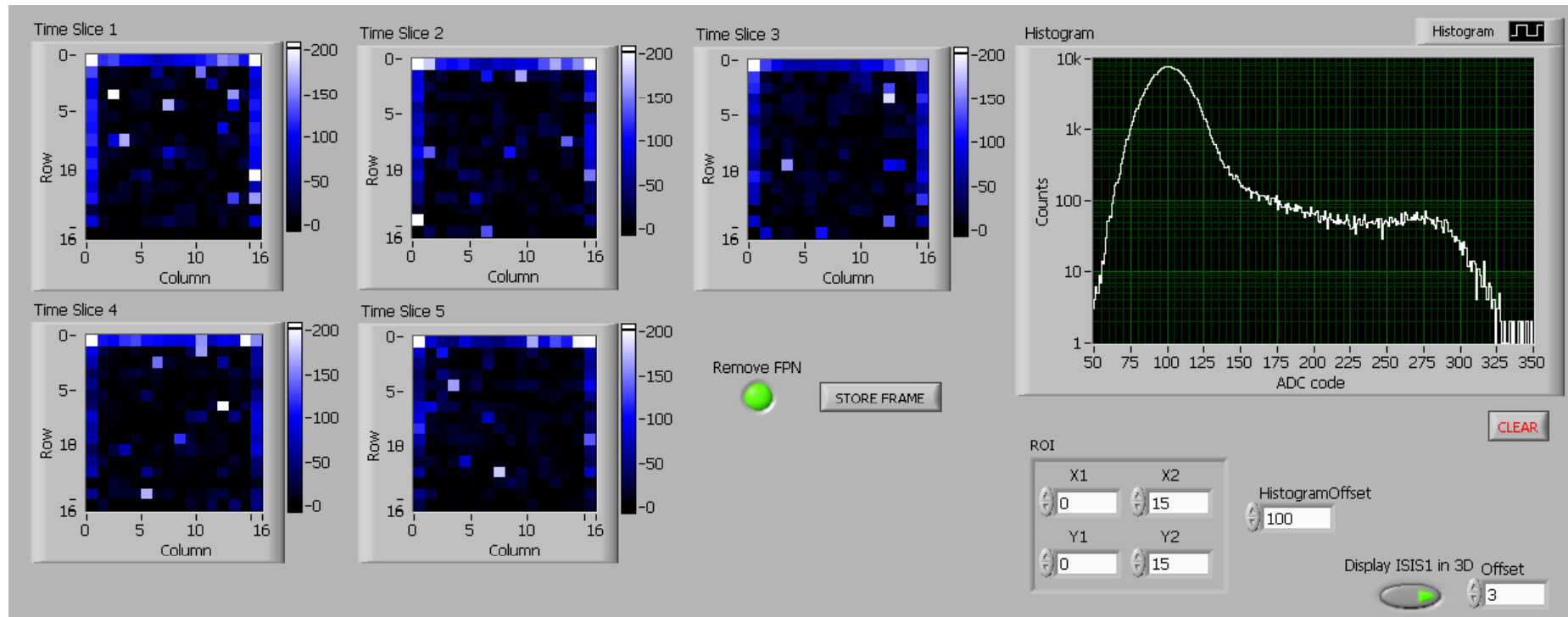
# ISIS: In situ storage CCD



- Beam-related RF pickup is a concern for all sensors converting charge into voltage during the bunch train
- Charge collection to photo gate from ~20μm as in conventional CCD
- Signal charge shifted into the storage register during the bunch
- Readout of the storage register in the inter train time

# ISIS Proto: ISIS1



- "Proof of principle" device (ISIS1) designed and manufactured by e2V Technologies

- 16 ×16 array of ISIS cells with 5-pixel buried channel CCD storage register each

- Cell pitch 40 µm × 160 µm, no edge logic (pure CCD process)

- Chip size ≈ 6.5 mm × 6.5 mm

**Output and reset transistors**

**Photogate aperture (8 µm square)**

**Storage CCD (5×6.75 µm pixels)**

# ISIS1 tests with $^{55}$Fe



- The top row and 2 side columns are not protected and collect diffusing charge
- The bottom row is protected by the output circuitry
- Results are encouraging even if there some technological issues to be understood (ISIS1 controlling the transistor threshold).
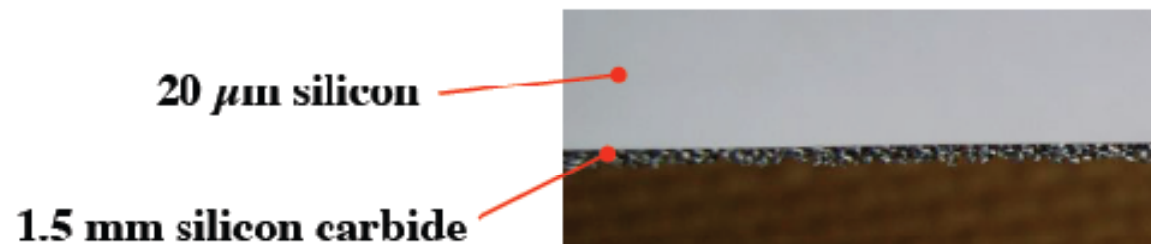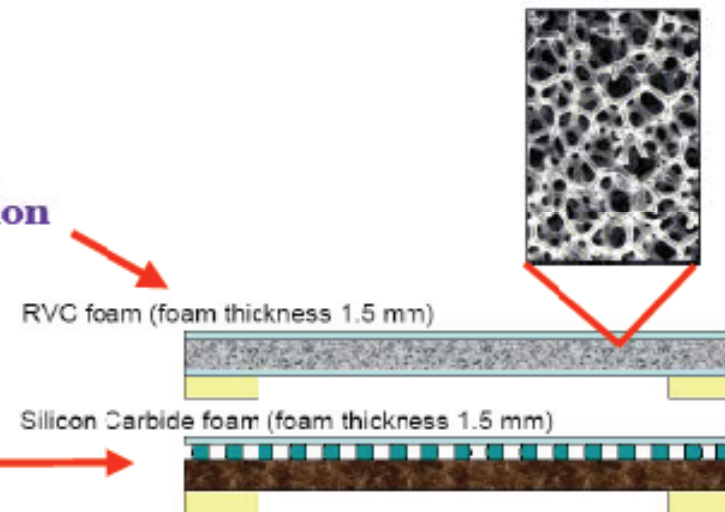
# CCD Mechanics

- **3% RVC Sandwich**
  - 0.09% $X_0$
  - Working on glue application



RVC foam (foam thickness 1.5 mm)

- **8% Silicon Carbide**
  - 0.14% X0
  - 3-4% believed possible

Silicon Carbide foam (foam thickness 1.5 mm)

20 $\mu$m silicon

1.5 mm silicon carbide

# CCD conclusion and outlooks

- This is the traditionally favorite candidate because it did already very well in the past. Excellent previous experience

- Verify how reliable are the column // readout and the ISIS architectures

# CMOS sensor for the ILC: MAPS

- p-type low-resistivity Si hosting n-type "charge collectors"

  - signal created in epi layer
  - $Q = 80$ e-h / μm $\rightarrow$ signal .~1000 e
  - excess carriers propagate (thermally) to diode with help of reflection on boundaries
  - charge sensing through n-well/p-epi junction

- Specific advantages of CMOS sensors:

  - Signal processing circuits integrated on sensor substrate (system-on-chip)
  - Sensitive volume ( epitaxial layer) is 10–15 μm thick $\rightarrow$ thinning to ~ 30 μm permitted
  - Standard, massive production, fabrication technology $\rightarrow$ cheap, fast turn-over
  - Attractive balance between granularity, mat. budget, rad. tolerance, r.o. speed and power dissipation



NMOS only
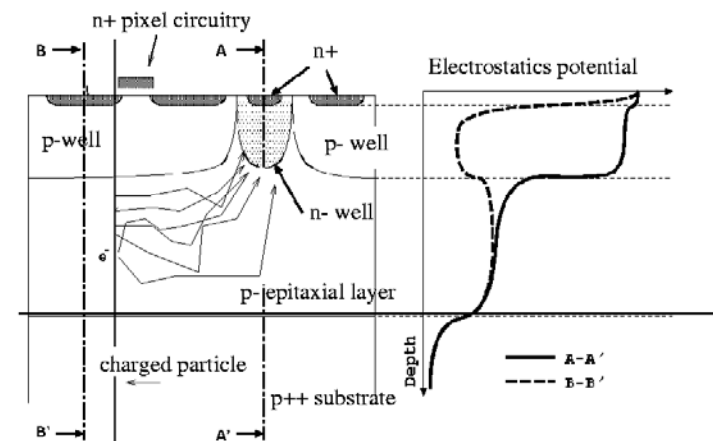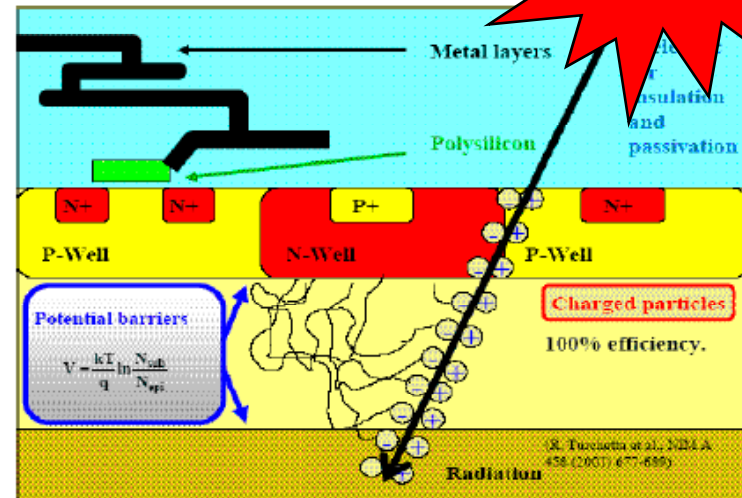
# World Wide CMOS

- **CMOS designers:**
  - Europe: IRES, DAPNIA, RAL, Grenoble, INFN (Rm3, Pv, Pi)
  - USA: LBNL, BNL, Oregon – Yale (Sarnof), Univ. Hawaii

- **CMOS characterization:**
  - DESY, Univ. Hamburg, GSI, Univ. Frankfurt, Univ. Geneva, INFN (Mi, Fe)

- **Why?**
  - Because CMOS sensors are relatively easy to do and they offer lots of interesting features that can be implemented (and tested!).
  - There are several deep sub-micron technologies available on the market to be explored

# "Standard" CMOS: the Mimosa family

- CMOS for particle detection was firstly used at Strasbourg with the Mimosa 1 chip. Currently designers are working on Mimosa 22

- Already tested many different technologies and architectures with well established performances
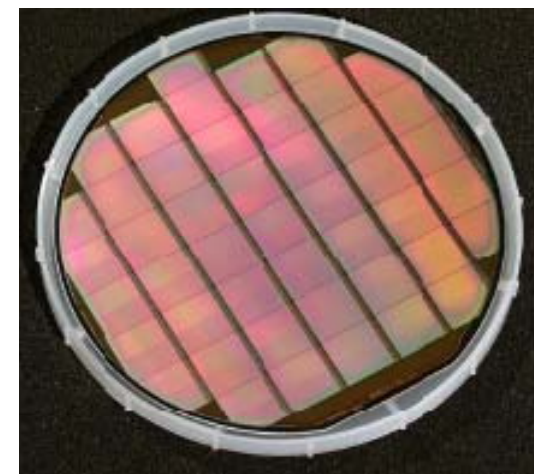
**SUMMARY**

- **Best performing technology:** AMS 0.35 opto

- **Noise:** 10 e$^-$

- **SNR for a MIP**: 20 – 30 (MPV)

- **Detection efficiency:** 99.5%

- **Operating temperature:** up to 40º

- **Single point resolution:** down to 1.5 μm



Mimosa 9. Efficiency VS Fake
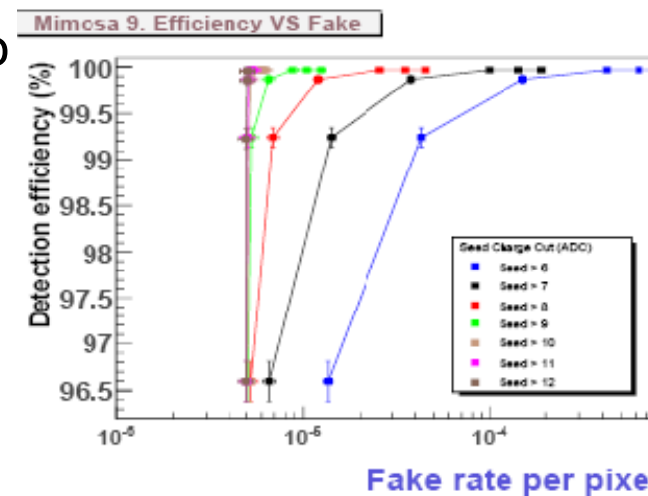
# CMOS development for the ILC

- **Thinning and ladders**
  - Several thinning attempts: easy down to 50 µm, going further trickier, but still possible.
  - Ladder prototype with 9 full area sensors mounted and tested in LBNL for STAR detector upgrade

- **High readout speed**
  - Parallel column readout
  - Zero suppression with simple pixel over threshold algorithm and binary output
  - 3 or 4 bit ADC integrated on the same chip

- **Radiation hardness**
  - **Neutron irradiation** up to $10^{12}/cm^2$ $\rightarrow$ 5% efficiency loss, modest increase of leakage current and 10% noise increase
  - **Ionizing radiation:** ok for X-ray with a specific design (500 krad) still to be investigated the effect of low energy electrons.

# Exotic CMOS development

- CMOS MAPS with hybrid-pixel-like analogue readout electronics in a 130 nm triple well process (INFN – PV + PI)
- Overcoming the only n-MOS limitation
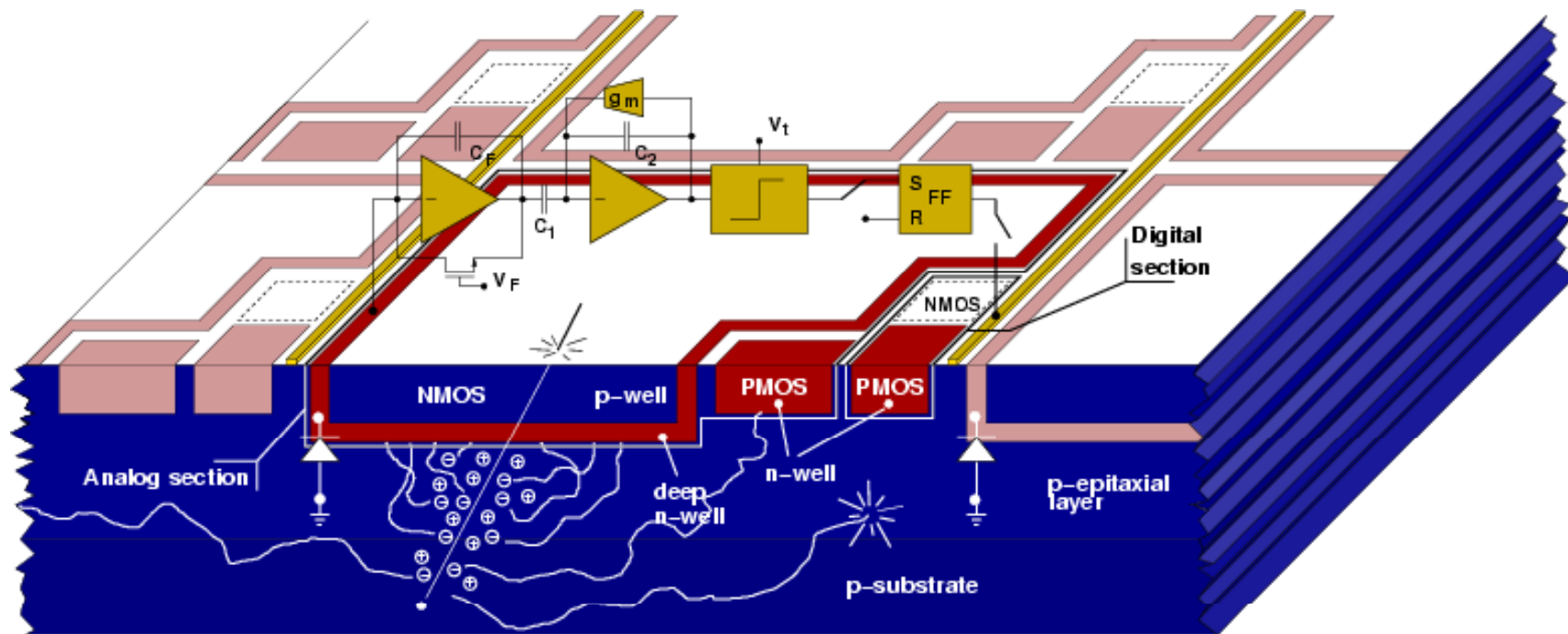
# CMOS conclusions & outlooks

- CMOS is a very appealing alternative to CCD
- This is most active technology in the vertex community
- Compare among different approaches:
  - Parallel column readout with digital / binary output
  - Sparsification at chip level
  - In situ storage (FAPS)
- The upgrade of the STAR vertex detector with CMOS sensors will help a lot system integration

# SOI & 3D: the runner-ups

- **The idea:**
  - ☐ standard readout electronics is silicon made
  - ☐ standard fully depleted sensors are silicon made
  - → Glue them together!
- **Why stopping at two layers?**
  - → Tile up all the layers you need = 3D electronics!
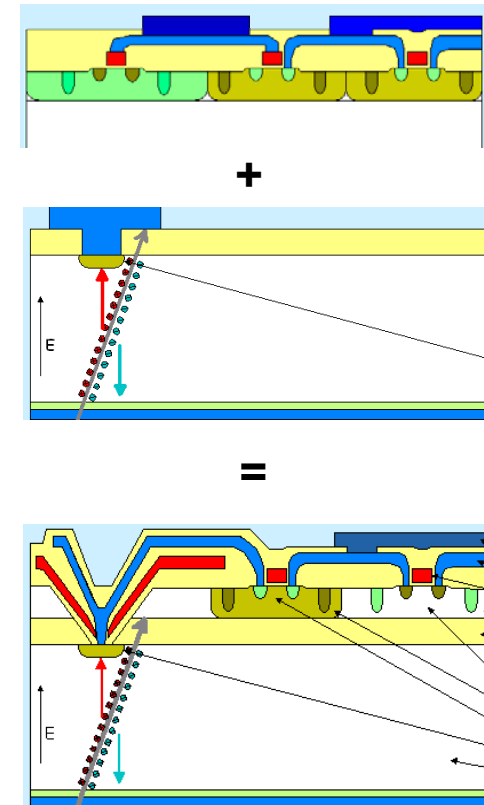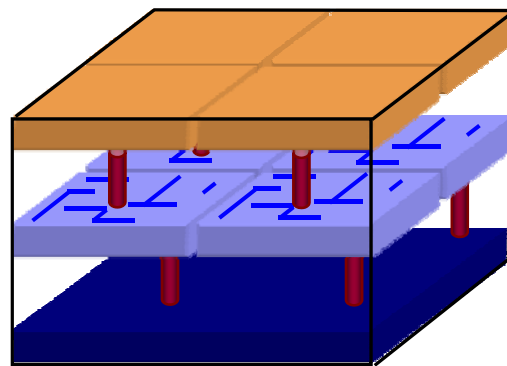
# SOI: Silicon On Insulator

- In the SOI technology, two silicon wafers are bonded together with a $SiO_2$ in between
- The bottom layer is usually used only as a mechanical support, but in our application, it can be used a detection medium while in the upper one whatever electronics can implemented.
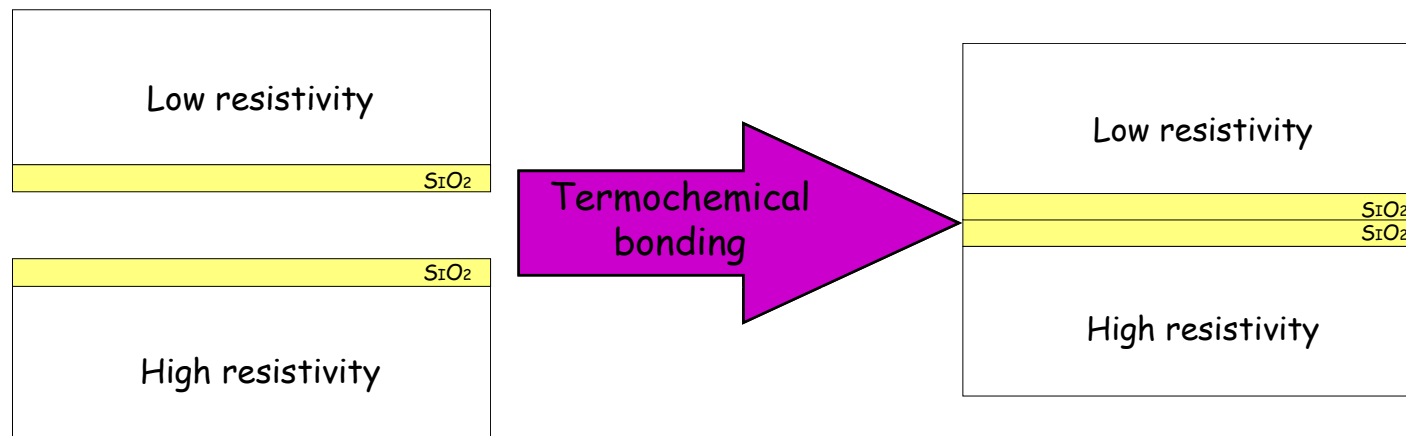
# SUCIMA experience

- SUCIMA was a Fifth Framework program funded project aimed to develop a monolithic real time radiation dosimeter in medical applications.

- IET in Warsaw carried on the technological development to integrate on a SOI substrate both the collecting p-n junction and the standard CMOS process



$^{90}$Sr Beta spectrum
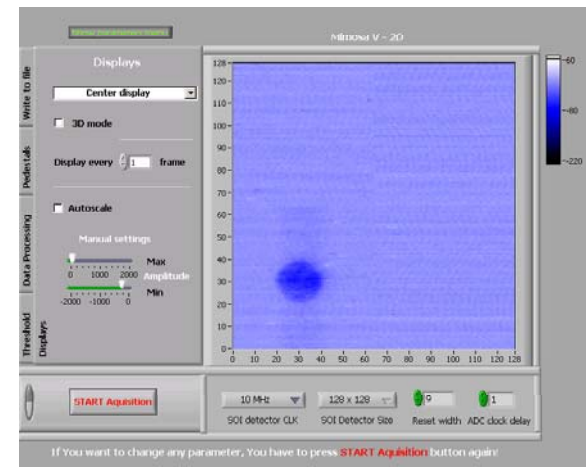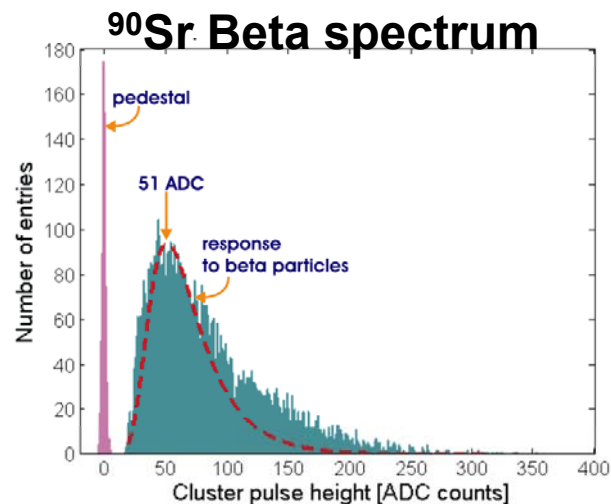
# SUCIMA results

- Pretty low yield mainly due to the bad quality of the target SOI wafers.
  - Having SOI wafer with high resistivity handle wafer is troublesome especially if you only need a few wafers batch
- Available technology at IET is too old and need to be updated in order to be compliant with the ILC requirements
- A new technological development has been started with some former SUCIMA partners, INFN and Hamamatsu.
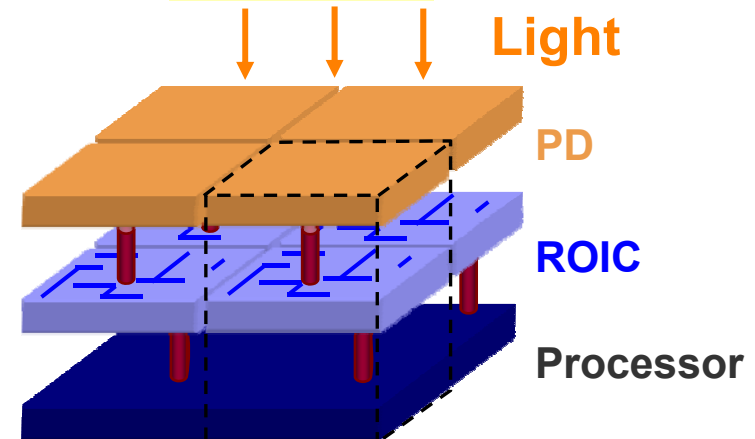
# Going 3D (MIT + Lincoln Lab)

## Conventional Monolithic APS
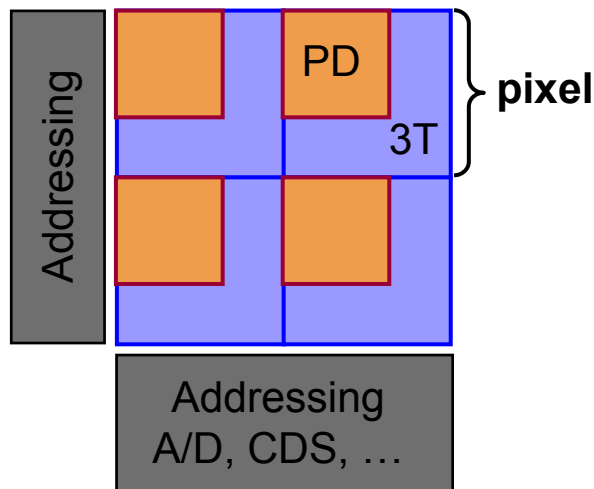


- Pixel electronics and detectors share area
- Fill factor loss
- Co-optimized fabrication
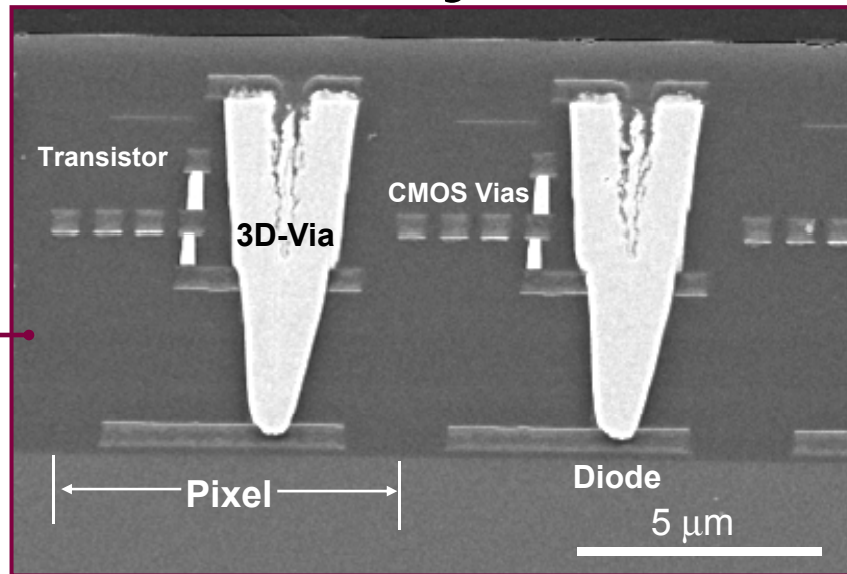- Control and support electronics placed outside of imaging area

## 3-D Pixel



- 100% fill factor detector
- Fabrication optimized by layer function
- Local image processing
  - Power and noise management
- Scalable to large-area focal planes

# Sci-fi or reality?



Bond Interface

Transistor

CMOS Vias

3D-Via

Pixel

Diode

5 µm

- A 1MPixel CMOS sensor has been produced using a quasi standard 3T design with collecting diode on a different substrate interconnected through 3D vias

# SOI/3D conclusions & outlooks

- Even if close to sci-fiction they are already true!

- Of course they are the last born technologies but we don't have to decide today which will be the vtx detector technology

- If they won't be mature enough for the ILC, they will be for the next

# Conclusion

- The ILC vertex detector is characterized by a very demanding impact parameter resolution.

- This is requiring a step forward in the development of monolithic sensor technology.

- Several different approaches are now being studied and the competition is increasing.

- There will be one winner only, but no losers!

# Credits

- **DEPFET**
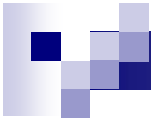  - Si-LAB Bonn - N. Wermes, http://siliconlab.physik.uni-bonn.de/
- **CCD**
  - LCFI (UK) – T. Greenshaw, C. Damerell http://hepwww.rl.ac.uk/lcfi/
- **CMOS**
  - IPHC, M. Winter http://ireswww.in2p3.fr/ires/web2/-CMOS-ILC-.html
  - INFN, V. Re et al.
- **SOI**
  - SUCIMA, M. Caccia
  - 3D MIT – Lincoln Lab http://www.ll.mit.edu
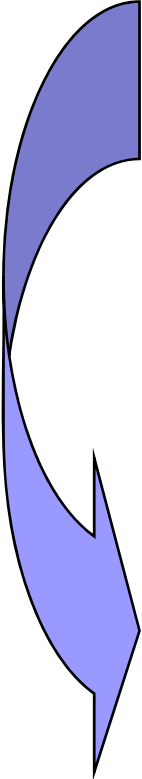
# Backup

# Loop the loop…

- The machine background is determining the readout speed
- The readout speed is constraining the geometry modularity
  - Was 8 in the Tesla TDR now is 20 considering // col ro and readout every 20 μs in the innermost layer.
- The mechanical structures is framed by the limited material budget.
- The limited material budget requires a light cooling system, i. e. low power consumption.
- The low power consumption means:
  - Exploit the low duty cycle
  - "Reduce" the leakage current due to radiation damage
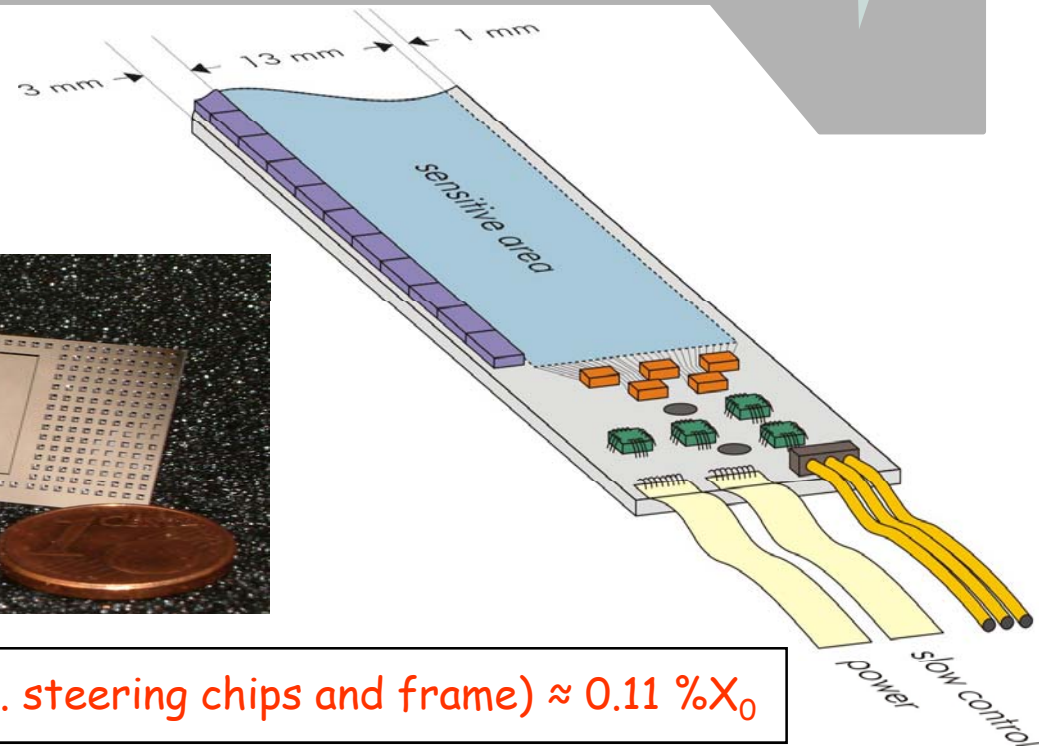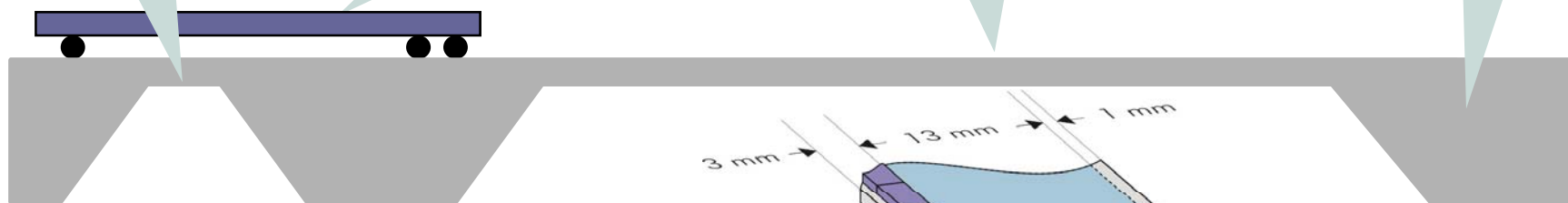  - Slow down the readout

# DEPFET ladder design

Cavities in frame can save material

Chips are thinned to 50 μm, connection via bump bonding

**Thinned sensor** (50 μm) in active area

**Thick support** frame (~300 μm)

3 mm — 13 mm — 1 mm

sensitive area

power

slow control

Material budget (1st layer, incl. steering chips and frame) ≈ 0.11 %$X_0$

# CCD ladder and mechanics

- **Unsupported silicon**
  - ☐ Longitudinal tensioning provides stiffness
  - ☐ No lateral stability
  - ☐ Not believed to be promising
- **Thin substrates**
  - ☐ Detector thinned to epi layer (20 µm)
  - ☐ Silicon glued to low mass substrate for lateral stability
  - ☐ Longitudinal stiffness still from tension
- **Rigid structures**
  - ☐ No tensioning required

# Overcome the NMOS limitation

- The main idea is to take advantage from the Triple Well available in some 130 nm technology.

- A big triple n-well as big as possible is containing a p-well with all the nMOS transistors.

- This deep n-well is acting as a collecting element, while another std and small n-well is used to contain all the pMOS.

- The presence of other n-well is introducing some collection inefficiency proportional to the ratio among the std and the deep n-well surface.

- Since both types of transistor can be used, all possible electronics can be designed as the standard CSA circuit or a complicated sparsification logic.