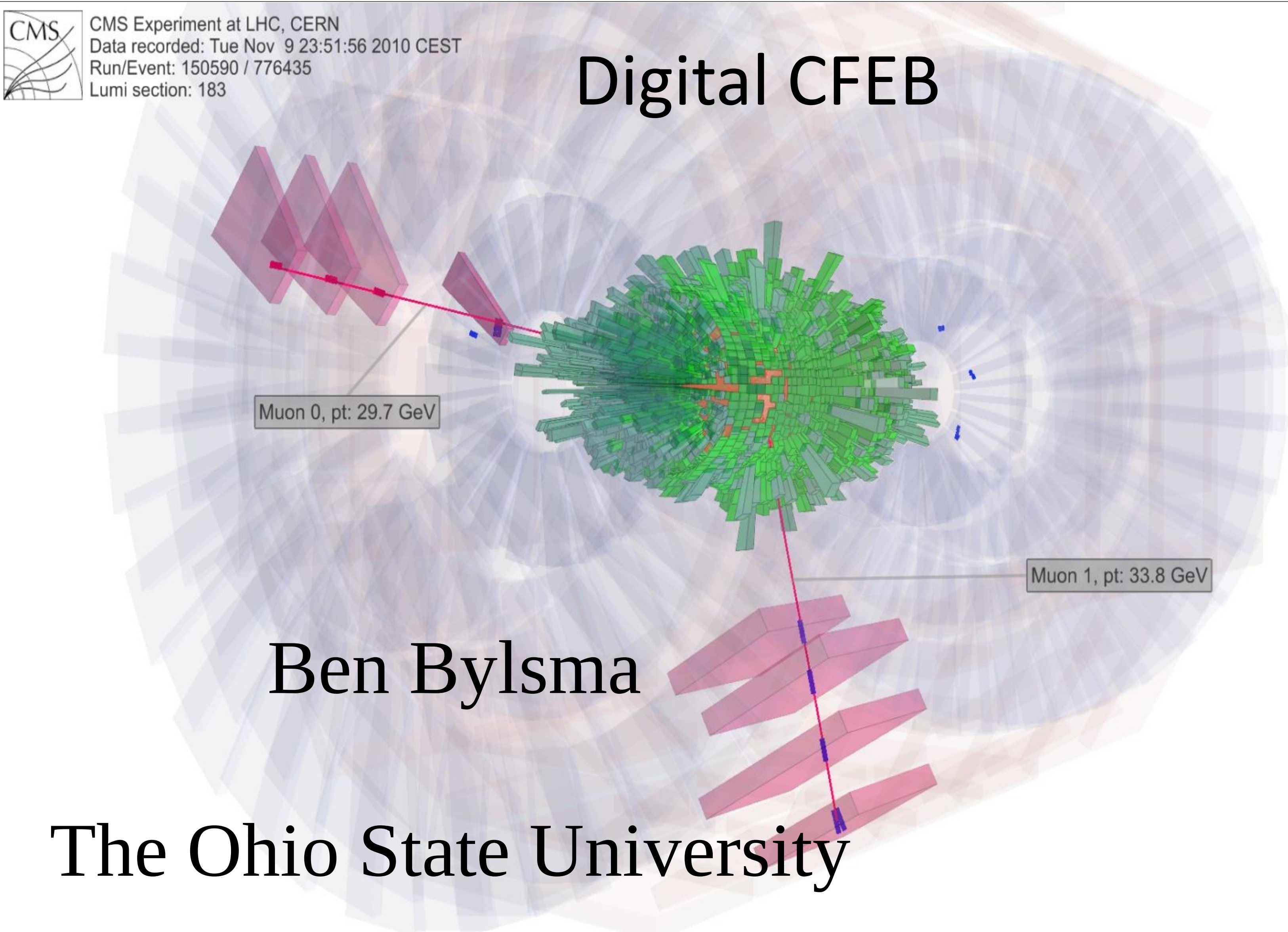
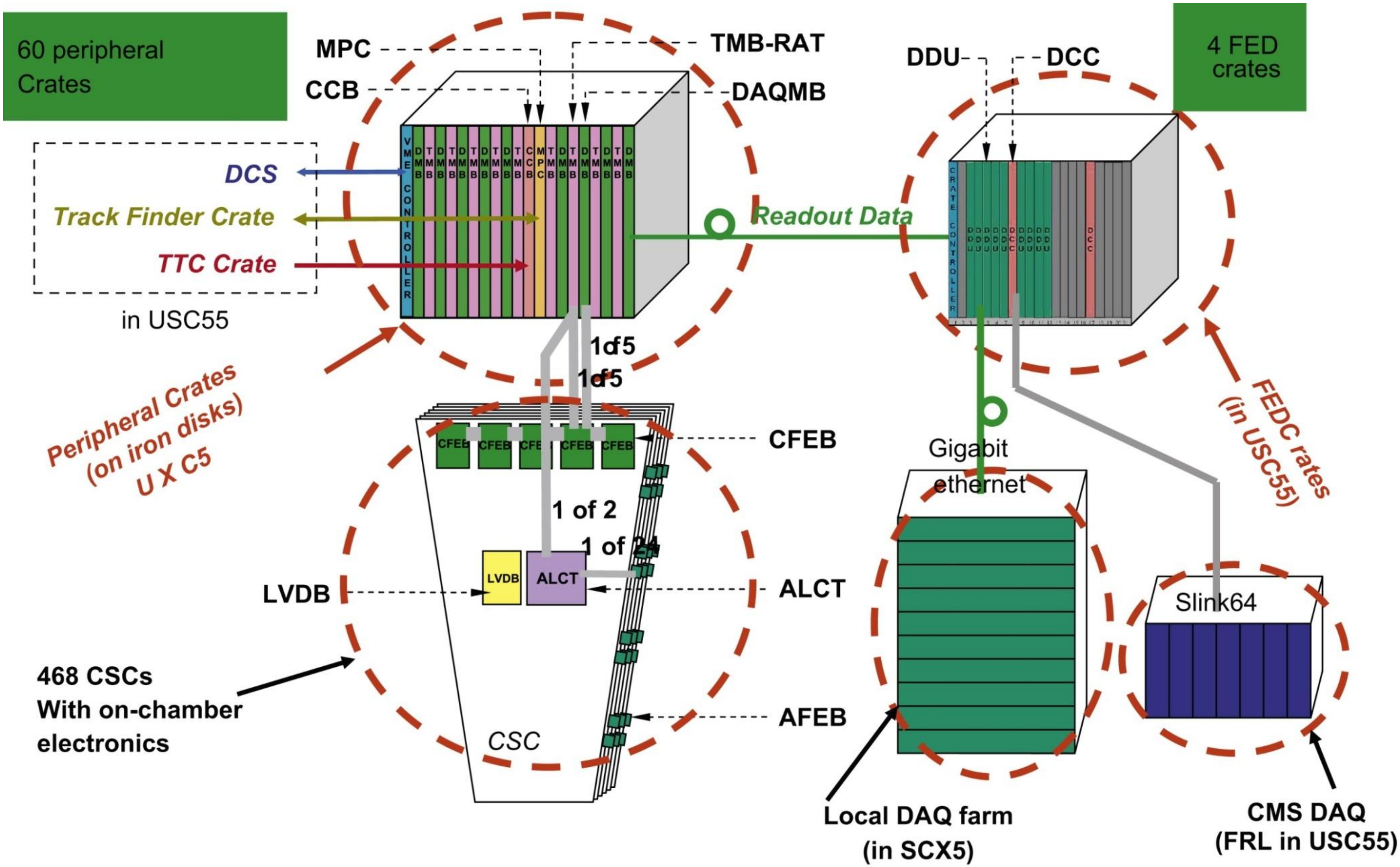
Digital CFEB



Ben Bylsma

The Ohio State University

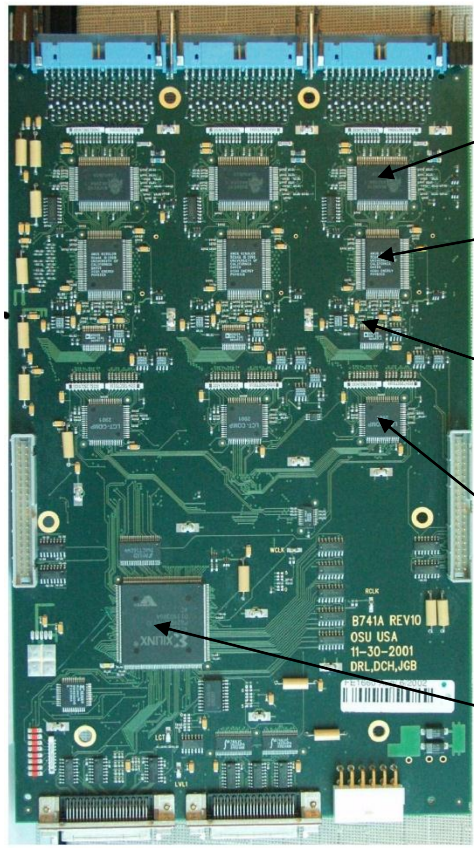
Overall View of Data Acquisition System



Cathode Front End Board (CFEB)

Optimized for Precision Position Measurement

- 5 cfebs/chamber, 96 strips/cfeb
- 96 switch capacitors/strip
- system is self triggering



BUCKEYE (ASIC) - amplifies and shapes input pulse

SCA (ASIC) - analog storage for 20 MHz sampled input pulse

ADC - events with LVL1ACC digitized and sent to DAQ Motherboard (25 nsec/word)

Comparator ASIC - generates trigger hit primitives from shaped pulse

Controller FPGA - controls SCA storage and digitization

Input/Output

Inputs	
Signal	96 channels input from chamber strips
LCT	from DMB, if CLCT is available, CLCT-->DMB-->CFEB, if CLCT is not available, -->FTC-->DMB-->CFEB, if Calibration mode, DMB-->CFEB
L1ACC	From DAQMB, - if CCB is available, CCB-->DMB-->CFEB, or CCB-->FTC-->DMB-->CFEB - if CCB is not available, FTC (LCT delay)-->DMB-->CFEB, or, DMB (LCTdelay)-->CFEB, - if Calibration mode, DMB-->CFEB;
DAC	0-5V adjustable for external, internal charge injection for BUCKEYE from DAC on DMB
BUCKEYE	+10V and -5V voltage references from DMB
Outputs	
DAQ data	Strip charge ADC data, Through 21-bit channel link to DMB
Trigger data	Comparator Triads through two 28-bit multiplexers to CLCT; End channel signals to neighboring boards, analog preamp signals and digital comparator signals
Monitor	Temperature sensor output, to DMB, program done
Controls	
Global-reset	from DMB, reset DMB and CFEBs, and synchronize the 50ns clock on DMB and CFEBs
Clock	40MHz, from DMB
FPGA-program	from DMB, re-program the FPGA from PROM on CFEB
JTAG port	from DMB, controls: BUCKEYE data shift, FPGA resets, ISP-PROM download, CFEB status monitor, etc.
Downloaded Constants	PREBLOCKEND (4 bits) Block Phase Shift PROM programming data (about 500K bits); BUCKEYE working mode (normal, internal capacitor select, external, kill, 3bits/channel); Comparator timing (3 bits), working mode (2 bits) and threshold
Power	+6V: for BUCKEYE clean power (550-600mA) +5V: for SCA, ADC, comparator, etc. (900-1000mA) +3.3V: for FPGA, Channel link, CPLD, etc.(450-500mA) +5V and +3.3V power supplies are subject to change.

LHC CSC Trigger Rates

- ME1/1 most important chamber for P_T Resolution
- Also the Highest Background rates for n's and γ's

L1 Accept: 100 kHz
LCT rate: 69 kHz per CFEB (worst case – ME1/1)

Estimated LCT rate for 10**34 lumi (D. Acosta et al, 2001)

Chamber Type	*LCT rate per CFEB (kHz)*
ME1/1	69
ME1/2	4
ME1/3	2
ME2/1	21
ME2/2	3
ME3/1	11
ME3/2	2
ME4/1	8
ME4/2	9

(Recent measurements of singles background consistent with these rates)

L1-LCT coincidence rate per CFEB:

100 kHz x 70 kHz x 75 ns = 0.5 kH

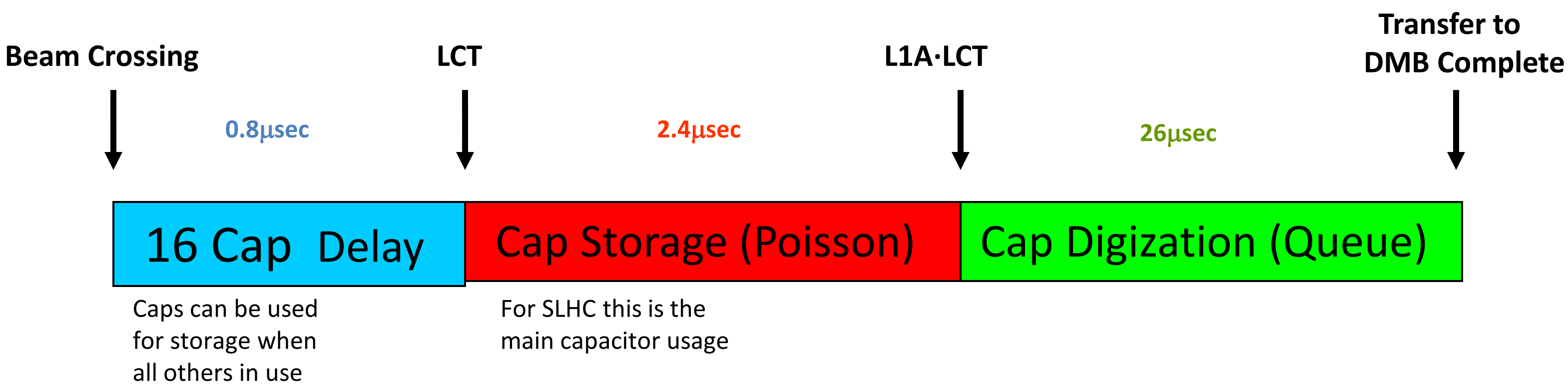
Digitization time (with 6 ADCs on each CFEB)

16 channels x 16 samples/channel x 100 ns = 26 μs

Data Bottlenecks in CSC DAQ at SLHC

- CFEB's 96 Capacitors/channel is main DAQ rate limiter
- Capacitor Storage Arranged in 12 blocks of 8 capacitors

Simple Model CFEB Capacitor Storage



ME1/1 Effective SCA Buffer Occupancy at SLHC

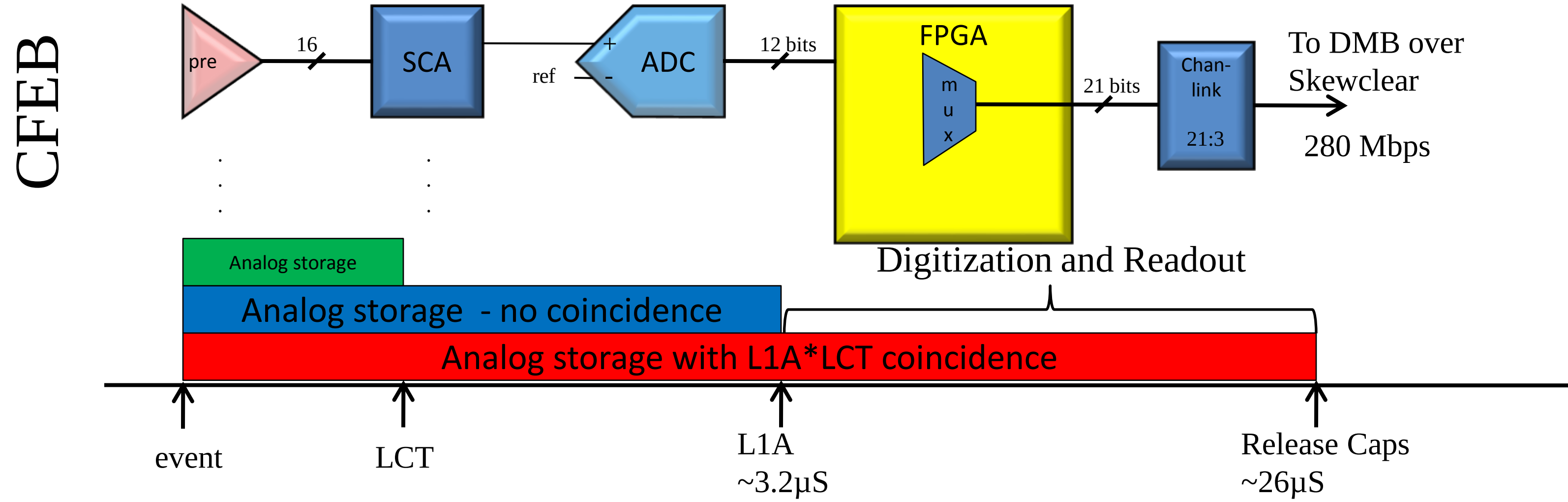
We Expect ME1/1 CFEB SCA's to Overflow

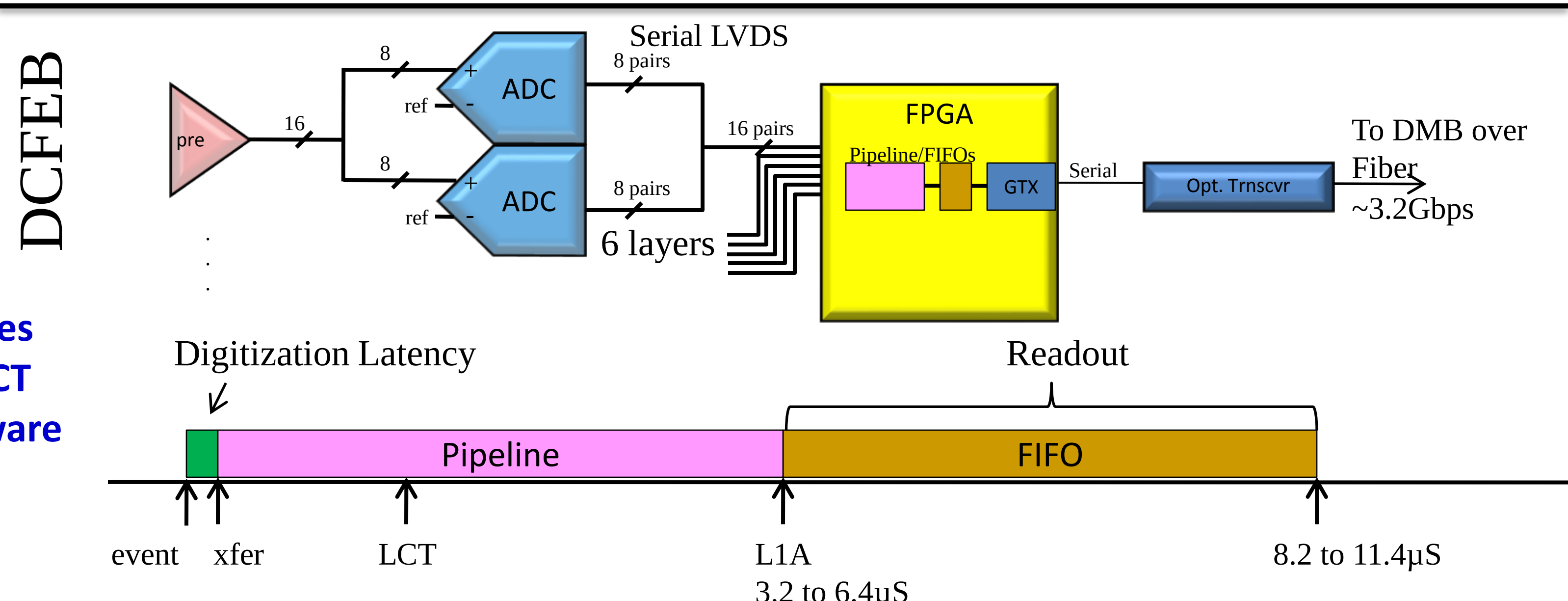
- At SLHC: use same L1 accept rate assuming rates go up linearly. Maximum LCT rate is 700 kHz (ME1/1),
  L1-LCT match rate is 5.25 kHz.
- Average number of LCTs during 5.2 μs (=6μs-0.8μs) holding time for 2-blocks: $\eta=5.2\text{x}10^{-6}\text{x}700\text{x}10^{3}=3.64$
- Average number of L1-LCT matches during 26 μs digitization time: $\rho=26\text{x}10^{-6}\text{x}5.25\text{x}10^{3}=0.1365$
- Probability of overuse of SCA: **0.09 !!!!!!!!!**

n	Free	Used	P(η,n)	Q(ρ,n)
0	12	0	0.026	0.86
1	10	2	0.095	0.12
2	8	4	0.174	1.60E-02
3	6	6	0.211	2.10E-03
4	4	8	0.192	3.00E-04
5	2	10	1.40E-01	4.10E-05
6	0	12	8.50E-02	5.60E-06

Digital CFEB – A Nice Idea for the SLHC

Replace SCA storage and Conventional ADC and with Flash ADC and Digital Storage



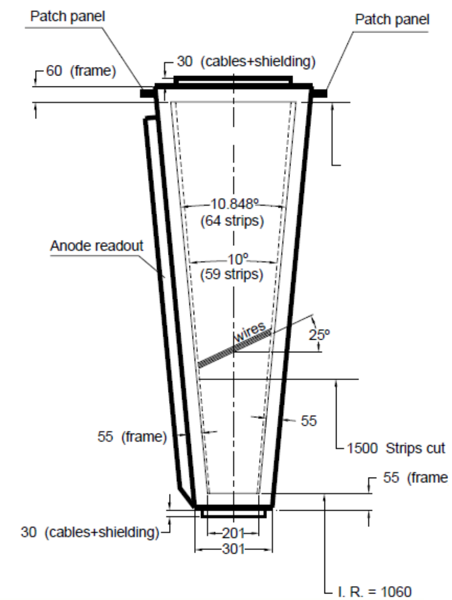


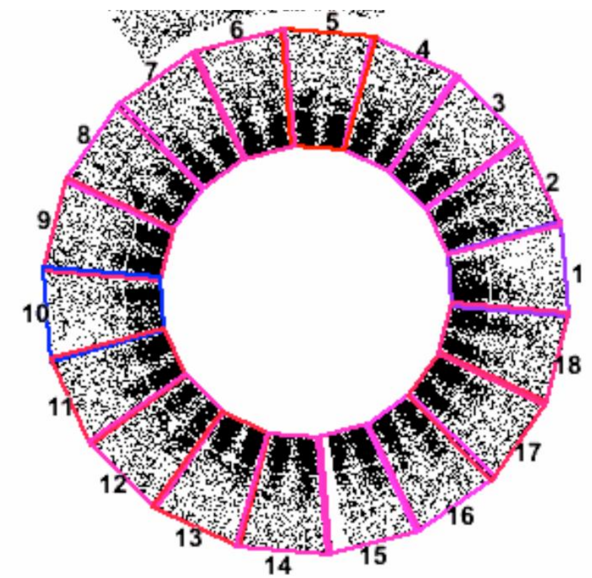
- **No Deadtime**
- **No rate worries**
- **No need for LCT**
- **Simpler Firmware**

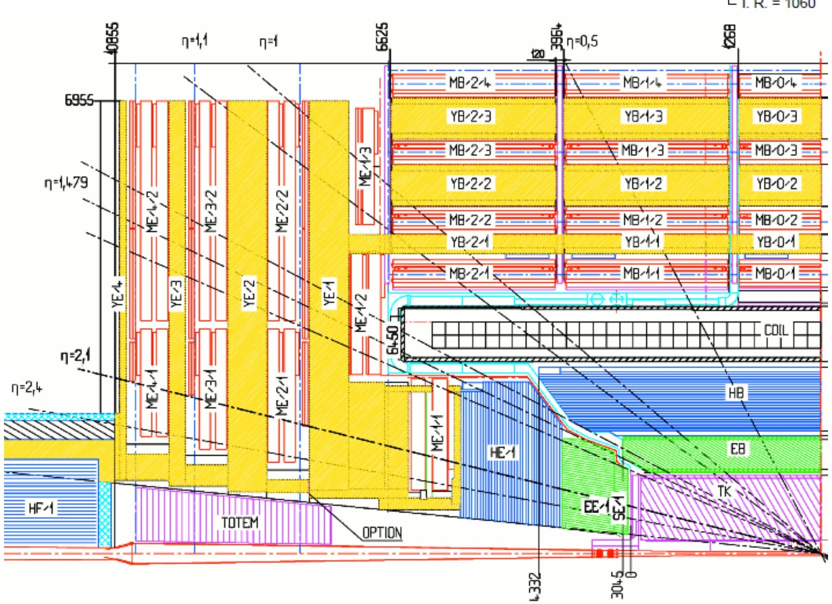
A Problem with ME1/1 Triggering

CSC Trigger disastrous for $\eta>2.1$

- for rate split strips in half
- for $$$ ganged strips (48 strips modulo 16)
- attempts to fix in firmware lead to rate problem







ME4/2 Linked to ME1/1 Upgrade

New ME4/2 chambers need boards.
Propose 514 new cards ME1/1
Old cards to populate ME4/2 Upgrade

ME1/1 Obvious for First Upgrade

- Handles highest particle flux
- Most important for momentum resolution.
- Removes ganged strips in ME1/1a

DCFEBs were designed for high Luminosity.

Improve Board-Board Communication

Present CFEB-Trigger CFEB-DMB/TMB Communications

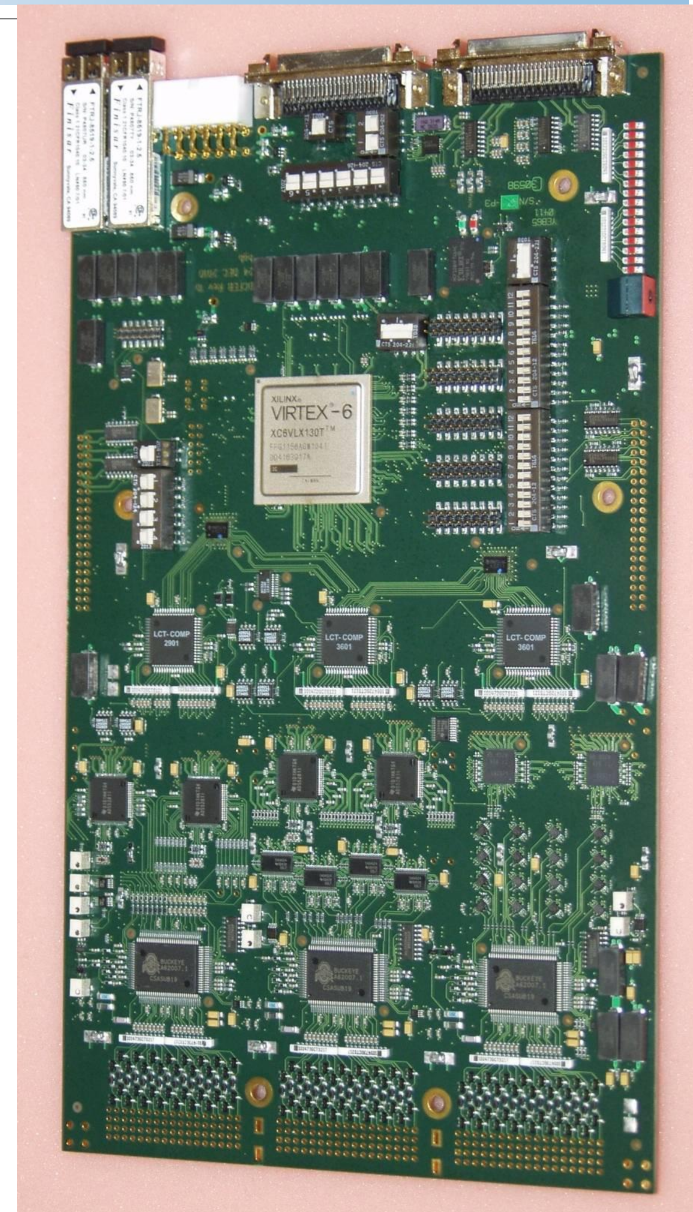
- 2 50-pin Skew-Clear Cables per CFEB
- Channel Links 280 Mb/s
- ME1/1 Cable Max Spec Length (a few problems)
- DMB/TMB boards need 7 (Skew –Clear won't fit)
- Special Manufacturing …

Preferred Option Replace Skew-Clear Cables with Optical Fiber (Snap-12)

- Room for 7 CFEBs on DMB/TMB
- More Reliable
- COTs
- Cheaper than copper

DCFEB R&D Prototype

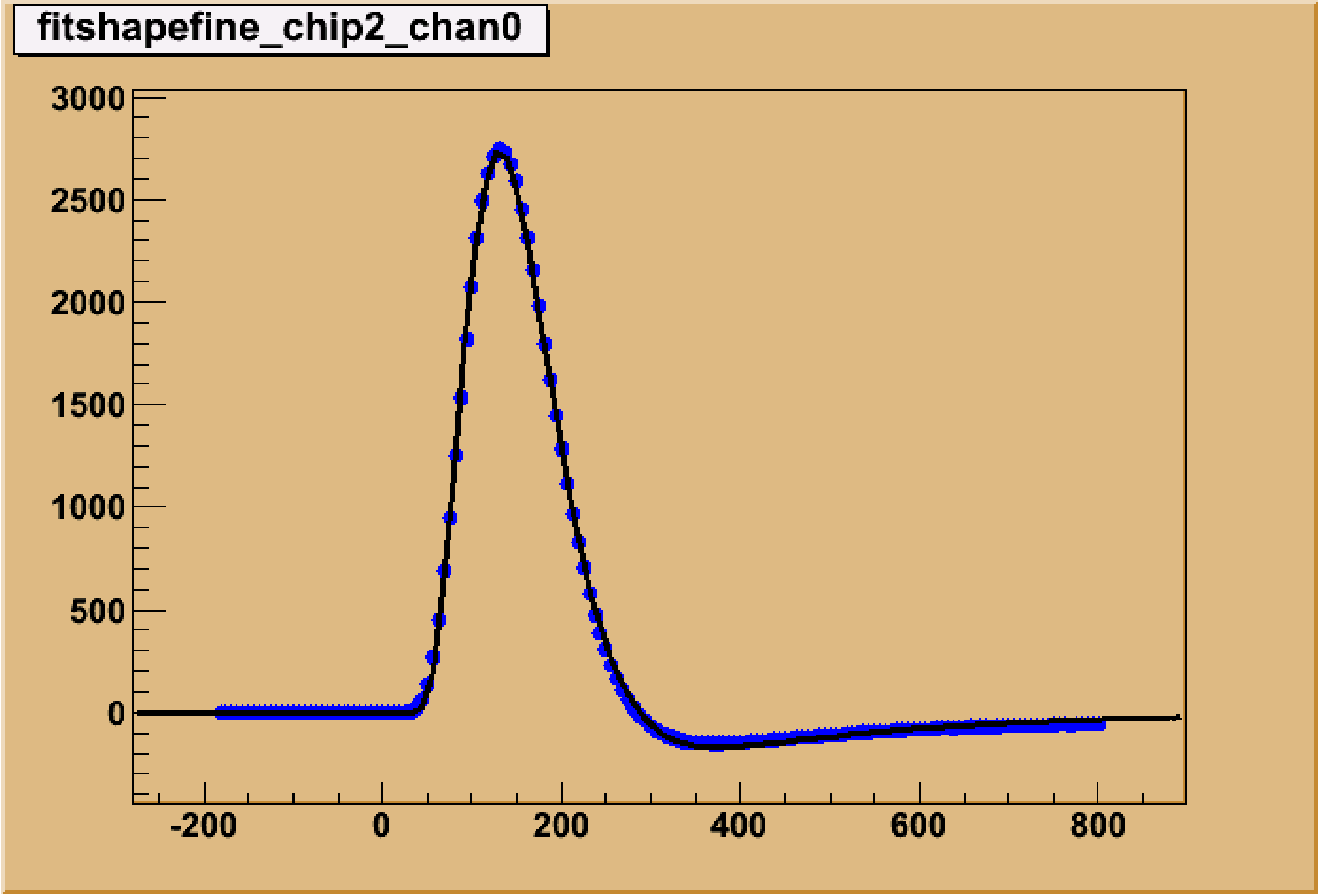
- Prototype to Test Buckeye Amplifier Connection to FLASH ADCs
  - use most of old CFEB layout , input protection, noise isolation, trigger path
  - use old CFEBs Pcrate communications
  - 4 differential amp options
  - realistic Virtex-6 digital pipeline
  - fiber optical output for tests
- Two cards received in mid-March
  - Fab: Compunetics, 20 layer board,
    special dielectric (Dk=3.5) to reduce thickness with same trace impedance
  - assembly: Dynalab
- Bench Testing
  - OSU test station, Pcrate
  - CERN building 904



We can bypass 2nd Prototype and go to Preproduction Board

Buckeye 5-pole plus 1-pole 1-zero Fits

Pulse Overlays in 6.24 nsec Intervals

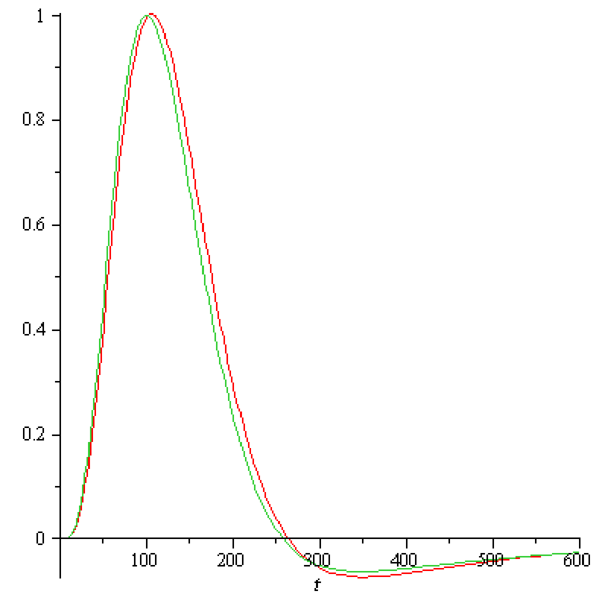


Fit Results by Coupling Type

Coupling	# Amps	Q_{peak} ADC counts	t_{start} nsec	p0 $nsec^{-1}$	p1 $nsec^{-1}$	z1 $nsec^{-1}$
Quad Diff	31	2696±21	32.0 ±0.4	0.0390 ±0.0002	0.00412 ±0.00010	0.00290 ±0.0001
Sing Diff	15	2696 ±30	32.1 ±0.4 -18.2 ±0.4	0.0387 ±0.0002	0.00422 ±0.00003	0.00289 ±0.0002
DC	15	2802 ±32	33.7 ±0.9	0.0382 ±0.0003	0.00424 ±0.00010	0.00292 ±0.0001
AC	8	2244 ±92	29.3 ±0.4	0.0168 ±0.0003	0.0148 ±0.0007	0.00210 ±0.0001

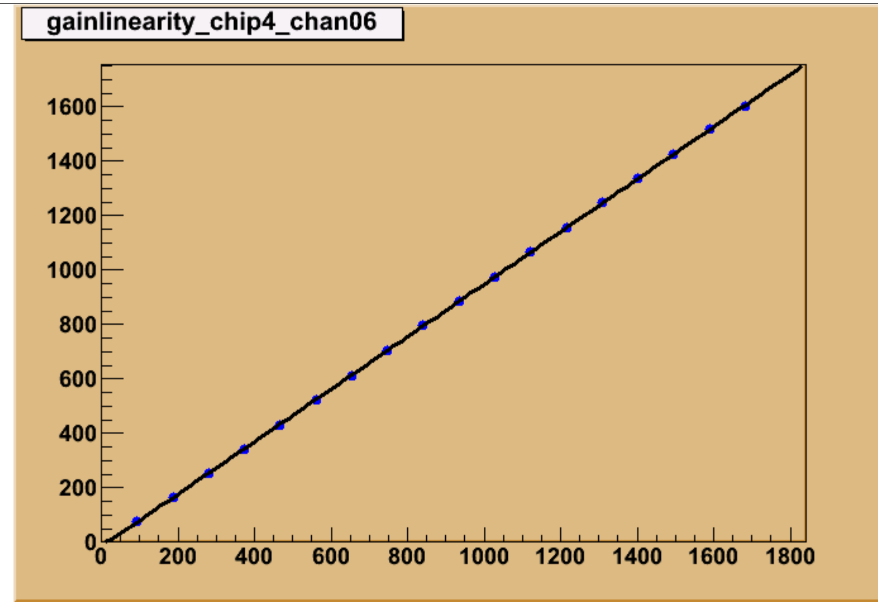
- **Quad Diff, Single Diff, and DC coupling reproduce same shape to 1%**
- **All Buckeye couplings work except AC so reject option**
- **Gain is ~0.93 mV/fC.**

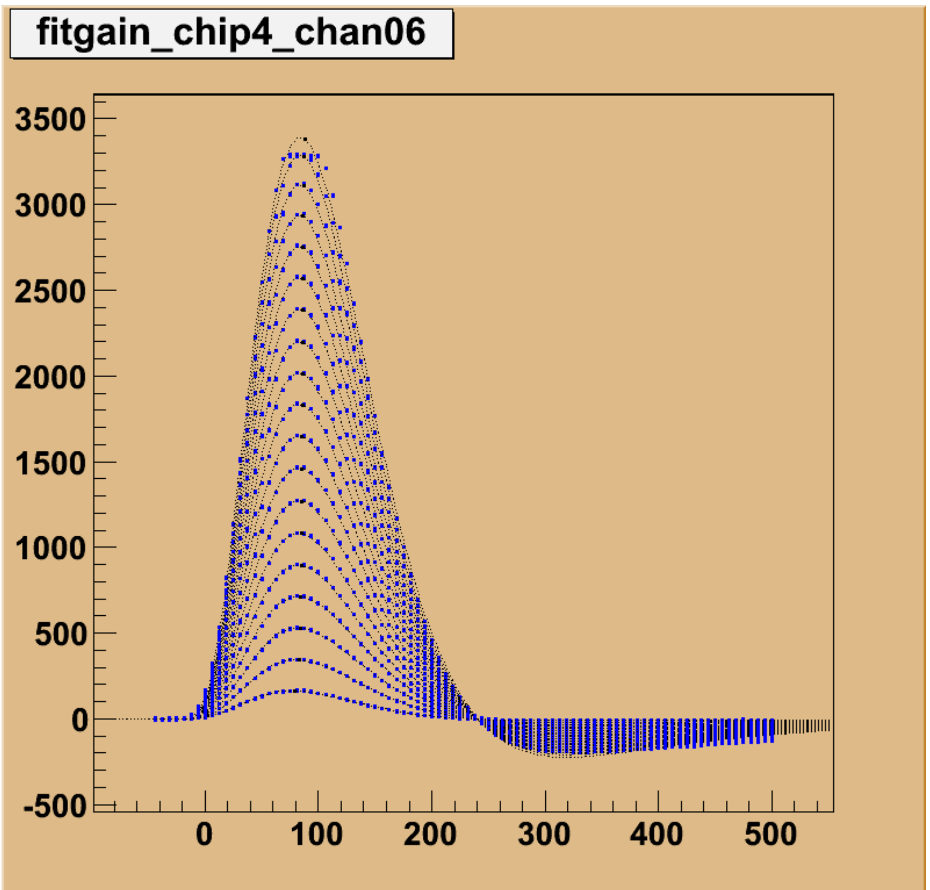
There is a small difference in pulse shape between DCFEB and CFEB pulses. The DCFEB peaks at 4/p0=103 nsec while the CFEB peaks at 110 nsec. We believe this is due to capacitance load when the CFEB measurements were take. This will be checked.

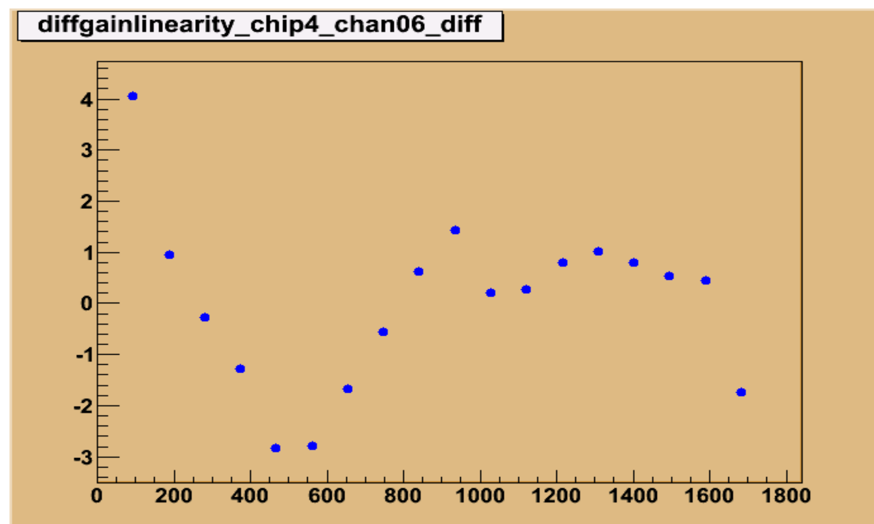


Linearity and Saturation Test

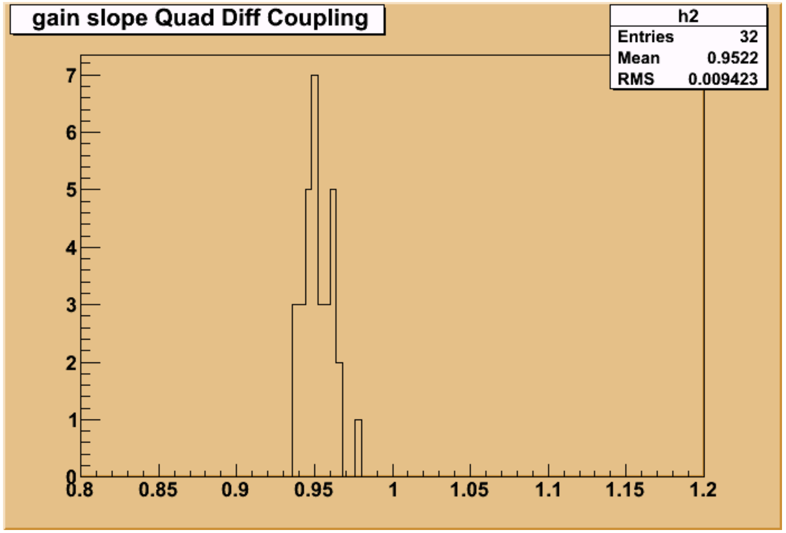
- Inject amplifier channels with 18 linear steps in voltage
- Fit Buckeye Pulses to 5 pole shaper with 1-pole 1-zero tail cancellations



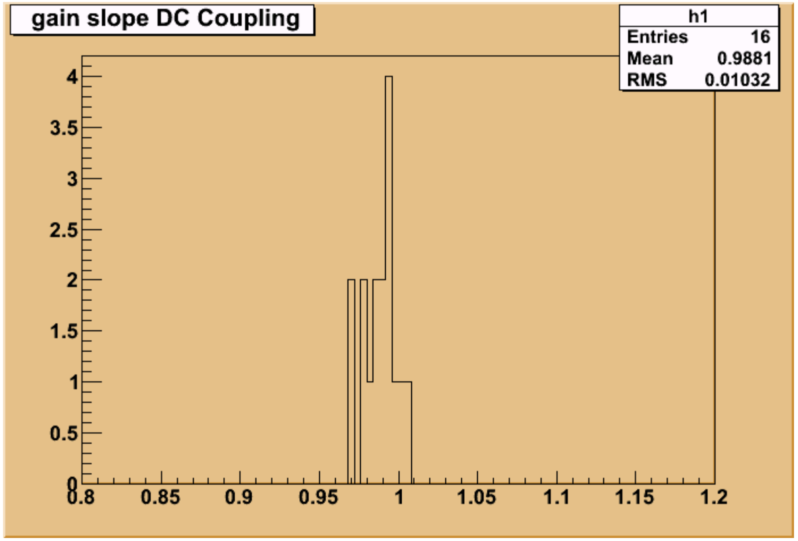


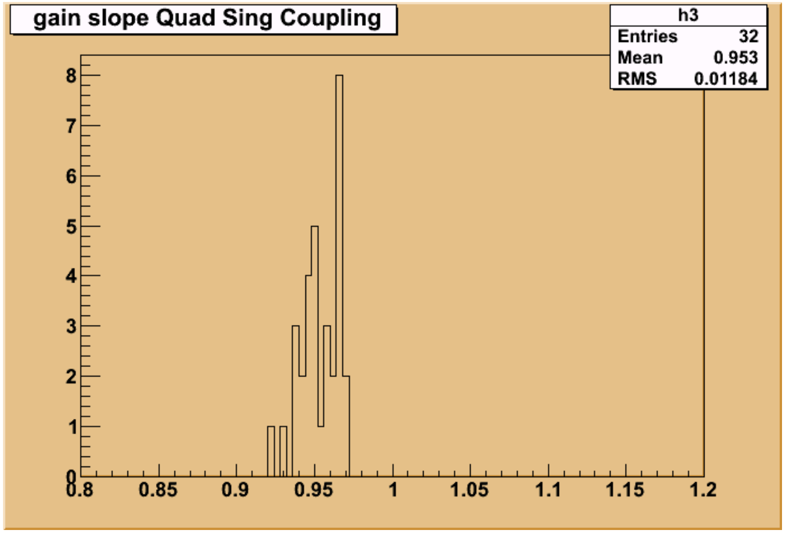


Linearity and Saturation Test (cont.)



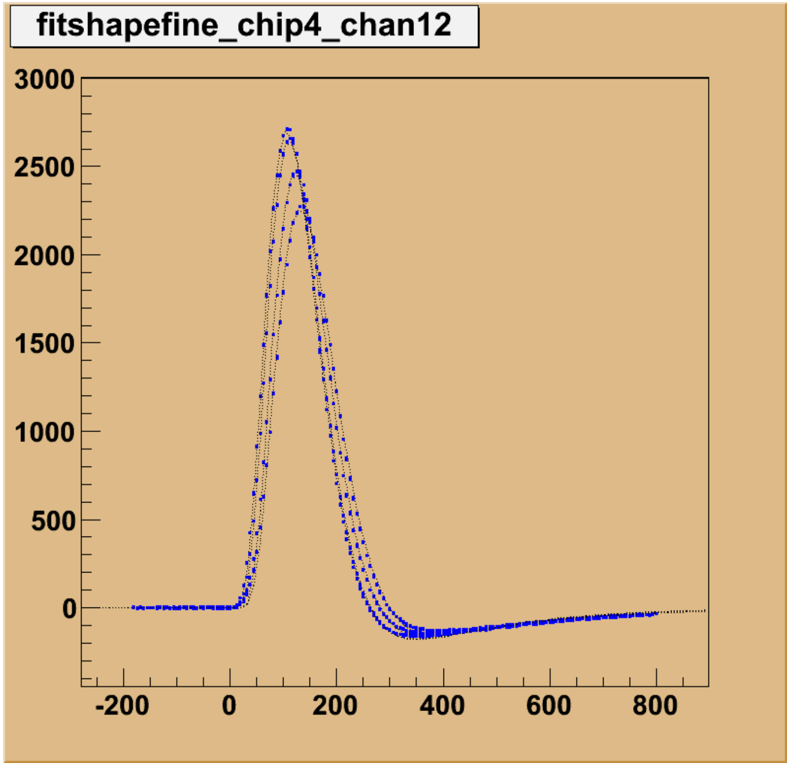
Gain is 0.95 mV/fC
(same as old buckeye board)





Slewing, Capacitance Load

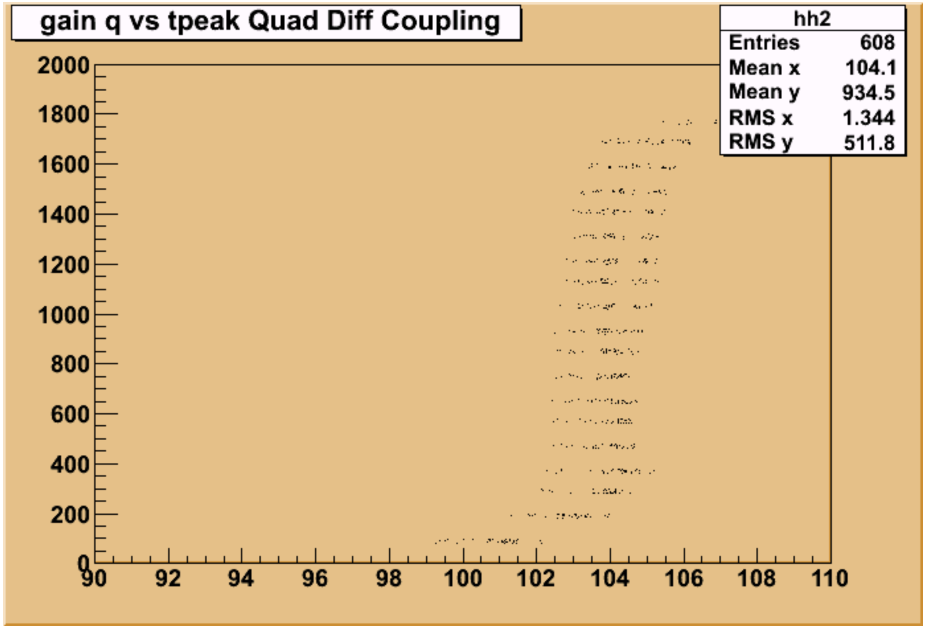
Load Buckeye Input with Capacitance



C	Q_{peak} (counts)	t_{peak} (nsec)
0 pF	2671	101
100 pF	2600	102
300 pF	2432	108
500 pF	2264	117

C	σ (ADC Counts)
0 pF	1.5
100 pF	1.7
300 pF	2.2
500 pF	2.7

Amplifier Slewing ~3 nsec



DCFEB Prototype Results from Building 904

Use 904 Spare ME2/1, Fully Configured System
17/7/11-27/7/11

(Not a Hospitable Working Environment)
Will improve with new FED Crate + VME Controller

-CFEB 5 replaced with new DCFEB Prototype

-First time DCFEB prototype on a chamber

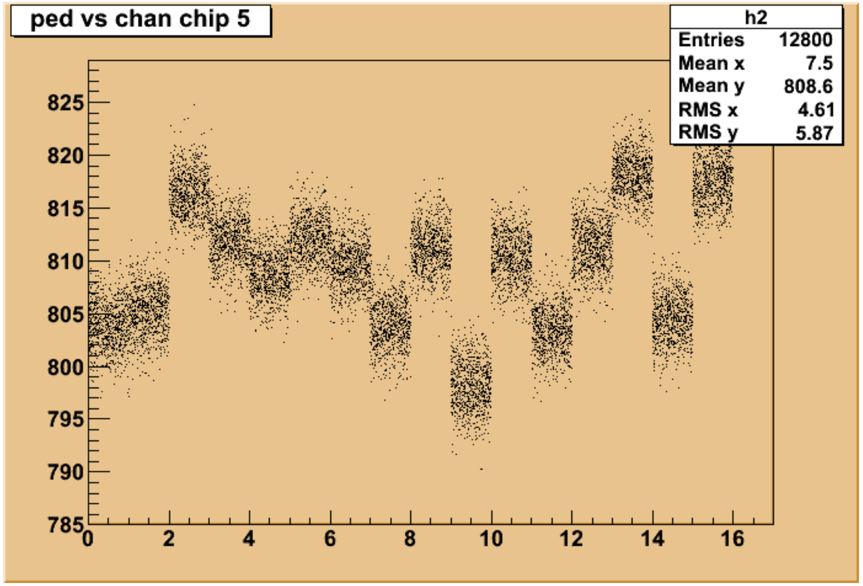
-Full DAQ readout working. DMB headers and trailers appended.
DDU headers and trailers appended

-Trigger Comparators working
Readout impossible without new FED Crate/Controller

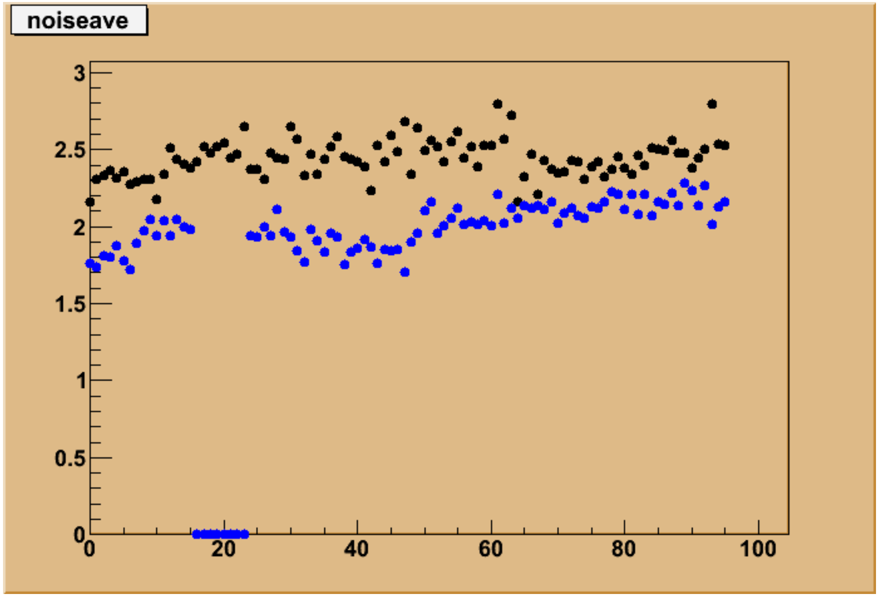
New DCFEB prototype is a plug in compatible for old CFEB

DCFEB Prototype Channel Noise

DCFEB Pedestals – Typical Chip



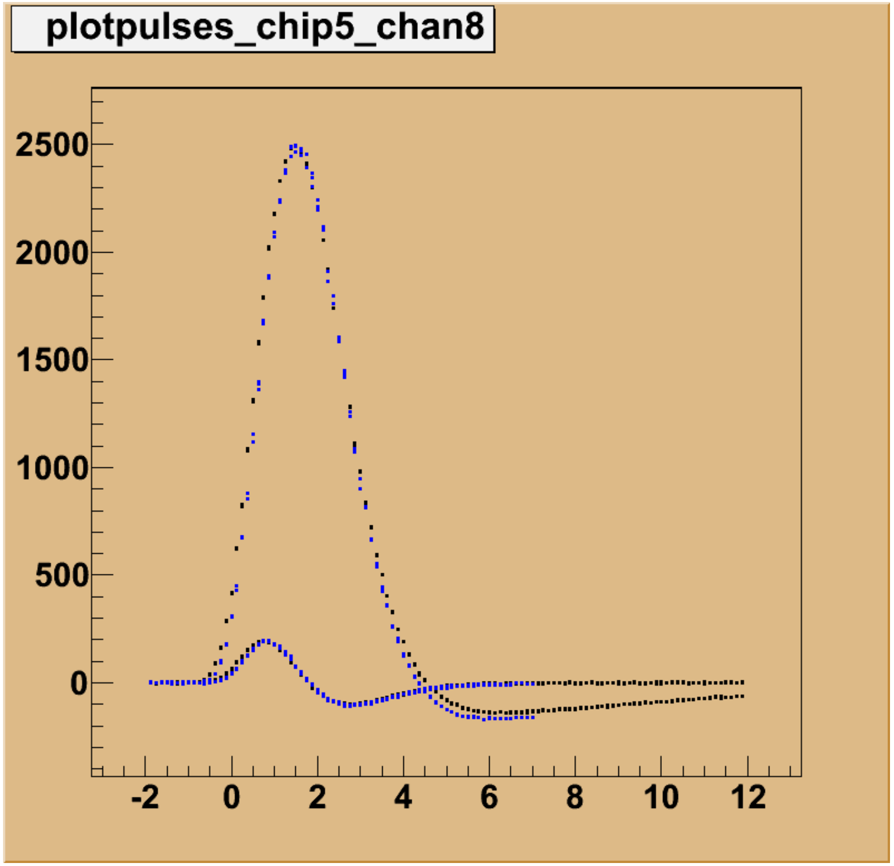
DCFEB and CFEB1 Noise σ



DCFEB Prototype Quieter than Old CFEB

No SCA so noise reduces by 1.3 ADC counts in quadrature

DCFEB Prototype Gain



Pulse Single Channels varying
Pulse timing

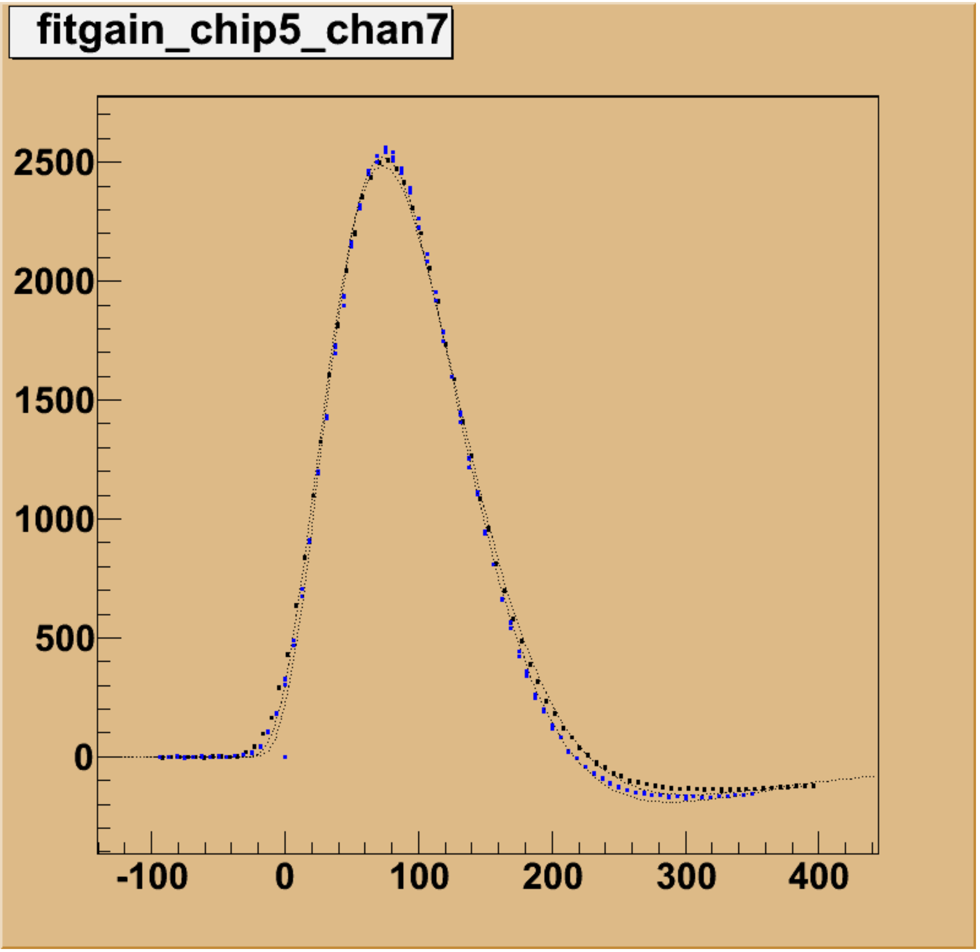
Peak Charge (ADC Counts)

Chip/Chan	DCFEB	CFEB1	CFEB2
3/7	2495	2496	2442
3/8	2503	2495	2396
4/7	2574	2436	2612
4/8	2553	2427	2582
5/7	2510	2496	2561
5/8	2496	2495	2514

-Gain Variation – ~1% within Buckey chip
-Chip-Chip variations larger
-Gain Identical to old CFEB
-Cross Talk nearly identical to old CFEB

DCFEB Prototype Pulse Shape

Fit Pulse to 5 pole with pole-zero tail cancellation
(with cross talk this is not strictly correct)



Tail cancellation shape a major systematic in fit)

Peak Time from Fit (nsec)

Chip/Chan	DCFEB	CFEB1	CFEB2
3/7	108.8	104.8	106.2
3/8	108.0	104.4	106.3
4/7	110.9	106.1	107.4
4/8	111.1	105.5	107.5
5/7	109.6	106.8	106.4
5/8	110.4	106.0	107.1
Avg	109.8	105.6	106.8

Negligible increase of peaking time seen +3-4 nsec, Another pole-zero lurks somewhere...

Optical Output Path Testing

Trigger Path:

- Uses GTX transceiver in the Virtex 6 FPGA
- Optical transfer of comparator hits to TMB
- Unambiguously transmit 48 bits every 25ns
- Fixed latency of 5 CMS clocks (transmit/receive)
- Line rate of 3.2 Gbps.
- Bench tested from DCFEB comparators through TMB mezzanine board.

Data Path:

- Uses GTX transceiver in the Virtex 6 FPGA
- Optical transfer of digitized samples to DMB
- Data sent in raw ethernet MAC frame 1 event/packet
- 2.56 GbE, line rate 3.2 Gbps
- Bench tested from DCFEB to DCFEB at 3.2Gbps then retransmitted to DMB over Skewclear

Platform Flash XL Storage

Xilinx XCF128X:

- For non-volatile storage of FPGA configuration data.
- No JTAG port, requires indirect programming.
- Intend to use unoccupied memory for parameter storage.

- Use Slave SelectMap x16 @ 40 MHz for loading FPGA
- Wrote BPI interface for programming the PROM
- Can program or read back < 4 min.

Next Step: Fiber Link Testing.

Need to test communications through the fiber link

- All TTC communications to the DCFEB will be through the 320 Mbps fiber link.
- FF-Lynx protocol
- Will be tested using the EMU-CC

Pre-Production DCFEB

Components to be removed

- Switches, headers, Skewclear connector for trigger.

Component/Design Changes

- Have chosen quad amp interface to flash ADCs
- Redesign power distribution / voltage regulators

Additional Components for the next DCFEB:

- Additional optical transceiver
- FF-EMU chip
- DAC for calibration references
- ADC for monitoring calibration refs, comp. threshold, temp, etc.
- Reference voltage connector
  (refs for preamp are now from LVDB)

Pre-Production DCFEB (cont)

PCB production issues:

- Board thickness / drill aspect ratio / reliability
- Working with manufacture to define optimal impedance control parameters to minimize board thickness

Assembly issues:

- Single amp option (QFN) had many bad connections
- Chose quad amp option as more reliable
- BGA connections should improve with thermal profile