CHAPTER 4

14/11/11

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Contents

Intro, Requirements

Pixels

Strips

On/Off detector electronics

Irradiation, testbeam

Main points

- Define technical requirements
- Present possible technologies
- Propose tests to qualify new technologies
- Present possible architectures
- Present options for the electronics readout, connections to central services, powering

- ..for pixels and strips

Requirements

Discussed in 4.1

- Start from layout used in chapter 3:
  - 7 layers
  - Radii from 22 mm to 430 mm
- Assume running scenario with 8 kHz Pb-Pb interaction rate

Table 4.1: Technical specification for the pixel and strip detectors for the ITS upgrade.

Pixels:	
Pixel size (rϕ)	20-30 μm
Pixel size (z)	20-100 μm
Track density (inner layer)	up to 85 cm^{-2}
Material budget [% X]$_0$	0.3-0.5
Signal to noise ratio (1 MIP)	>10
Power density	0.25-0.5 W/cm^2
Read-out time	< 50 μs
Strips:	
Strip width (rϕ)	50 μm
Strip length (rϕ)	20 mm
Strip thickness	300 μm
Power consumption (strips)	$\leq$ 0.5 mW/channel
Noise (strips)	$\leq$ 400 e$^-$ rms
Dynamic range (strips)	$\approx$ 10 bits

Requirements

- A very light mass detector (0.3-0.5% X_0)
  - Especially important for the innermost layers
- With excellent pointing resolution
  - Pixel sizes ~20-30 um
- Low power density
  - 0.25-0.5 W/cm^2
  - Consider longer shaping times (O(0.5-1 us))
- Readout time <50 us
- PID information (and/or from strips and pixels)
- Radiation resistant to ~2E13 n_{eq} cm^{-2} and 1.4 Mrad

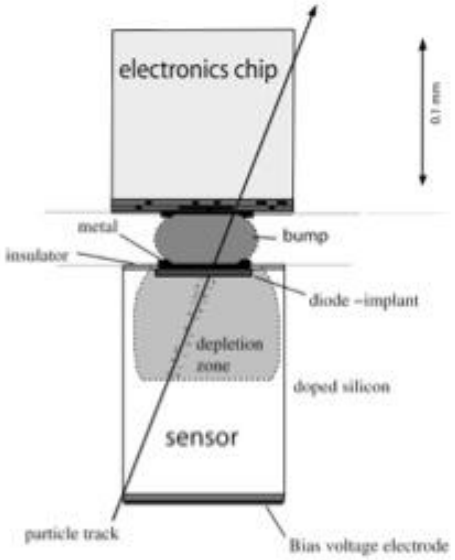
How to achieve this

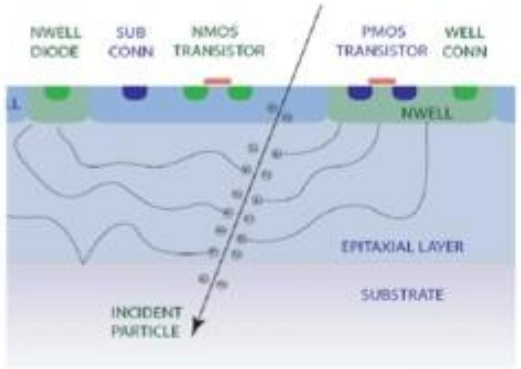
- Discuss technologies, architectures and designs which can meet the requirements

- 2 distinct parts:
  - Pixel technologies (4.2)
  - Strip technologies (4.3)

Pixels

- Start with general considerations:
  - Present concept of hybrid and monolithic detectors (4.2.1)





Pixels

- Discussion on the technical implementation (4.2.2)
  - What is state of the art (LHC pixels…)
  - What technologies are being used in ALICE like environments (STAR upgrade)
  - What new developments could be of interest (Tower/Jazz 0.18, INMAPS, LePix)

Pixels

- Finish 4.2.2 with a summary table of possible technologies for pixels in the ITS

Table 4.4: Key parameters for different pixel technologies under consideration for the ALICE ITS upgrade.

	Hybrid Pixels	Mon. Pixels (MAPS)	Mon. Pixels (LePix)
Maturity	++	+	-
Pixel size	30μm	20μm	30μm
Material budget (Si)	$\approx$0.16% X_0	$\approx$0.05% X_0	$\approx$0.05% X_0
SNR	>50	$\approx$20	>50
L1 trigger	+	-	+
Timestamp	+	-	+
Cost/cm^2	-	++	+
Radiation hardness	$>10^{14}n_{eq}$	$\approx10^{13}n_{eq}$	$>10^{13}n_{eq}$

Pixels technologies for the ITS

- Distinguish between hybrid and monolithic pixels
- Presented in two different sections

4.2.2.1 Hybrid Pixels

- State of the art, used in all LHC experiments
- Challenge: build a low mass hybrid pixel detector
  - Comparison table with other LHC experiments of sensor and ASIC

Table 4.5: Summary of thicknesses used in current LHC hybrid pixel detectors and target values for a hybrid pixel detector for the ALICE ITS upgrade.

	ASIC thickness [μm]	Silicon sensor thickness [μm]
ALICE pixel	150	200
ALICE ITS upgrade	50	100
ATLAS pixel	180	250
CMS pixel	180	285

4.2.2.1 Hybrid Pixels

- Sub-sections:
  - Sensor options
  - FE chip architecture
  - TSV
  - Bump bonding and thinning

4.2.2.1 Hybrid Pixels

- Sensors
  - Discuss the options to produe 100 um thin sensors
    - Epi wafers
    - Standard wafers with supports
  - Expected radiation induced
  - Edgeless layout option
- Prototypes
  - Epi wafers
  - Testbeam 2010 results
  - Outlook for 2011/12
    - VTT thin sensor run
    - FBK edgeless epi sensor run

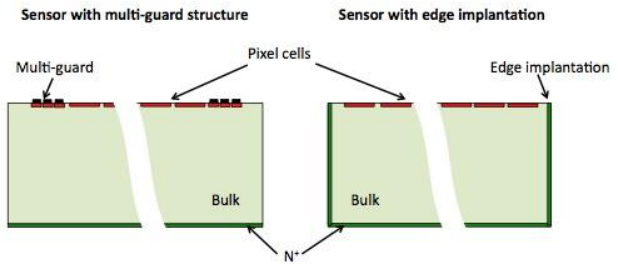


Figure 4.2: Schematic view of a sensor with multi-guard structure and of an edgeless sensor using an n^+ edge implantation.

4.2.2.1 Hybrid Pixels

- FE chip architecture
  - Discuss the general architecture of a standard hybrid pixel detector with BC tagging capability
  - Option to use also rolling shutter architecture for hybrids
  - How can the power consumption be reduced to minimize the material budget
    - Which parts of a circuit consume how much power
    - Which S/N (taking into account lower sensor thickness)
    - Present a simplified schematic of an architecture
  - Development strategy

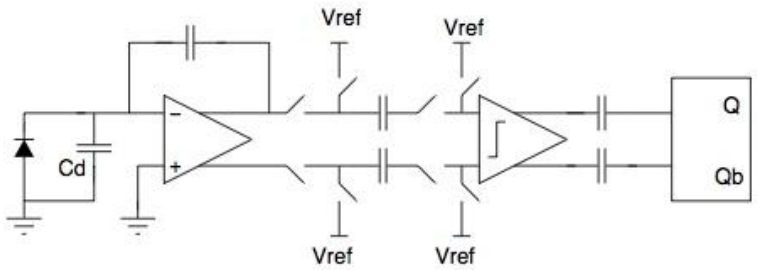


Figure 4.6: Simplified schematic of a pixel cell with dynamic comparator

4.2.2.1 Hybrid Pixels

- TSV
  - Introduce concept
  - Common effort with Medipix to develop TSV process

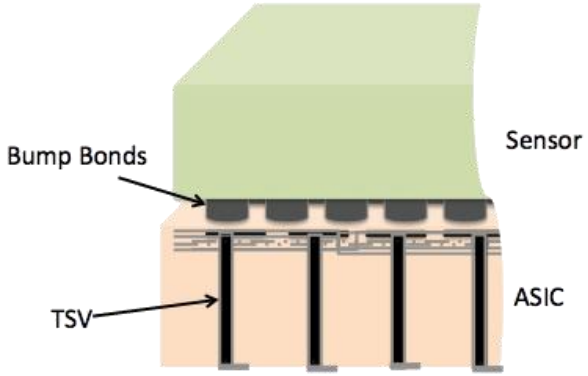


Figure 4.7: Schematic view of a hybrid silicon pixel detector with TSVs.

- Bump bonding and thinning
  - General problems
  - Present tests carried out with iZM

4.2.2.2 Monolithic Pixels

- Divided into 3 sub-sections
  - Sensors with rolling shutter readout
    - MISTRAL
  - Sensors with in-pixel hit discrimination
    - INMAPS
  - Drift based sensors in very deep sub micron CMOS
    - LePix

4.2.2.1 Monolithic Pixels

- Sensors with rolling shutter readout
  - Present concept (reference to MIMOSA)

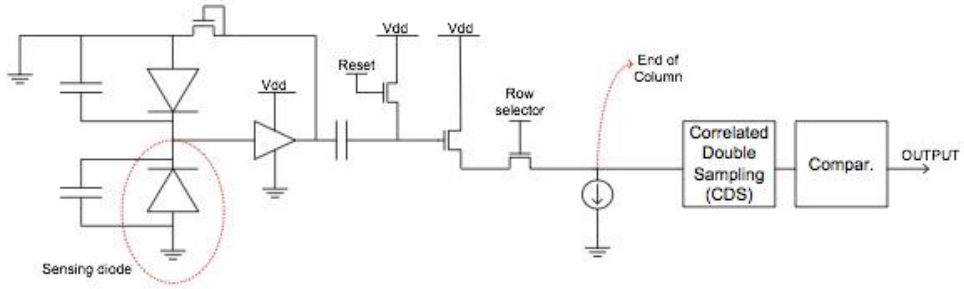


Figure 4.9: Simplified schematic of a pixel cell.

  - Prototype development for ALICE
    - MISTRAL
    - Which technology to chose (0.18 um Tower/Jazz)
    - What are the prototype plans (submissions of test structures and chips, etc.)

4.2.2.2 Monolithic Pixels

- Sensors with in-pixel hit discrimination
  - Present option to use deep p-well for the design
  - INMAPS or quadrupole well technology
  - Discuss possible architecture to achieve low power circuit
  - Prototype developments in 0.18 um CMOS by Tower/Jazz, i.e. test structures for evaluation of radiation hardness

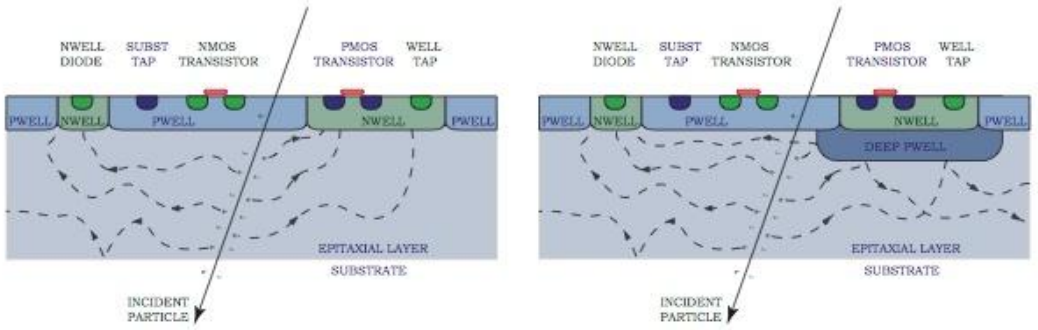


Figure 4.10: Standard monolithic approach (left) and quadruple well technology (right).

4.2.2.2 Monolithic Pixels

- Drift based sensors in very deep submicron CMOS
  - Present sensor principle of LePix
  - Discuss architecture, keeping in mind to minimize power
  - Prototype developments - plans, first results from radiation tests

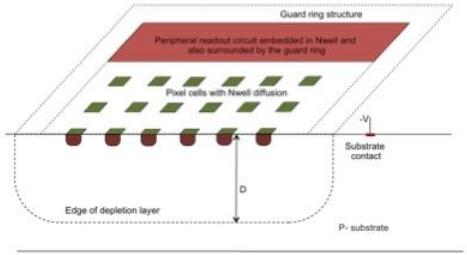


Figure 4.12: Schematic overview of the detector structure for drift based monolithic pixel detectors.

4.2.3 Pixel Module and Interconnection

- What are the sizes needed (ref. to chapter 5)
- What are the reticle sizes in CMOS production (mention stitching here)
- Hybrids: single chip assemblies vs. multi-chip assemblies
- How to make the connection to the outside world
  - BGA connections to flex

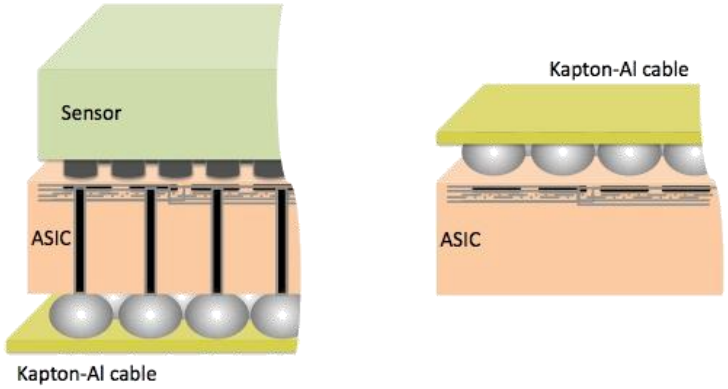


Figure 4.14: Schematic view of a possible pixel detector module, shown for a hybrid pixel detector on the left and a monolithic pixel detector on the right.

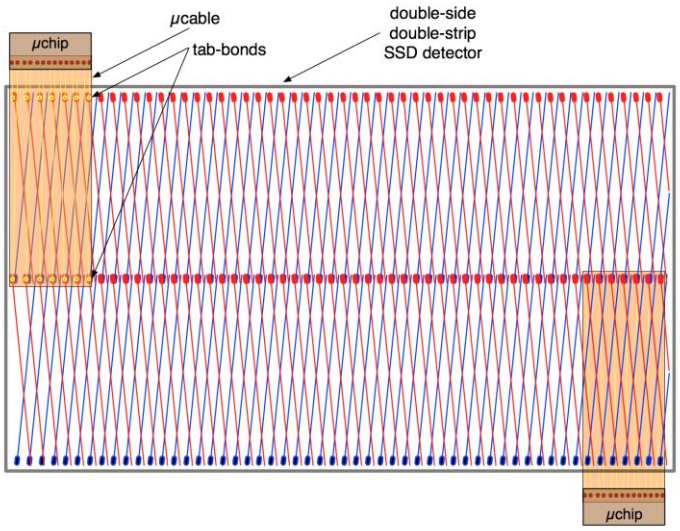
4. Technology Options for Strip Detectors

Introduction

1. Sensor Design
    1. Layout Options
    2. Performance in simulations
2. Front-End Electronics Development
    1. Requirements
    2. ASIC architecture
    3. Development program
3. Aluminum-polyimide μcables for Interconnections
    1. Cable Layout
    2. Assembly test plans
    3. Hybrid circuit layout
4. Module design and Assembly

4. Technology Options for Strip Detectors

- Introduction:
  - Well known technology
  - New requirements
    - Experimental conditions
    - Layer position
    - Low momentum PID



4.3 Technology Options for Strip Detectors

The present ITS strip detector design is optimized for the present LHC conditions and ALICE physics goals. Although the available strip detector technologies are rather mature, the construction of a new strip detector will benefit from past experience, leading to better reliability and uniformity of several components and thus to a significantly improved overall performance in real operating conditions. In addition, appropriate modifications made on each component design will allow to meet the requirements suggested by the new physics aims, the expected experimental conditions and the position of the detector in the new tracker. At smaller radii with respect to the present position, the strip detector will probably face an occupancy problem that requires to redefine its geometric characteristics. Moreover, since the low-momentum particle identification performed by the silicon tracker appears to be a relevant physics item and requires a wide input dynamic range, the development of the strip detector will take into account this need.

Screenshot

4.3.1 Sensor Design

The upgraded strip detector will be based on 300 μm thick, double-sided micro-strip sensors with a small stereo angle between the strips on opposite sides, in order to keep an acceptable rate of ambiguities in track reconstruction. Given the prospect of a smaller distance between the strip layers and the interaction vertex and taking into account the increased particle multiplicity foreseen at the nominal LHC energy, we considered a redesign of the current SSD sensor that allows to decrease the cell size in order to keep the occupancy low.

The simplest way to do this is to halve the strip length while keeping the same sensor

- Sensor Design
  - Half-length strips
    - Smaller cell size
      - Better ghost hit rejection
      - Lower capacitive noise
    - Higher power consumption

Sensor Design

@Trieste

- Options for the layout
  - half-length strips
  - two options for the track inclination:
    - 35/40 mrad stereoangle
      - Geometric precision
      - Dead area position
- Improvements on point reconstruction and resolution of ambiguities are estimated in simulation:
  - Ghost hit rejection power

4.3.1.1 Layout options

In the process of defining the new sensor layout, different options for the strip stereo angles have been considered in order to obtain the best trade-off among ghost hit rejection capability, spatial resolution and sensor dead area (which defines the required overlap between adjacent layers).

Two configurations are being studied for what concerns the arrangement of the half-length strips. The first case reproduces the present configuration of the SSD sensor, where the strips are tilted with respect to the small axis of the sensor by 7.5 mrad on P-side and 27.5 mrad on N-side, for a total stereo angle of 35 mrad; this choice of angles results in 4 and 11 strips of shorter, decreasing length at the ends of the detector, respectively. The position of the aluminum bonding pads on the sensor surface has been optimized in order to have a symmetric layout on the two sectors (upper and lower) of each sensor side (p and n).In the second case the angles are 10 mrad on P-side and 30 mrad on N-side, for a total stereo angle of 40 mrad, defining 4 and 12 shorter strips. The geometric precision in the two directions and the dead area size are being studied for both options.

Screenshot

4.3.1.2 Performance in simulations

The new half-length configuration considered for the strip sensor (keeping the present 35 mrad stereo angle) has been implemented in a dedicated simulation, in order to evaluate its performance; it takes into account the signal-to-noise ratio measured by the present SSD. In this paragraph we show the results in terms of reconstruction efficiency and purity, when many particles cross the detector at normal incidence. Figure 4.15 (left panel) shows, versus track density, the fraction of non-ambiguous points (with respect to the number of tracks) reconstructed with geometric considerations only (i.e. without applying the charge matching). This fraction is larger than 78% even with a multiplicity of 2 particles/cm^2. Figure 4.15 (right panel) shows the fraction of ambiguous points (with respect to the total number of reconstructed impact points) as a function of the multiplicity; the fraction of ambiguous points, around 16% even with a multiplicity of 2 particles/cm^2, can be significantly reduced by applying the charge matching between p and n side. These results suggest the feasibility of using microstrip detectors to build the

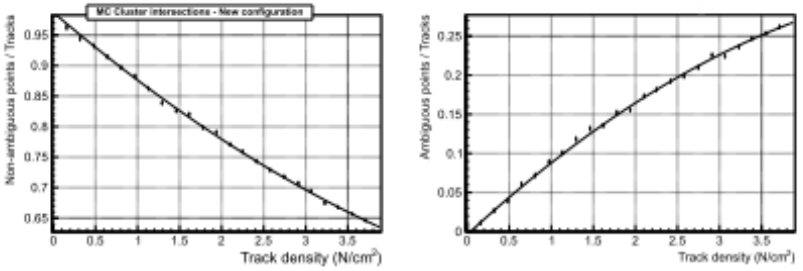
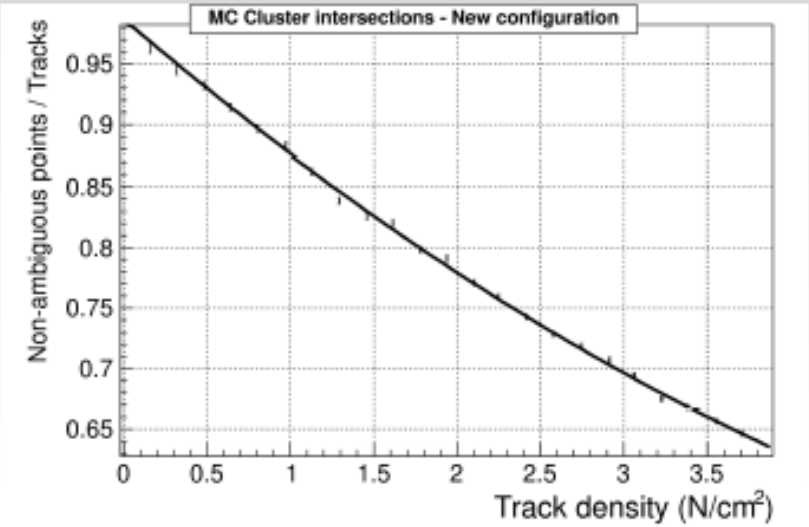


Figure 4.15: Point reconstruction efficiency and purity with the new strip sensor layout in simulation: fraction of non-ambiguous points with respect to the number of hits (left) and of

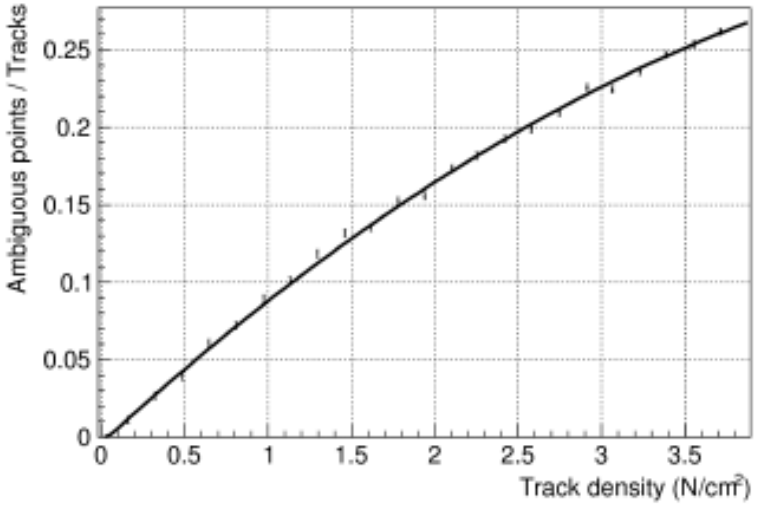
Efficiency/purity

Miljenko Šuljić, Stefano, Giacomo



Fraction of non-ambiguous points
- w.r.t. the generated tracks
- reconstructed with only geometric considerations
- no charge-matching

Fraction of ambiguous points
- w.r.t. all the crossing combinations
- reconstructed with only geometric considerations
- no charge-matching

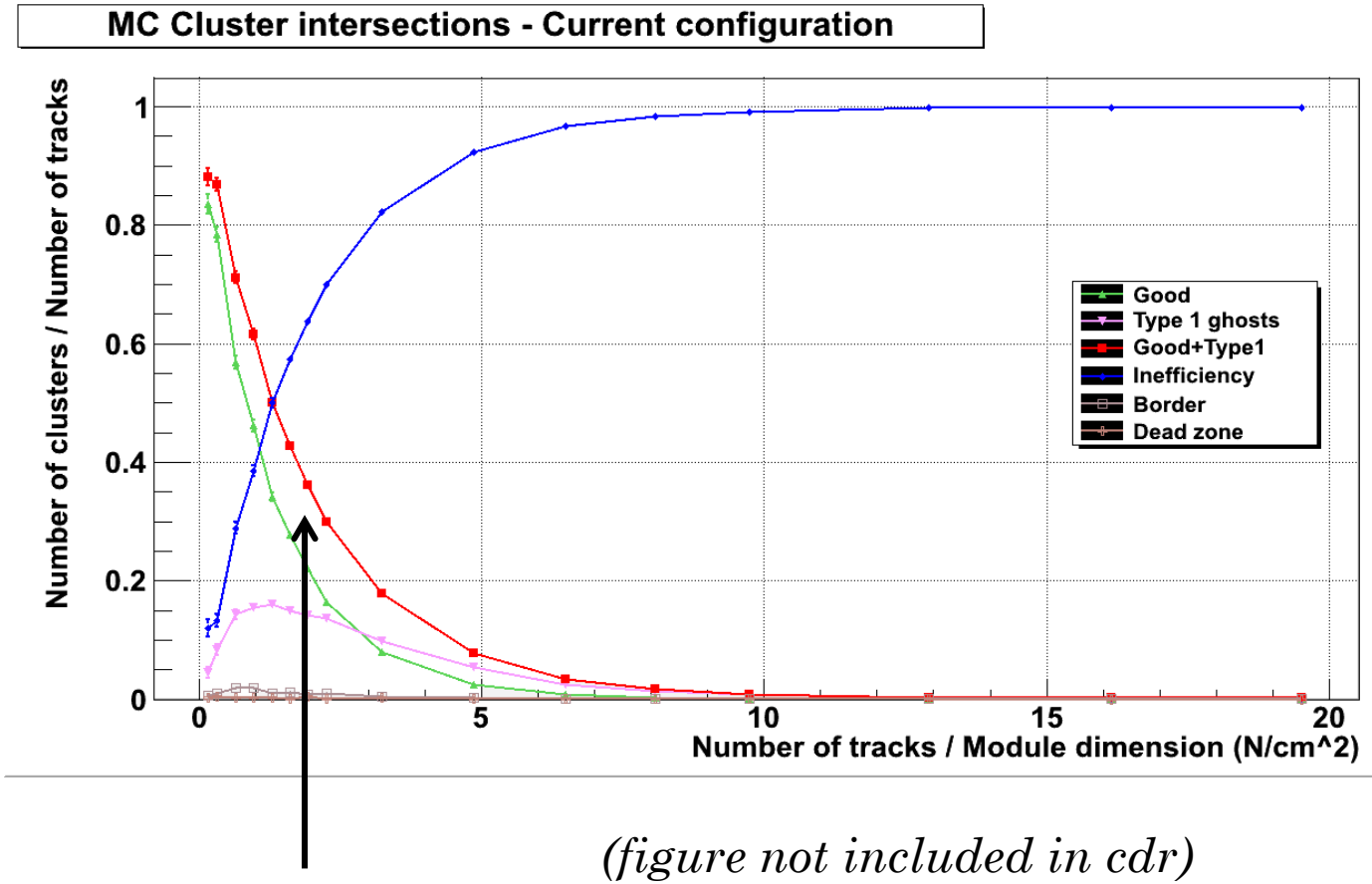


GOOD AND GHOST POINTS - PRESENT CONFIGURATION

Simulation:

- present SSD layout
- 500 MeV/c pions
- normal to the sensor
- realistic signal-to-noise ratio
- 2D points with only geometric considerations

Miljenko Šuljić, Stefano, Giacomo



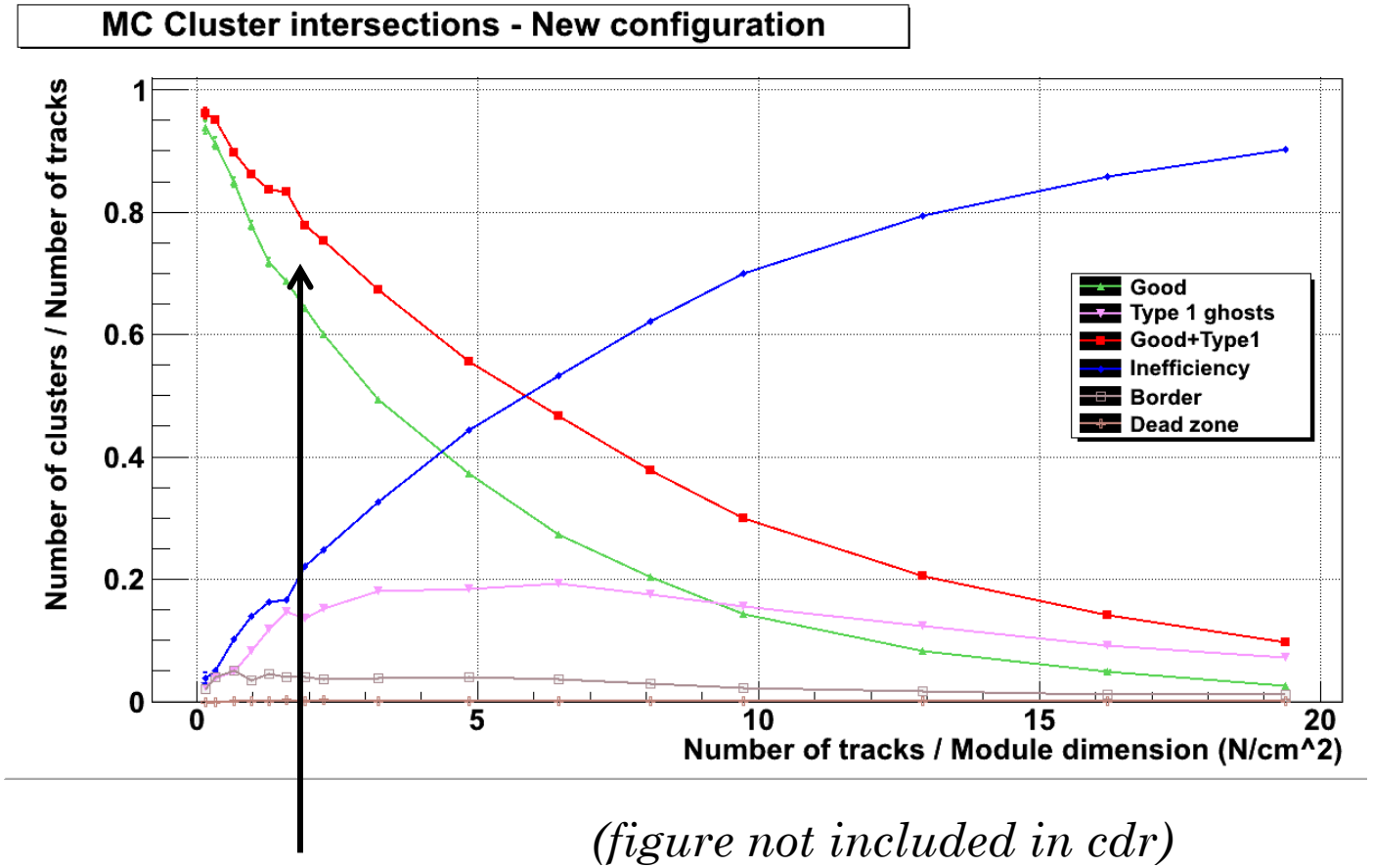
(figure not included in cdr)

GOOD AND GHOST POINTS - NEW CONFIGURATION

Simulation:

- **half-length strip layout**
- 500 MeV/c pions
- normal to the sensor
- realistic signal-to-noise ratio
- 2D points with only geometric considerations

Miljenko Šuljić, Stefano, Giacomo



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Strip Front-End Electronics Development

4.3.2 Front-End Electronics Development

A new front-end chip for Silicon Strip Sensors will incorporate on board the analog to digital conversion, today performed outside the front-end ASIC. The ASIC will deliver to the back-end electronics digitized data serialized on a few high speed differential links. To accommodate more channel on chip, one could explore the use of commercial flip chip technologies as an alternative to standard wire bonding. The front-end chip will be designed in the same process (0.13 μm or 0.18 μm) chosen for the pixel sensors. This will minimize the use of different technologies in the project and will favor expertise exchange and building block re-use among the different subsystems.

4.3.2.1 Requirements

The requirements for the front-end ASIC for the strips are reported in table 4.7

The key difference between a new chip and the HAL25 will be the data digitization directly on chip. The requirements on total dose are easily accommodated by modern CMOS technologies without enclosed layout transistors. Single Event Upset tolerant design will be adopted in the control path.

4.3.2.2 ASIC architecture

The front-end ASIC will interface to the outside world with fully differential digital I/O (LVDS or SLVS). Several approaches can be used for the on chip digitization of the analogue information. The spectacular progress recently made in the domain of analog to

Screenshot

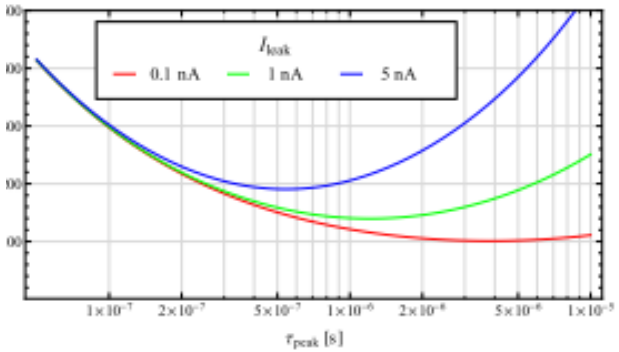


Figure 4.16: Noise versus peaking time for strip sensors for 5 pF of sensor capacitance.

transconductance of 1 mS (achievable with a current smaller than 100 μA) and a sensor capacitance of 5 pF were assumed in the calculations. Since for the strips the power and the space for the front-end electronic are not as constrained as for the pixels, a more elaborate shaper (CR-RC^4) was considered, which offer better noise performance for the same pulse width with respect to the simple CR-RC. With this configuration, a noise below 300 electrons for a peaking time above 1.2 μs is achieved up to a leakage current of 5 nA per strip.

As for the pixel, the ASIC will incorporate on board the service and slow control components (voltage regulation, temperature monitoring, etc.).

Front-End Electronics Development

- Requirements
- ASIC architecture
- Development program

Strip Front-End Electronics Development

Requirements: Table 4.7

Table 4.7: FE requirements

ASIC spec	HAL25 (present SSD)	Upgrade chip
Input pitch	80 μm	44 μm
ASIC size	(3.65 x 11.90) mm	(6 x 6) mm
Noise (5 pF load)	400 e^-	400 e^-
Peaking time	1.4 - 2.2 μs	1 - 2 μs
Power per channel	500 μW	500 μW
Total number of channel	128	128
Digitization	Off chip	On chip
Radiation level	30 krad	30 krad
Technology	CMOS 0.25 μm	CMOS 0.13 - 0.18 μm

ASIC architecture

- On-chip ADC
  - 10 bits
  - low power
  - also ToT considered (large integration time)
- 1 µs peaking time
  - Adjustable to accommodate trigger latency
- Sampling/digitization in 100 ns
- Transmission of non-ZeroSuppressed data in 10 µs
- Technology node → 0.13 – 0.18 µm
- Chip geometry → 6mm x 6mm
- CM correction & Zero-Suppression
  - Off-detector FPGA → + bandwidth, programmable
  - On-chip

Development program:

- To be started after upgrade decision
- 2 years expected time

ALUMINUM-POLYIMIDE MICRO-CABLES

4.3.3 Aluminum-polyimide μcables for Interconnections

The present SSD module uses low-mass Kapton-based cables with aluminum conductors for the electrical connections between the sensor and the front-end chip. This technology is still considered the most suitable for this kind of detector layout, thanks to its greater flexibility with respect to the standard wire bonding technique: it allows positioning both hybrid circuits (reading p and n-sides) on the same side of the sensor, by folding around the sensor edge the microcables connected to the strips of one side. Moreover, in combination with the TAB bonding on the sensor side, the use of commercial flip-chip technologies to connect the μcables to the front-end chips is being considered in order to preserve the module layout despite the increased channel density in the electronics. Flexibility, reliability and thermal and electrical insulation of the considered interconnection techniques are being evaluated and compared.

4.3.3.1 Cable Layout

Screenshot

In the present SSD, cables made of 10 μm polyimide foil with 14 μm thick aluminium traces are used to connect the front-end chip to the sensor on the input side and to the hybrid circuit on the output side. The length of the input traces connecting the chip to the detector is 11 mm, with a fan-out to adapt the input layout (128 input pads in one row with 80 μm pitch) to the sensor pitch (95 μm). The trace width is 35 μm. The recent technology development offers now the possibility to realize cables with a smaller inter-trace pitch, down to 44 μm, and to connect and read-out a doubled number of strips arranged on two separated rows, preserving the low material budget and a compact detector layout. Prototypes of (10+14) μm thick kapton-aluminum cables, with minimum inter-trace pitch of 44 μm and trace width of about 25 μm are being developed: the geometrical characteristics for the sample designed to connect the p- and n-side of the sensor, with the corresponding two different dimensions, are listed in table 4.8. The traces are arranged in order to match two rows of bonding pads with a pitch of 95 μm on the sensor side (contacting two groups of 64 half-length strips), and the two staggered rows of pads on the front-end chip, each with a pitch of 88 μm.

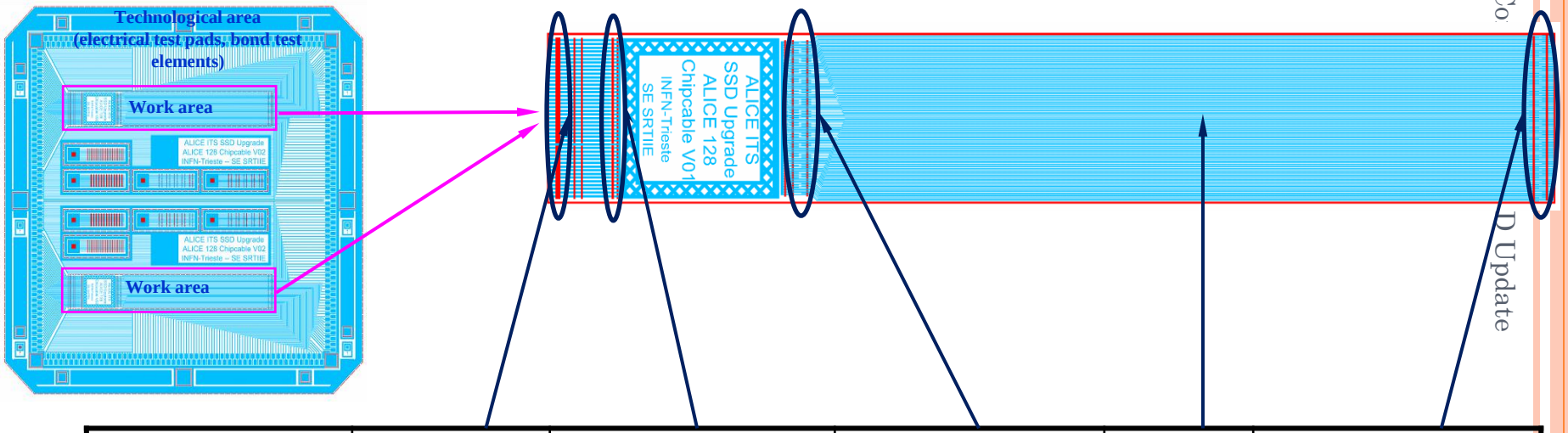
Table 4.8: Microcable dimensions and arrangement

Cable area	to-hybrid	to-chip (*output pads*)	to-chip (*input pads*)	transmitting area	to-sensor
Trace pitch [μm]	136	136	44	47.5	47.5
Trace width [μm]	$\sim$ 80	$\sim$ 50	$\sim$ 30	$\sim$ 22	$\sim$ 30
Trace quantity	43	43	128	128	128
Pads placement	one row	one row	two rows (staggered)	- -	two rows (staggered)

MICROCABLE SPECIFICATIONS

SE SRTIIE - Karkhov

- Technology features:
  - Flexibility
  - Low material budget
- Chipcable developed for assembling to ALICE 128 dummy chips
  - Material: an aluminum-polyimide adhesive-less foiled dielectric FDI-A20
  - Thickness: Al 10um, Polyimide 10um



	Cable-to-hybrid bonding area	Cable-to-Chip bonding area (output pads)	Cable-to-Chip bonding area (input pads)	Transmitting area	Cable-to-sensor bonding area
Trace pitch, um	136	136	44	47.5	47.5
Trace width, um	~ 80	~ 50	~30	~22	~30
Trace quantity, pcs	43	43	128	128	128
Bonding pads	one row	one row	two rows (staggered)	-	two rows (staggered)

Module Design and assembly

Screenshot

4.3.3.3 Hybrid circuit layout

The hybrid circuit used to accommodate the chips, drive out the signals and provide the services is being designed with the same aluminum-polymide cable technology as used in the present SSD, in two symmetric layouts corresponding to the two sides of the sensor. The power and interconnecting cable (also called *flex*) is glued on to a stiffener, that is made of five-layer carbon-fibre material. The flex is a two-layer bus used for power, digital i/o and analog outputs. The interconnections between the two layers are made by TAB bonded vias.

4.3.4 Module Design and Assembly

The front-end module of the upgraded strip detector is shaped in a very compact layout in order to guarantee a continuous sensitive area once integrated in the tracker layers. The flexibility of the interconnections should allow to arrange the front-end electronics of the whole module on the downstream side with respect to the incident particles, leaving sufficient space to accommodate the supports and the cooling services. Different options for the module layout are are being studied. Figure 4.17 shows a possible arrangement of the cables and the hybrids, before and after folding them on the sensor. At present, this option seems to allow the simplest assembly procedure and the most comfortable placement of the chips, optimizing at the same time the cable dimensions and the hybrid layout.

A specific session of test and quality control will be organized to carry out a complete static characterization of the sensors. The assembly procedure will foresee electrical and functionality tests at each processing step, allowing faulty component rejection and possible reworking before final integration in the complete module.

First strip module prototypes will be tested with beam particles to study the performance, the efficiency and the spatial resolution of the strip detector once the full chain is integrated in the module.

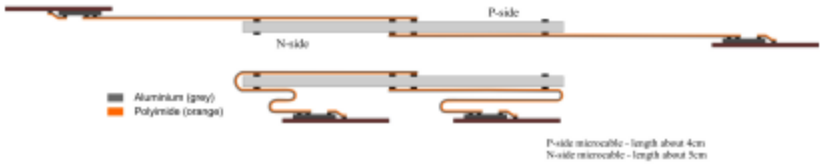
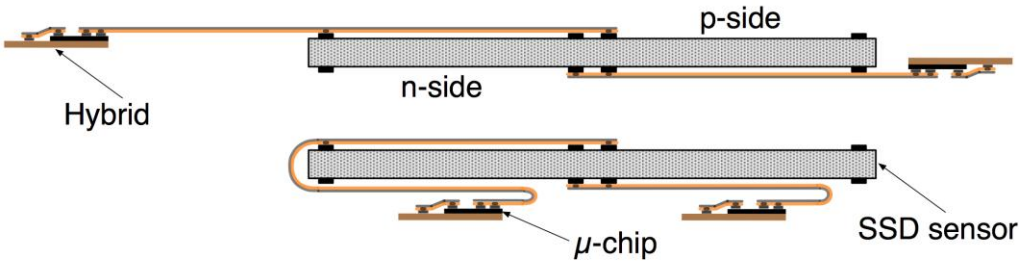


Figure 4.17: Schematic view of the strip module, in the open (top) and folded (bottom) configurations.

Module Design and assembly



- Several options for the assembly of chips, cables, sensor in the module:
  - folding configuration
  - hybrid layout (flex to accommodate the chips)
  - bonding procedure

Screenshot

4.3.3.2 Assembly test plans

Since the single-point Tape Automatic Bonding (TAB) technique becomes extremely challenging at small trace width and pitch, a set of dummy components with the proposed geometric characteristics are being fabricated in order to test and verify the possible solutions for module interconnection and assembly. Small pitch bonding tests and quality

- Assembly test plans
  - Dummy components productions (@FBK)
    - Sensor with new layout
    - Chips with different input pitches
  - Ready for next spring
  - TAB bonding plans with different pitches

4.4 Readout electronics

- Off-detector electronics and interface to ALICE central systems
  - Expected data throughput
  - Powering
    - DC-DC converters
    - Serial powering
    - Power consumption estimates for ‘all-pixels’ scenario

Screenshot

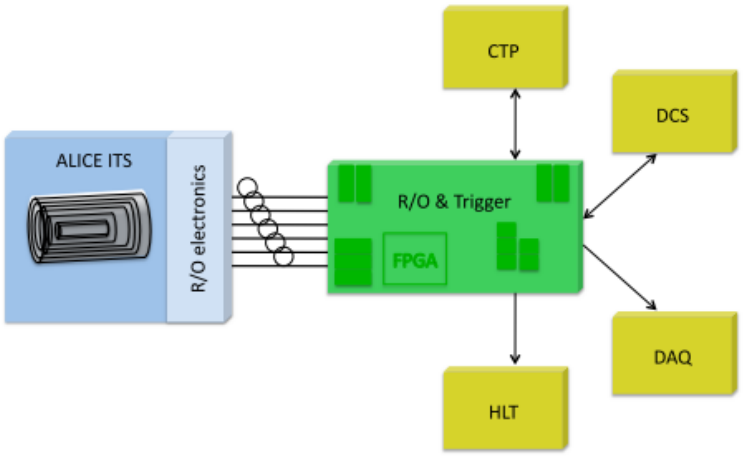


Figure 4.18: Illustration of an architecture for the upgraded ITS trigger and readout electronics (R/O). The connections to the central services (CTP-Central Trigger Processor, DCS-Detector Control System, DAQ-Data AQuisition, HLT-High Level Trigger) are indicated schematically.

4.5 Irradiation and Testbeam Plans

Screenshot

- Short description of the irradiation plans
  - evaluate TID damages on electronics (X-rays)
  - evaluate NIEL damages on sensors (hadrons)

4.5 Irradiation Plans

The radiation levels expected for the innermost layers of the future ALICE ITS will lead to radiation induce damage in the front-end electronics and the sensor parts as described in section 4.1.2.

Irradiation tests have started in 2011 and will be continued to investigate if the different technology options are sufficiently radiation resistant for the ALICE ITS upgrade. The tests are carried out to the respective radiation levels as described in table 4.2. A detailed annealing scenario is currently in preparation and will be based on the expected operating temperature (i.e. room temperature) and the foreseen accelerator operation schedule.

The irradiation tests can be distinguished in two groups: X-ray irradiation tests and hadron irradiation tests. While it is expected that the TID delivered during X-ray irradiation tests will lead to radiation induced damage mainly in the electronics parts, the non ionizing energy loss (NIEL) delivered by the hadrons will lead to lattice damage which manifests itself in the degradation of the sensor characteristics. Furthermore, during an

- Description of testbeam plans
  - MIP beams @PS-SPS
  - Estimate point space accuracy
  - Two track resolution
  - dE/dx capability

irradiation with charged hadrons (i.e. protons), there will be in addition TID effects. It is therefore necessary to carry out both types of irradiation tests to simulate the radiation environment in the ALICE experiment and to disentangle the radiation induced effects on the different components.

4.6 Testbeam Plans

The performance of the detector prototypes will be evaluated in dedicated beam test runs at the CERN SPS and PS. In addition to the electrical characterization and the irradiation measurements, the tracking performance of the detector prototypes being developed for the ITS upgrade will be evaluated by exposing them to minimum ionizing particle beams. The performance of monolithic and hybrid pixel as well as microstrip prototypes in terms of intrinsic point space accuracy, two track resolution and dE/dx capability will be evaluated and compared. We envisage also to study the detector performance in a

Chapter 4 – additions for V 2.0

- 1. Add one paragraph and table in 4.1.1 to list the two scenarios (8kHz 50kHz) and discuss the implications. Rework the bullet list in 4.1.1 in accordance with that
- 2. Add one sub-section at the end of 4.1.1 to discuss the possibility to make the innermost layer 0 with 0.1% X0
- 3. Add a paragraph (bullet) in 4.1.1 the option of having 2 layers with high time resolution
- 4. Add one sub-section in 4.1.1 to discuss in short possible read-out architectures in view of the two scenarios. Check the other sub-sections which mention architectures for inconsistencies and redundancy

Chapter 4 – additions for V 2.0

- 5. Table 4.3 Add a column with the yearly radiation values, eventually add a table only for layer 0 and layer 1 with the yearly values
- 6. 4.2.1 state that test-structures are being submitted to Tower for irradiation and functional tests in 2011
- 7. 4.3.3 Define the foreseen assembly tests on dummy strip components and describe the hybrid layout
- 8. 4.4.2 propose a powering scheme and present for example the one developed for ATLAS