The development of the multi PPD readout electronics with EASIROC and SiTCP

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Outline

Introduction

- J-PARC E40
- EASIROC

The evaluation board with EASIROC

Performance evaluation with a pulse generator

- Charge measurements
- Timing measurements
- Multi-hit TDC in the FPGA

Performance summary

- Expected dead time
- ADC, MHTDC readout with LED

Summary

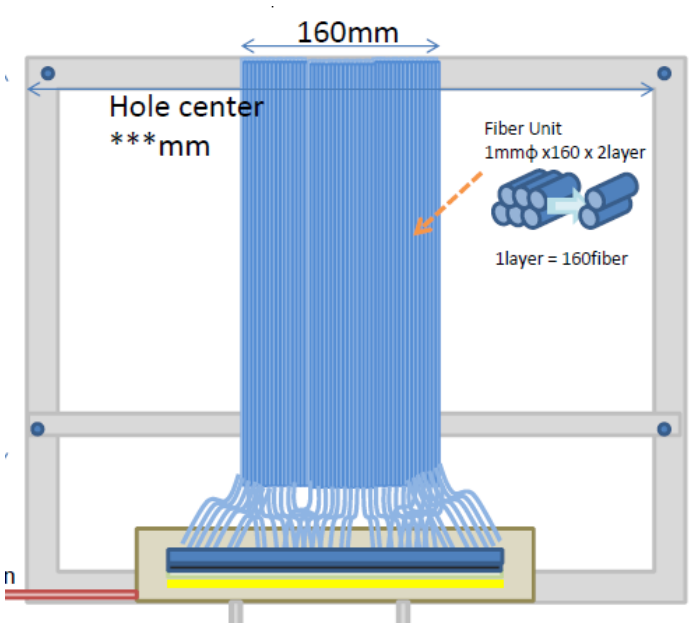
Introduction -J-PARC E40-

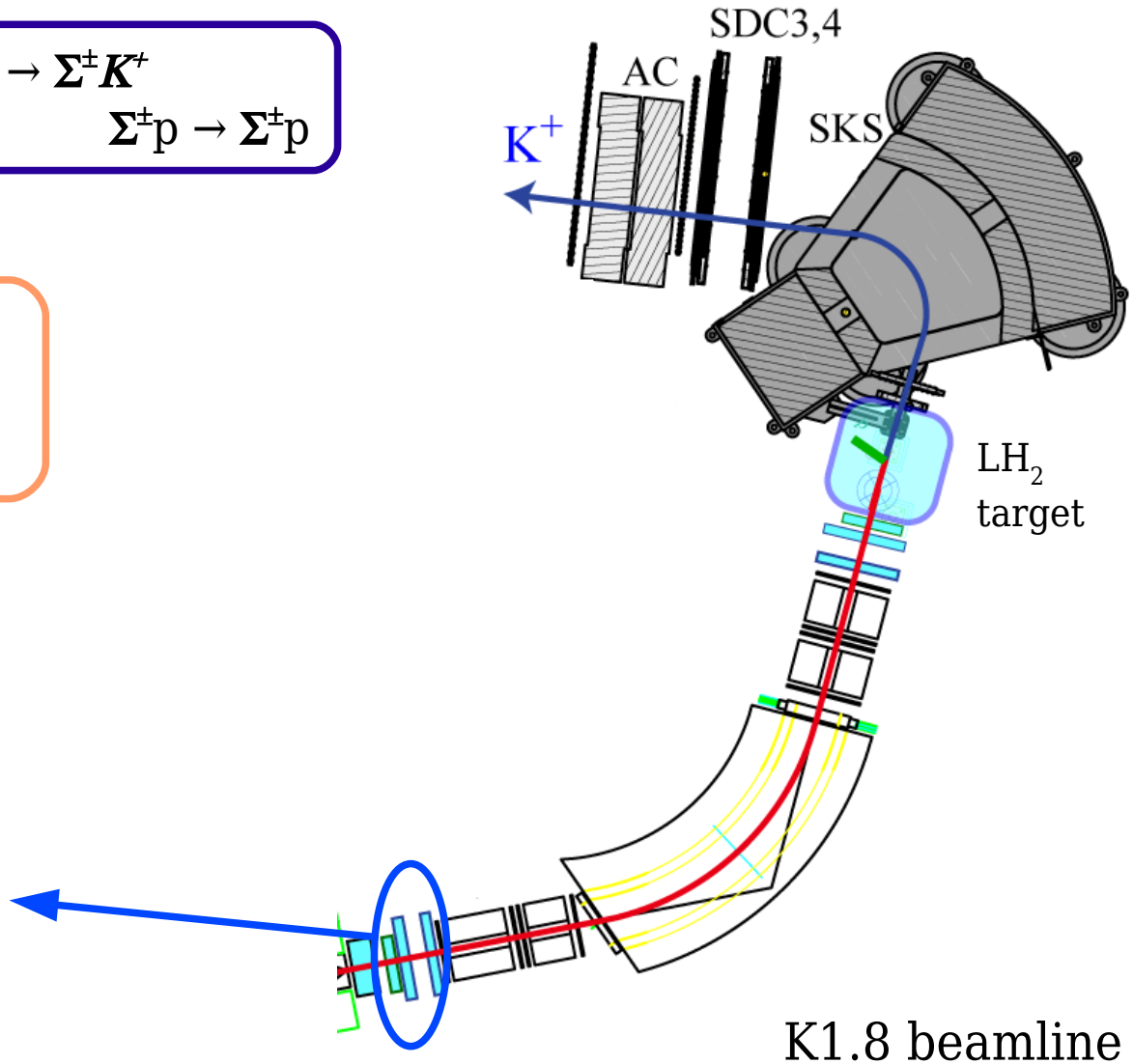
The experiment on **Σ**p scattering in K1.8 in J-PARC.
The measurement for the differential cross section,

- Σ^-p elastic
- Σ^+p elastic
- Σ^-p → Λn inelastic

π^+p → Σ^+K^+
$\Sigma^\pm$p → $\Sigma^\pm$p

The beamline fiber tracker
to measure position of
the π beam.





K1.8 beamline

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- Σ^-p elastic
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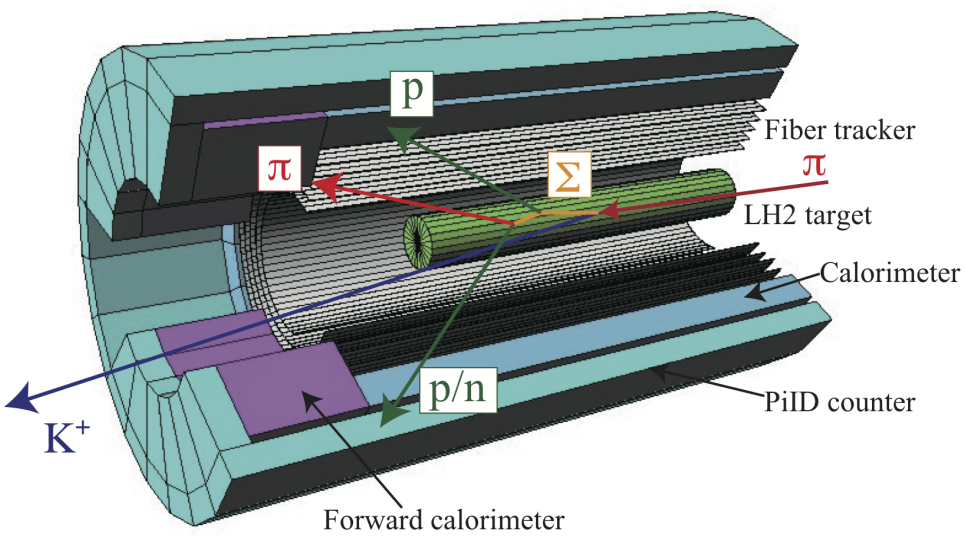
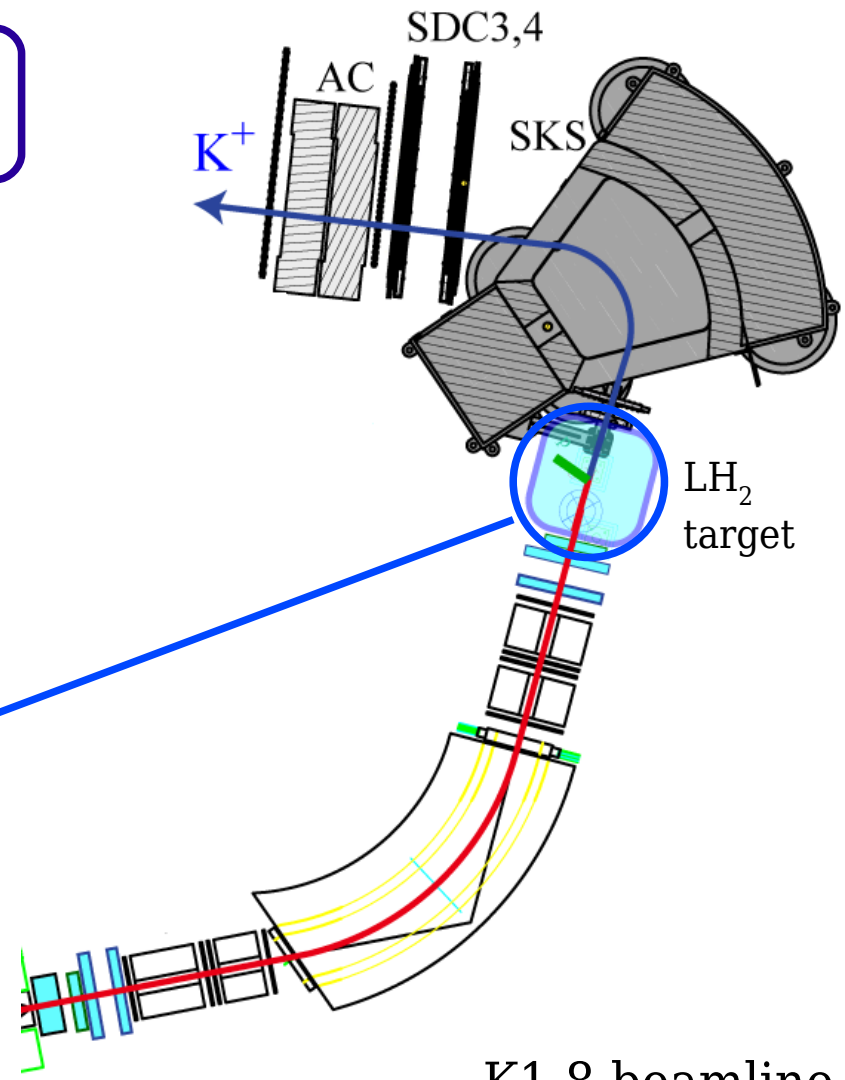
$\pi^{\pm}$p → $\Sigma^{\pm}K^{+}$
$\Sigma^{\pm}$p → $\Sigma^{\pm}$p

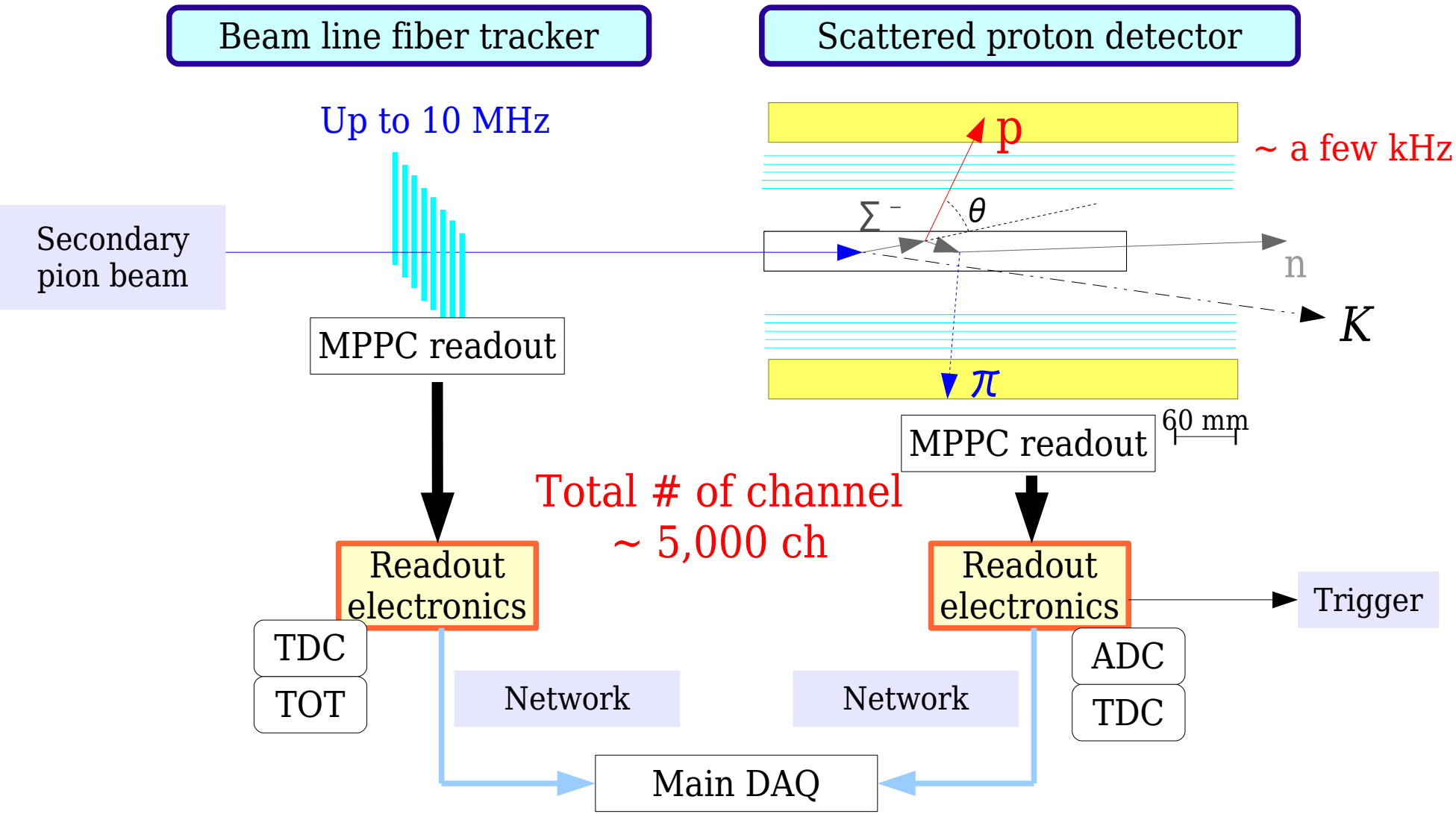
The scattered proton detector
to measure track and energy of
the scattered protons.





K1.8 beamline

Introduction -J-PARC E40-



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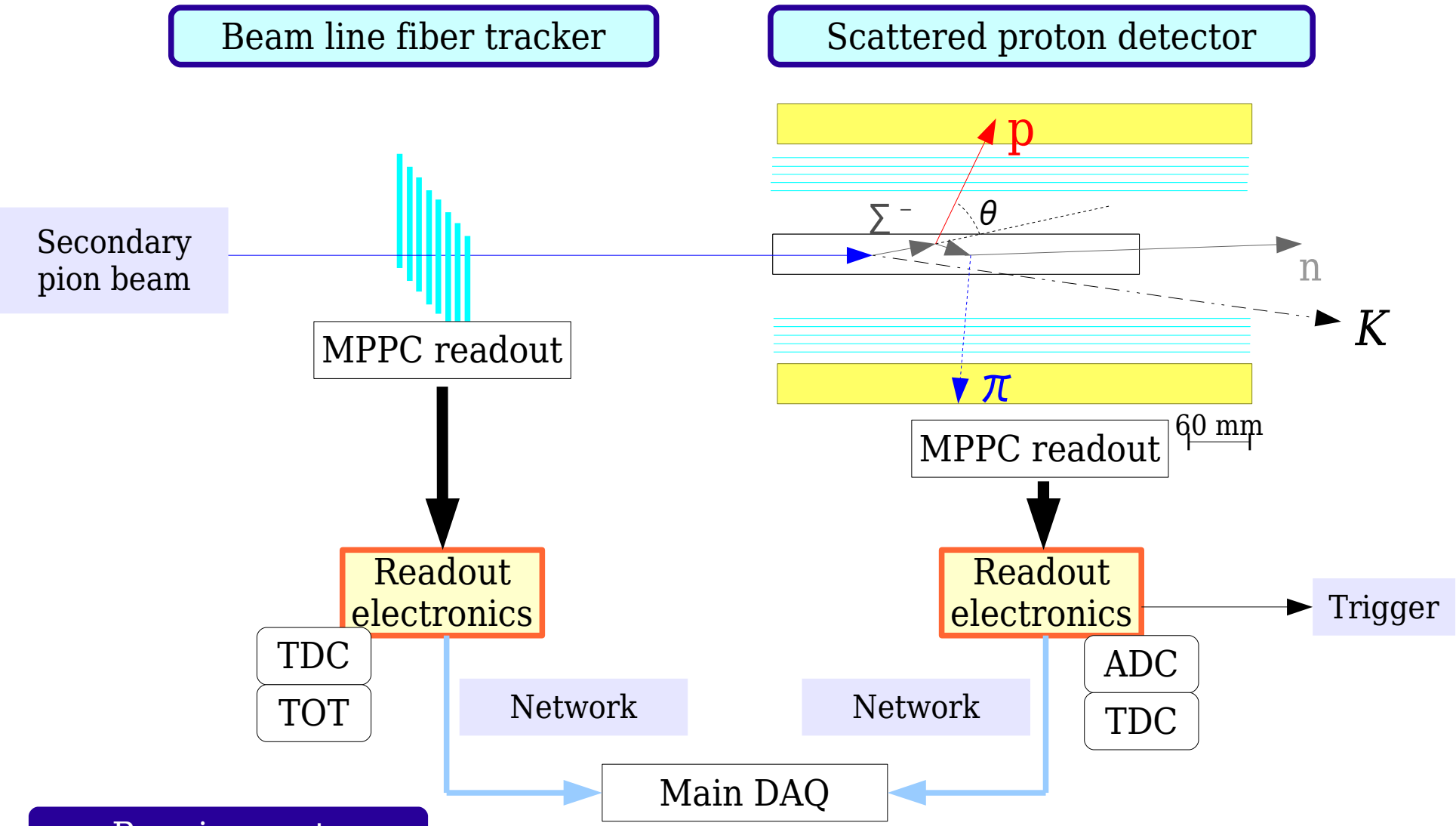

Requirements

- Handling multi MPPC
- Random trigger
- Charge and timing measurements
- Data transmit via network

Introduction -EASIROC-

EASIROC (Extended Analogue SiPM Integrated Read Out Chip)

- 32 channels inputs
- HV adjustment (4.5 V, 8 bit)
- Amp, shaper, discriminator
- Analog (serial)
- discriminator (parallel) outputs.

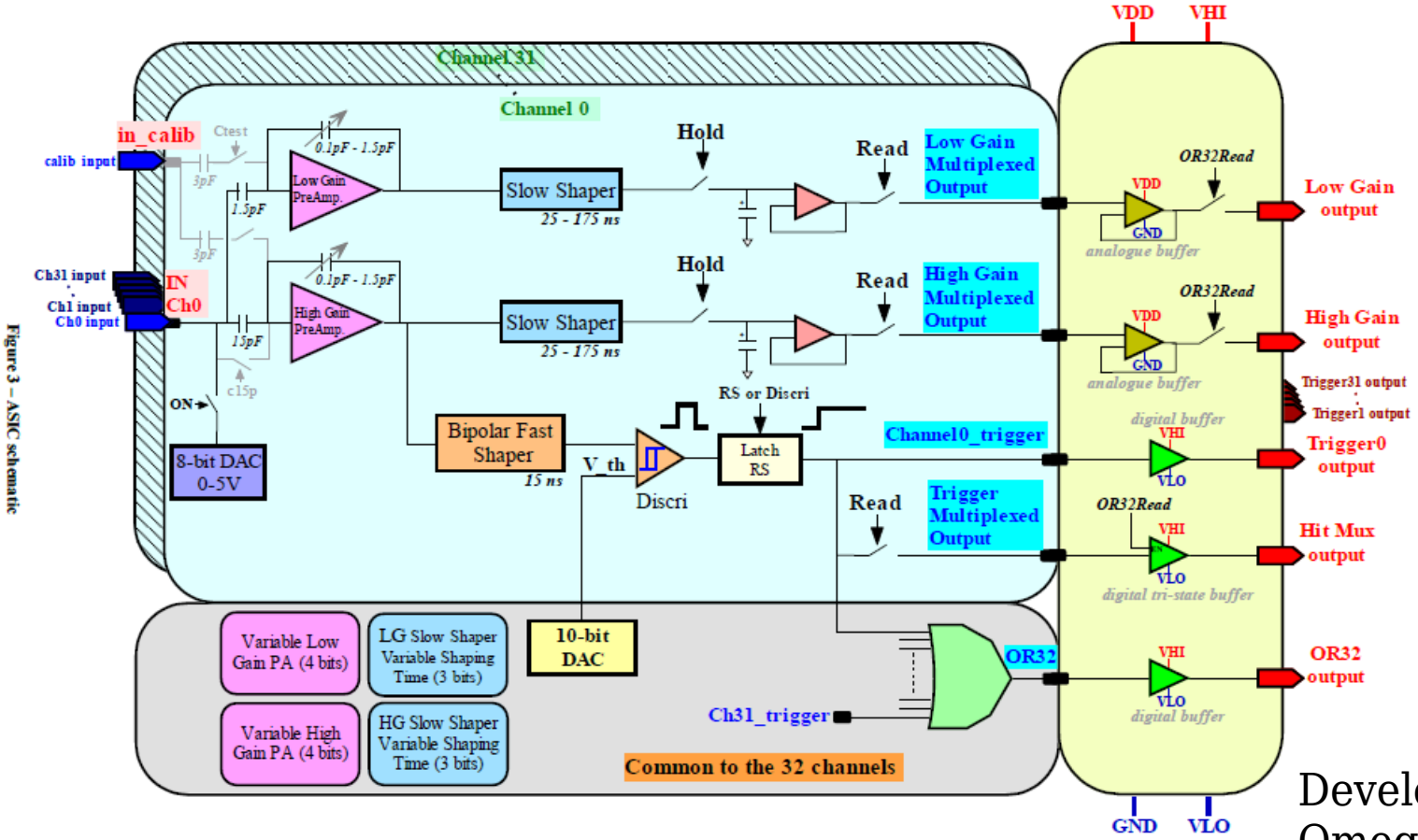

Figure 3 – ASIC schematic

Developed by Omega/IN2P3

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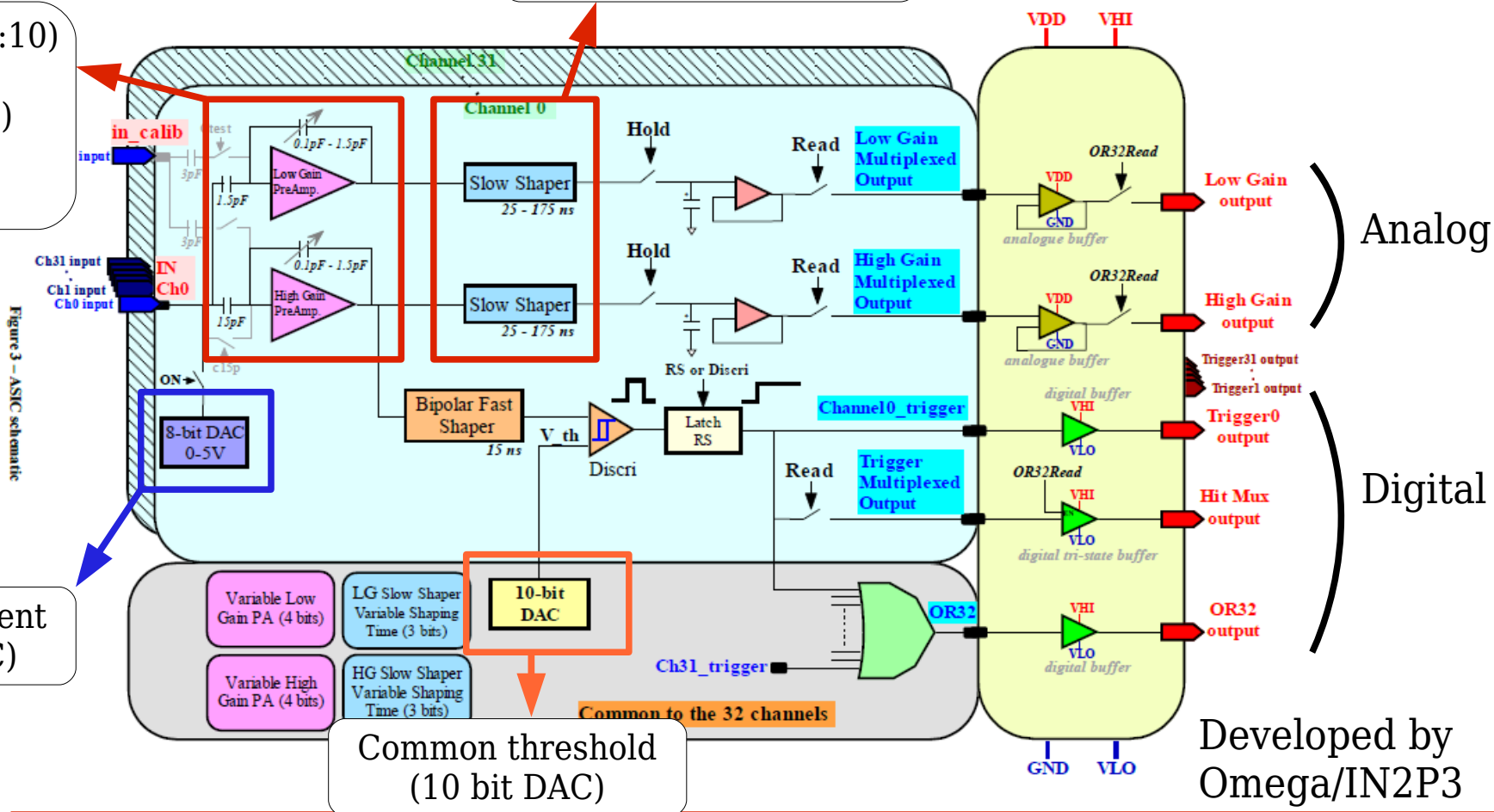
Shaper
(variable shaping time)
25 → 175 ns

Double gain (1:10)

- High gain
  (10 → 150)
- Low gain
  (1 → 15)



HV adjustment
(8 bit DAC)

Common threshold
(10 bit DAC)

Developed by
Omega/IN2P3

The evaluation board with EASIROC

I/O components

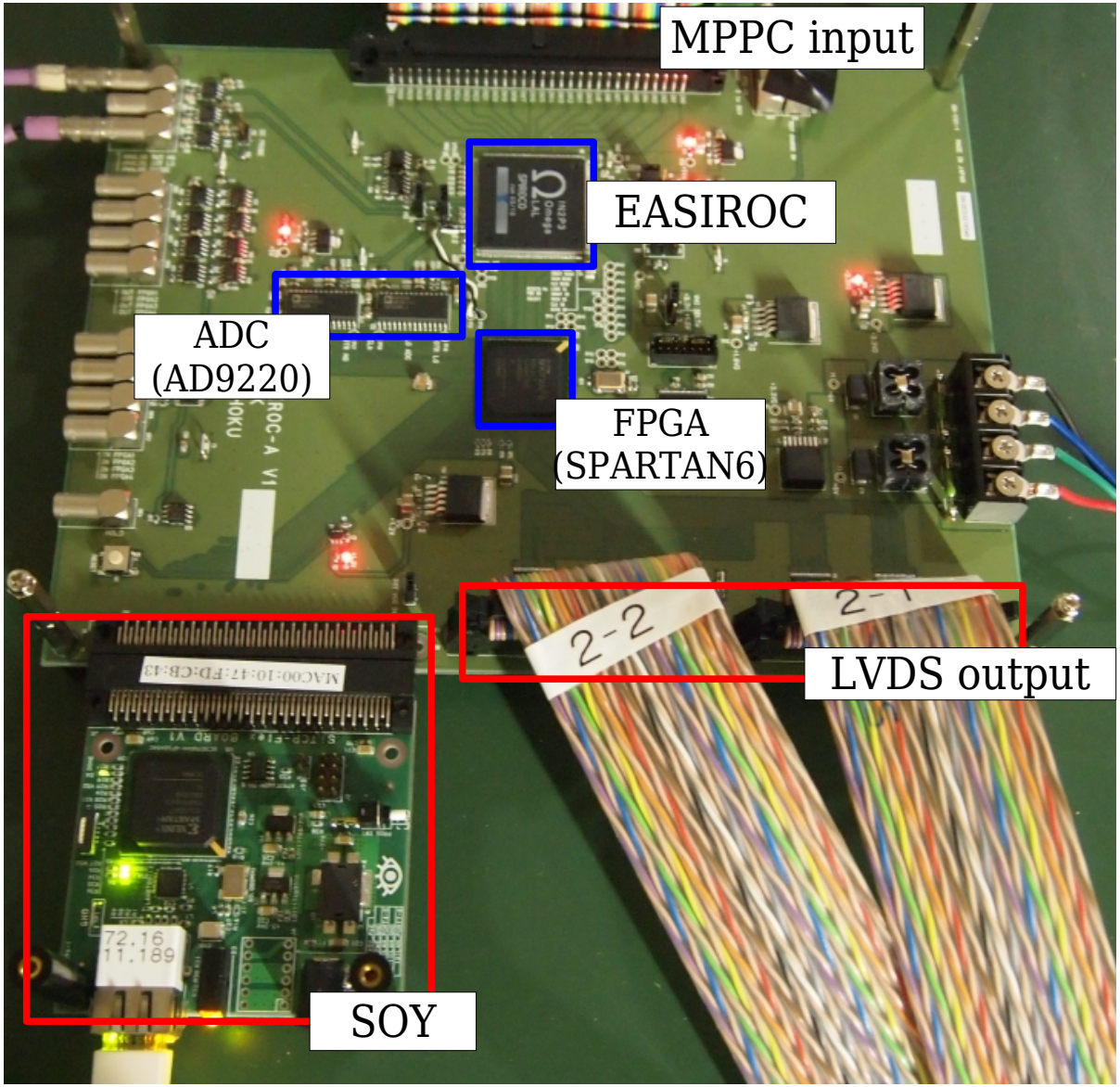
Analog I/O
- MPPC input (32 ch)
- HV input
- Analog output / probe output

Digital I/O
- NIM level input x5 (400 Mbps)
- NIM level output x4 (~ 1Gbps)
- LVDS output (640Mbps)
- SiTCP

On board ADC and TDC
- AD9220
- Digital MHTDC in FPGA

Power supply
- ±6 V

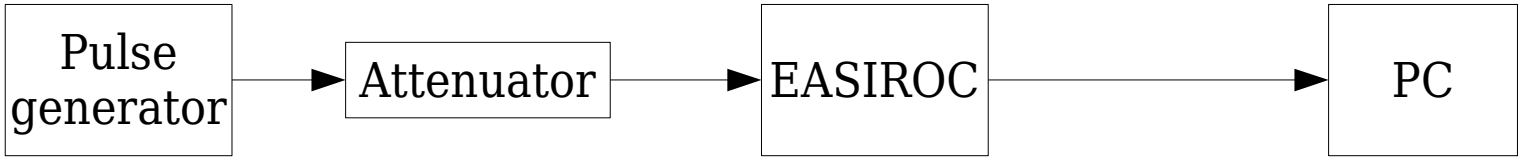
SOY (general purpose SiTCP board) is needed to use SiTCP.
Bandwidth : 100 Mpbs.

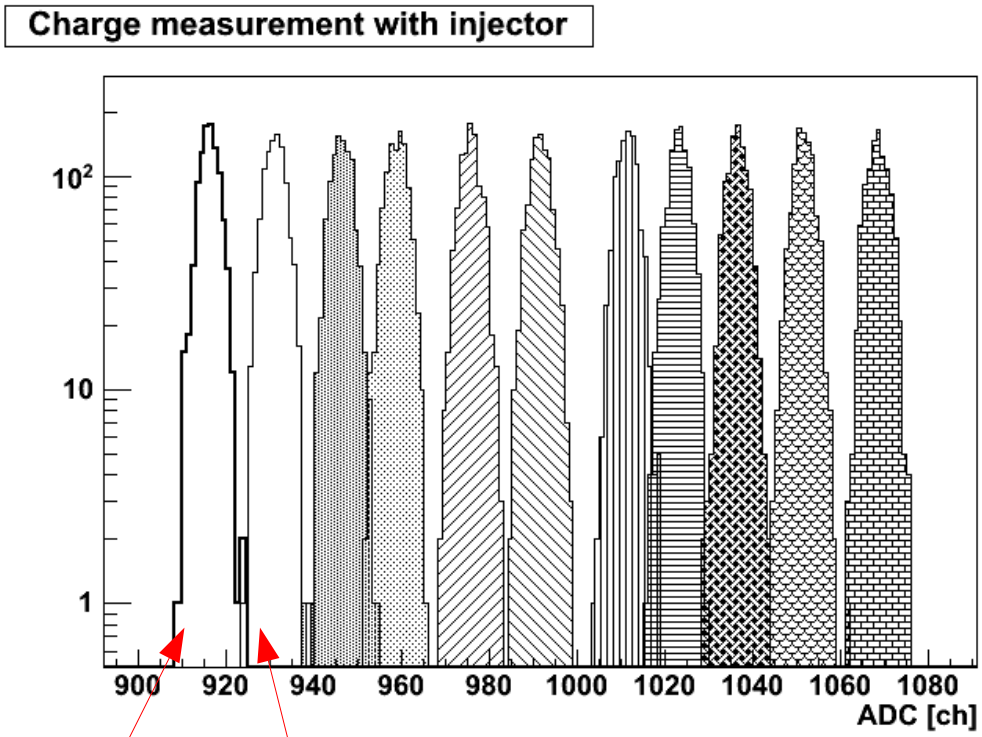


Test results

Performance evaluation : ADC

Test setup for the charge measurement





Pedestal 160 pC ~1 p.e

Assumption

gain = 10^6

(1 p.e ~ 160 pC)

SNR = $20\log_{10}(1\ p.e/bg(\sigma))$

~ 16 dB @ 1 p.e

C10507-11-100

~ 22 dB @ 1 p.e

C10507-11-050

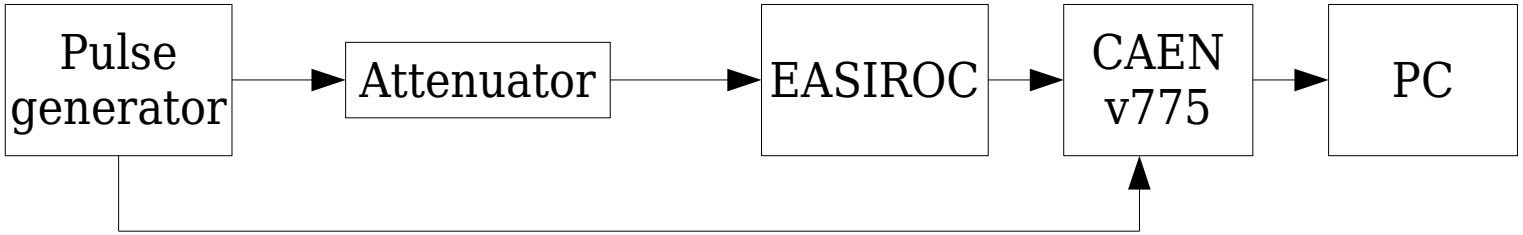
~ 14 dB @ 1 p.e

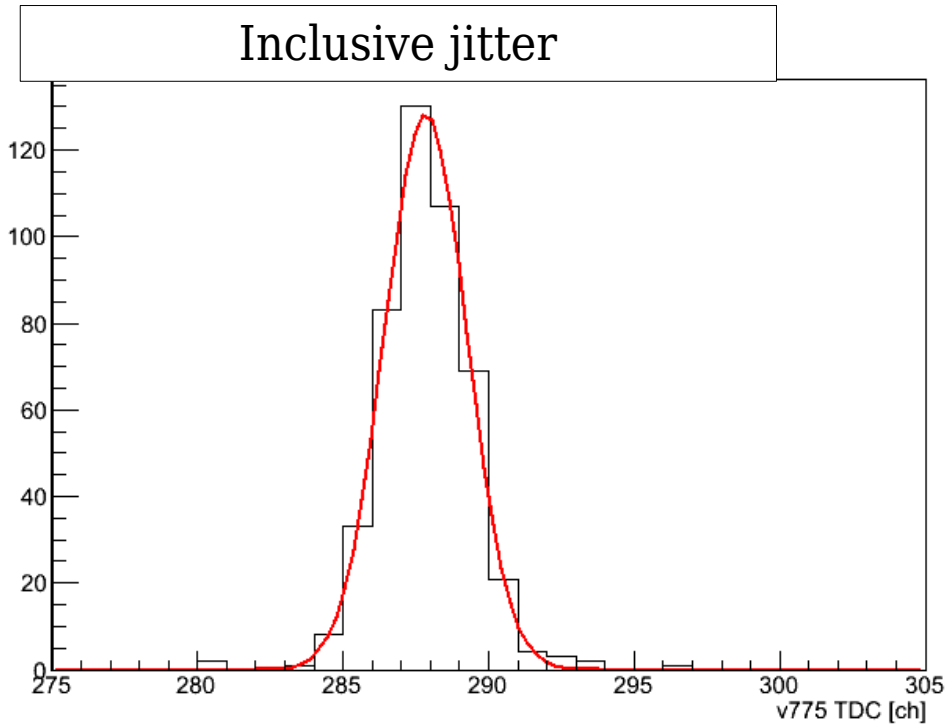
C10507-11-025

~ 4.2 dB @ 1 p.e

Performance evaluation : Input jitter

Test setup for the timing measurement





Inclusive jitter

~270 ps (σ) @ VTh = 0.5 p.e
(TDC 1 bin = 190 ps)

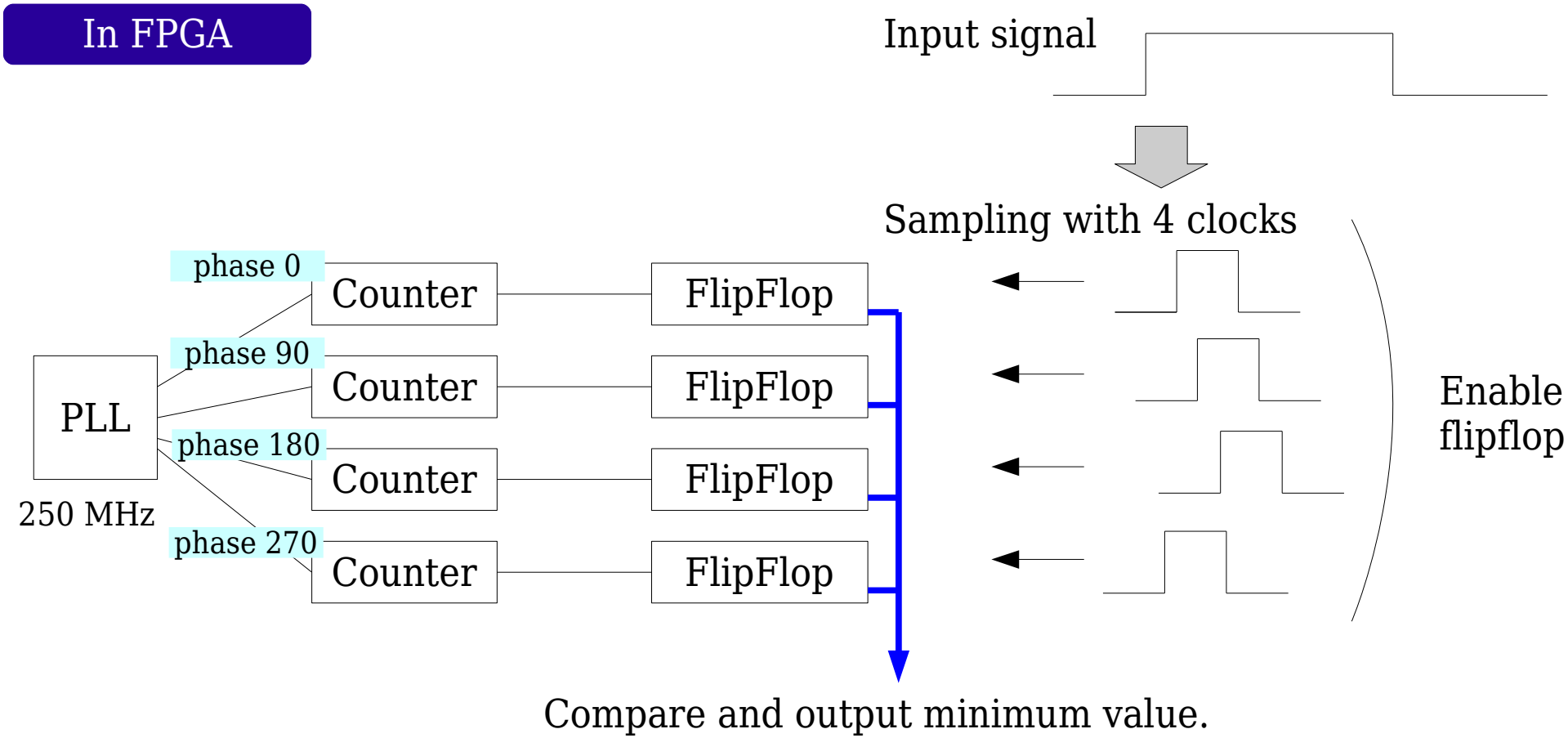
Including noise of
Attenuator
EASIROC itself

Sufficient performance for our application.

Performance evaluation : MHTDC

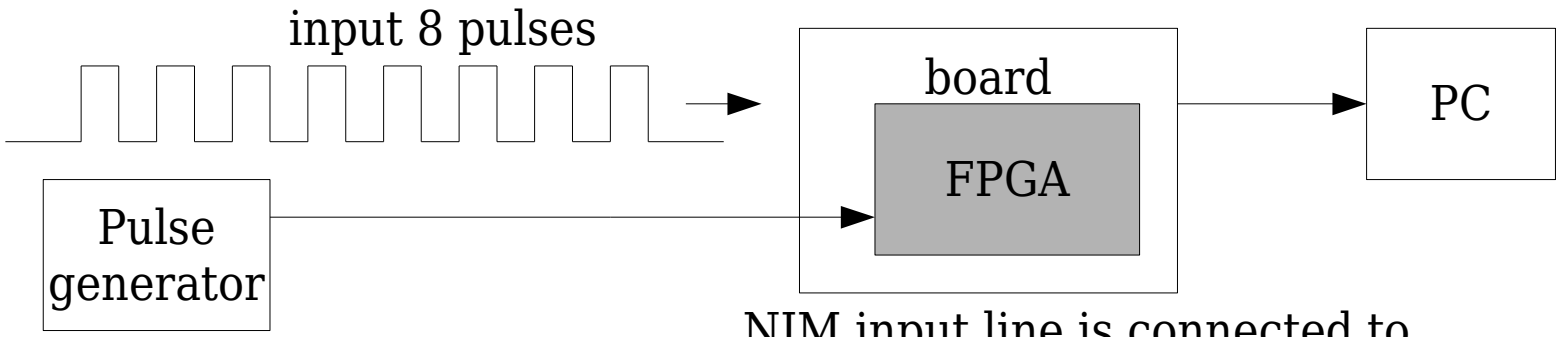
Multi-hit TDC in the FPGA

Time window	: 2 us
Depth	: 8
1 ch	: 1 ns
Stop	: Common stop mode



Performance evaluation : MHTDC

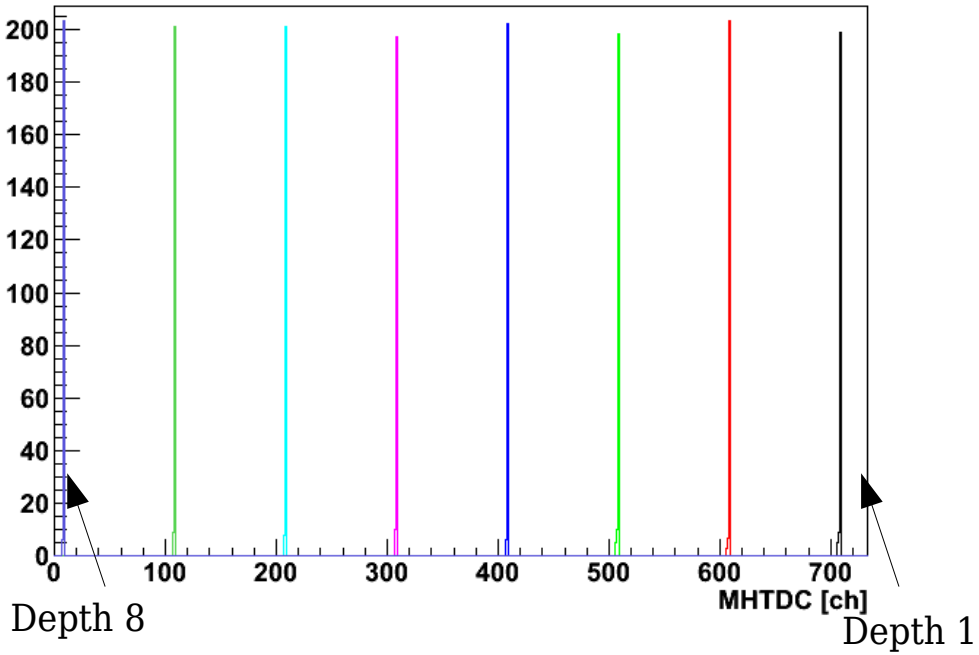
The test for the logic of MHTDC by using NIM input.



NIM input line is connected to MHTDC directly for this test.

Test result with clock input.

MHTDC depth test

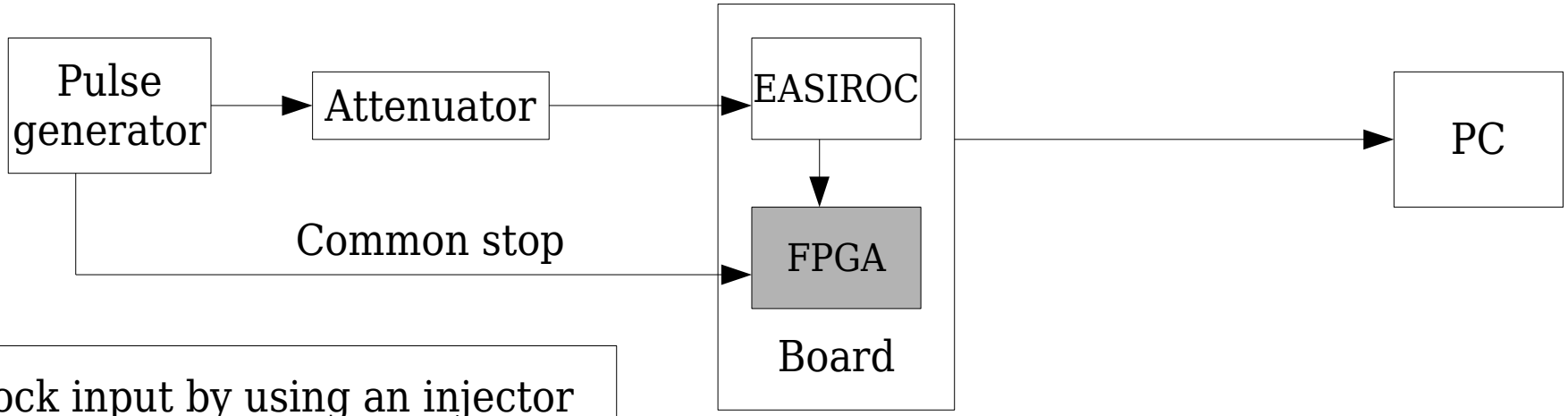


All input signals are stored in each buffer.

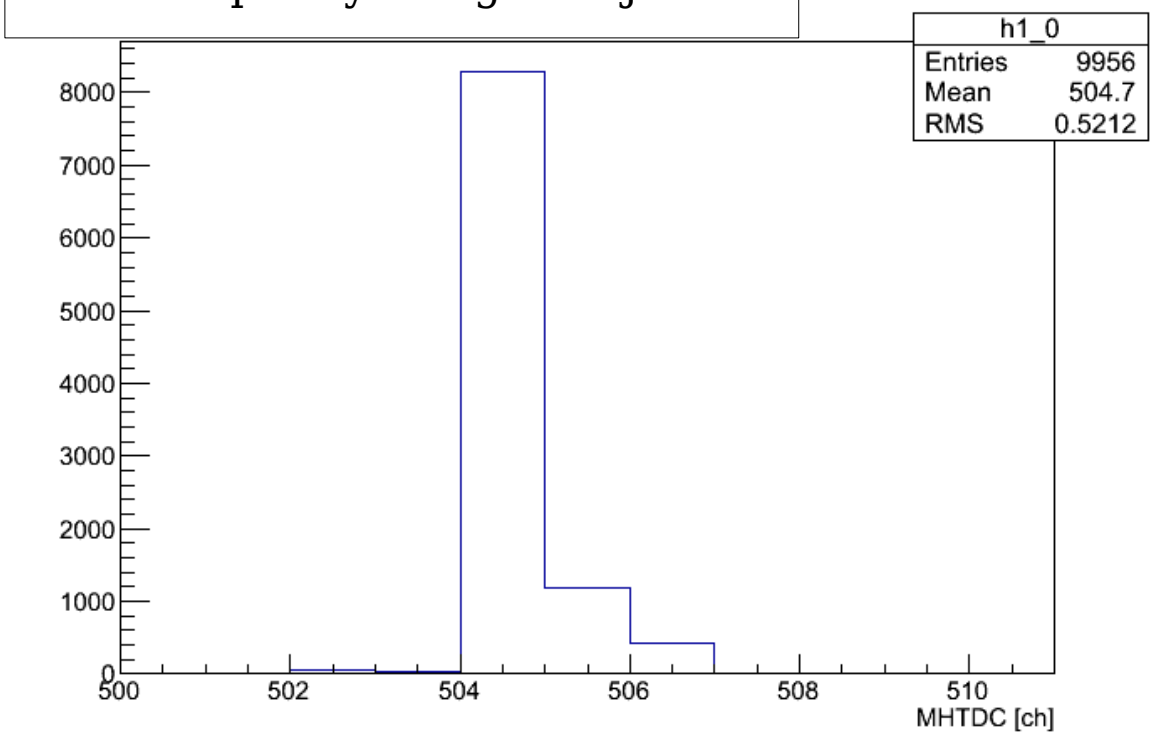
The logic works well as multi-hit TDC.

Performance evaluation : MHTDC

Evaluation for the resolution of the internal timing measurement part.



Clock input by using an injector



The resolution for the timing measurement

~530 ps (RMS) @ 0.5 p.e.

The best case achievable when we use the timing measurement function on this electronics.

Discriminator bus output (LVDS) is available if you need higher resolution.

Performance summary

Expected dead time in E40

Expected trigger rate in E40 : **3 kHz**

Mean dead time for expected event size.

conversion (ADC)	: 60 us (constant)
conversion (MHTDC)	: 1 us
data transfer	: 15 us
Total	: **~ 75 us**

Expected DAQ efficiency : **~80 %** (for random trigger)

→ Not high, but acceptable.

Readout pattern

Choose from the following:

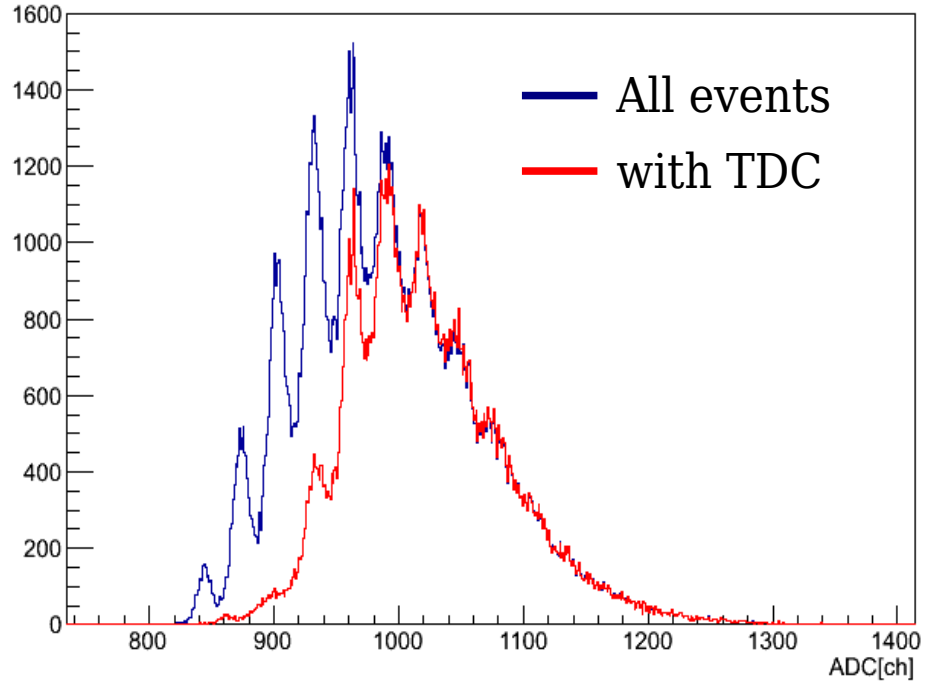
A) ADC + MHTDC
B) ADC
C) MHTDC

for pattern C), **7 kHz with DAQ efficiency 90 % is achievable.**

Performance summary

Demonstration of ADC and TDC readout

ADC histogram for LED



PPD : C10507-11-100 (HAMAMATSU)

VTh : 3.5 p.e
Trigger : LED timing

Readout of ADC and TDC for multi MPPC by one board is achieved.

Summary

We are planing to perform an experiment on **Σ**p scattering as J-PARC E40.

→ Measurement of the differential cross section of **Σ**p scatterings by using the liquid hydrogen target and the fiber trackers.

→ The development of the readout electronics for multi MPPC is essential, because the total number of MPPC is about 5,000.

The evaluation board with EASIROC and SiTCP was developed and tested.

→ SNR for the charge measurement was 16 dB for gain = 10^6

→ Inclusive jitter of this board was 270 ps (σ) @ VTh = 0.5 p.e

→ The MHTDC was implemented in the FPGA.

Time window	: 2 us
Depth	: 8
1 ch	: 1 ns
Resolution	: 530 ps (RMS) @ 0.5 p.e.

→ 80 % DAQ efficiency for 3 kHz random trigger.

The next version of the readout board will be developed in the next fiscal year.

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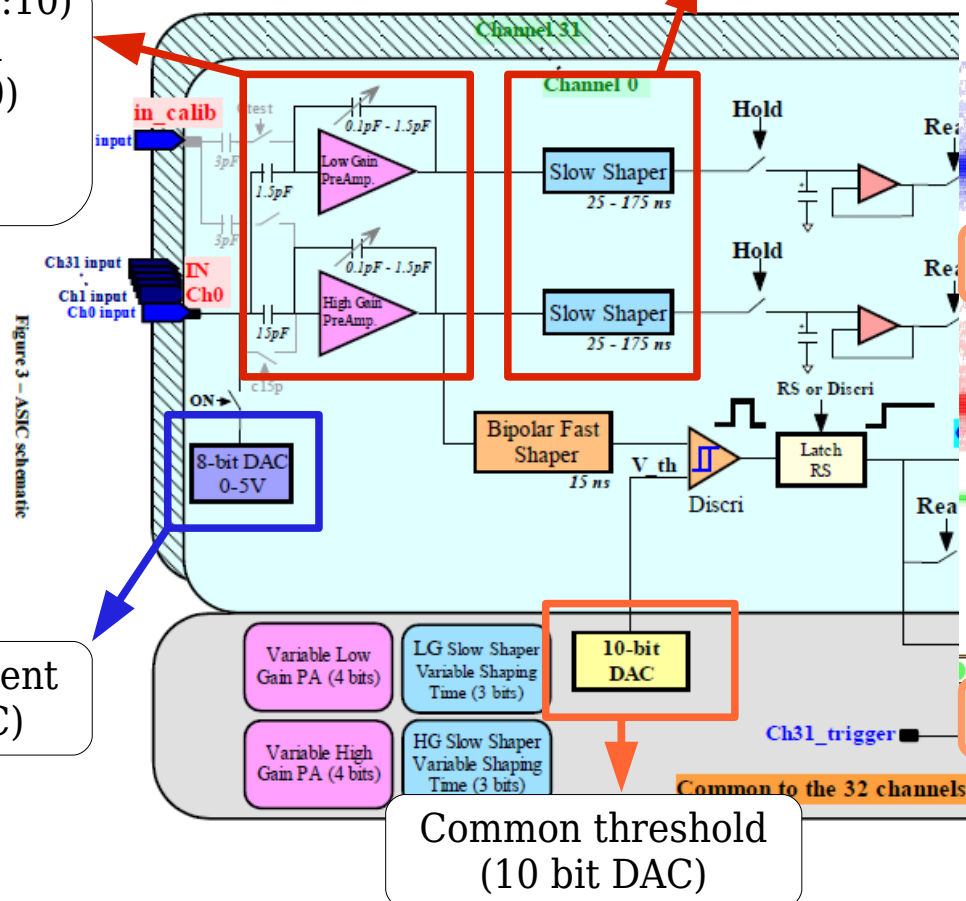

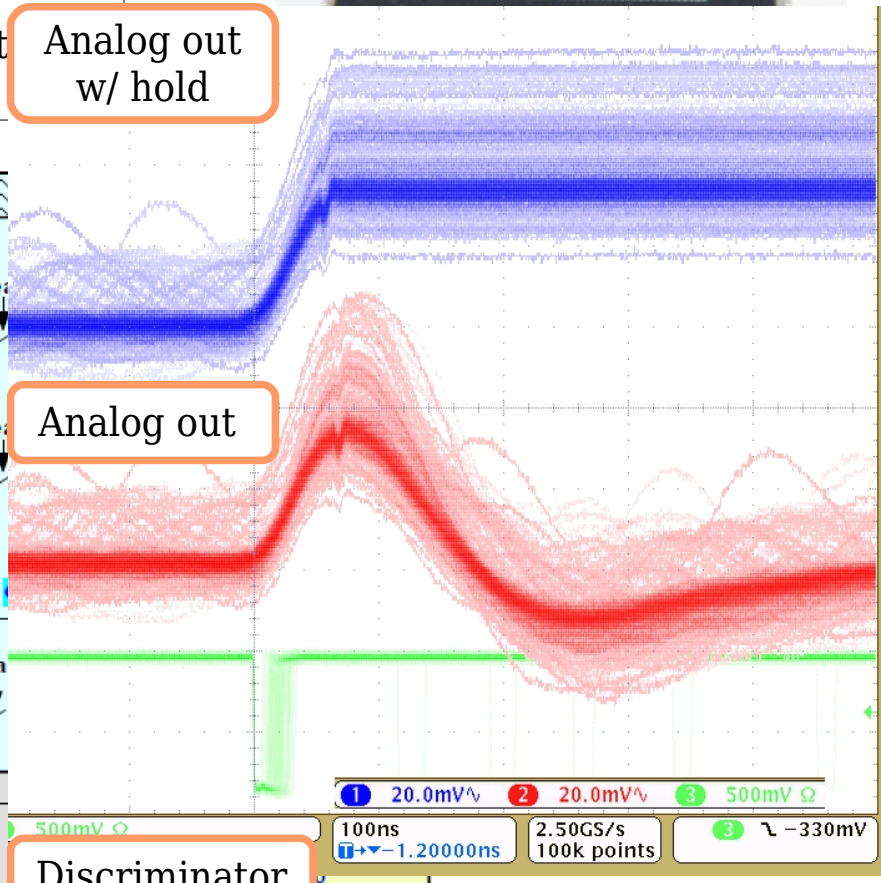

HV adjustment
(8 bit DAC)

Discriminator

Common threshold
(10 bit DAC)

Developed by
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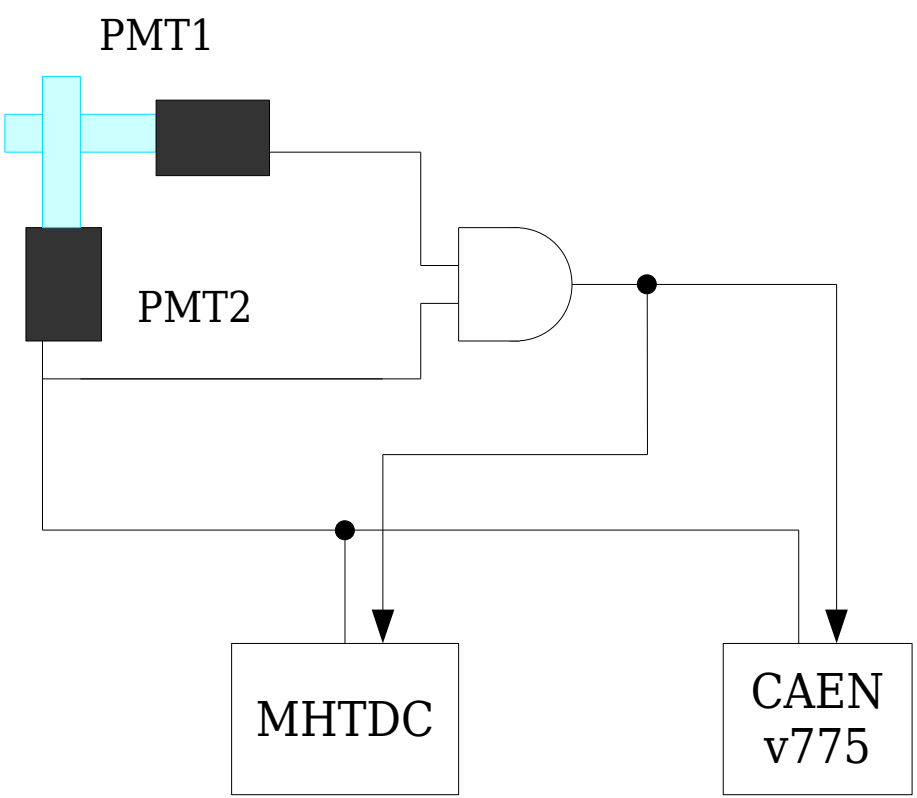
Multi-hit TDC in FPGA

Time window	: 2 us
Depth	: 8
LSB	: 1 ns
Stop	: Common stop mode



Test with PMT signal by using ^{90}Sr

Correlation between CAEN TDC and MHTDC
Common stop is coincidence of two PMTs.
(CAEN TDC LSB = 0.19 ns)