Picosec Contribution

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WP2 Goals

- Main Topic

  New PM designs and technologies

- ESR4

  Design of time-to-digital converter (TDC) arrays; readout of individual single-photon detecting pixels based on SPADs

- ESR5

  Design of single-photon detector arrays (SPADs) in CMOS; event-driven column readout or on-chip data reorganization;

Specific Goals: TDCs

- Study a the relations between performance measures in TDCs to guarantee an informed trade-off during a design
- Create a repository for FPGA TDCs to be freely accessible
- Create TDC textbook for our courses that could eventually extend Hansel's reference

Specific Goals: SPAD & R/O

- Study new and alternative guard rings for DCR reduction and FF increase in SPADs
- Explore alternative CMOS processes for SPAD design
- Create a R/O programmable harness (scout) that enables quick SPAD array development (like in RAMs and imagers) to be used in training programs

Training Programs

- 1-2 per year in Dutch Commonwealth
- The first one is proposed as a Summer school of 5 days, content:
  1. Fundamentals of SPADs and SiPMs
  2. Modeling, theory and practice
  3. TDC design
  4. SPAD-TDC system issues
  5. Readout Design

Training Programs (Cont.)

- **SPAD Boot Camp**
  - Understanding of SPAD design
  - Perform SPAD design
  - Understanding quenching
  - Understanding SiPM design
  - Perform mini-SiPM design
- **SPAD Imaging workshop** (5th Dec. 2012)

Secondment / Duty Missions

- ESR4 (from ST)
  Learn SiPM design and production in industry
- ESR5 (from Lisbon)
  Learn data processing
- ESR2 (to CERN)
  Learn SiPM SPAD readout
- ER2 (to Heidelberg)
  Learn SPAD developments & readout
- ESR12 (to Lisbon)
  Learn SPAD readout

Filling the Positions

- 2 interviews done
- 1 more TBD
- When will we make a decision?