Organisation européenne pour la recherche nucléaire

Handbook of Mitigation techniques against Radiation Effects for ASICs and FPGAs

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EN/STI group

Who am I?

- PhD graduated from Grenoble Polytechnic Institute (INPG) in 2010.
- Theme of my thesis:
  - Fault injection in SRAM-based FPGAs (software, laser beams & heavy ion particles)
  - Error rate prediction for applications embedded in SRAM-based FPGAs
- Post Doc (2010-2011) at TIMA laboratory (Grenoble): write a HandBook (HB) named “Mitigation techniques against Radiation Effects for ASICs and FPGAs”.
- Since September 2011: collaboration between TIMA laboratory and the CERN EN/STI group.

Outline

1. General description of HB and the context
2. Structure of the HB
3. Classification of mitigation solutions
4. List of techniques
5. Present & future

Definition of the Handbook

- ESA ITT (Invitation To Tender) : produce a handbook to help space application designers choosing appropriate mitigation solutions depending on their project requirements & constraints
- Target circuits: analogue, digital and mixed-signal ASICs and digital FPGAs
- Intended readers:
  - Junior engineers: provide background and detailed information
  - Confirmed engineers: Well classified and easy access to information, comparison tables, etc.
  - Experts: used as a checklist
- Levels of abstraction: from silicone to system architecture

Limiting the scope of the handbook

Problem: defining the limits of the handbook

- What technique should we include? According to which criteria? Which level of maturity should the techniques have?

=> Techniques exhibiting proof of efficiency: results at least from simulation or radiation results or having flown.

- What depth of information do we want to provide?
  - Too much details -> the HB would become enormous and this is not what ESA wants. Difficult to maintain & update
  - Not enough details -> HB = useless

The reader will find answers to What? What do I gain? What do I loose? But he will NOT find ~~How to do~~? He will have to find somewhere else => references are provided for this purpose.

Current version of the HB: 225 pages & more than 300 references

Technical content sources & authors

Technical content based on:

- State-of-the art techniques published in the scientific community (publications, workshops)
- Commercial solutions & vendors
- Volunteer contributions from experts :
  - Michael Alles, University of Vanderbilt (process and layout level)
  - Daniel Loveless, University of Vanderbilt (analogue & mixed-signal circuits)
  - Michael Nicolaidis, TIMA laboratory (digital circuits)
  - Fernanda Lima Kastensmidt, Universidade Federal do Rio Grande do Sul (digital circuits & FPGAs)
  - Melanie Berg, NASA (digital circuits & FPGAs)
  - Massimo Violante, Politecnico di Torino (embedded software)
  - Michel Pignol, CNES (system architecture)

Authors: Raoul Velazco (technical supervisor), Gilles Foucard (until September 2011) & Fabrice Pancher (since September 2011)

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Part 1: Radiation environment & its effects on ICs

① Radiation environment & effects on ICs

② Choosing a hardening strategy

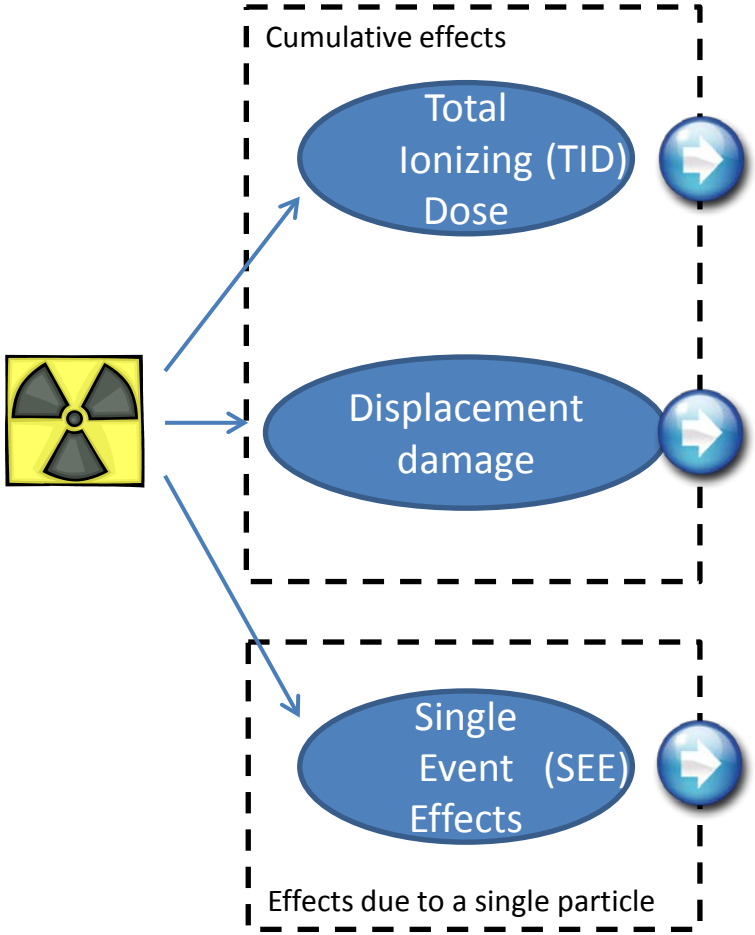
③ List of mitigation solutions

④ Validation tools & methodologies

- Radiation sources & environment
- Types of interactions between particles and matter
- Radiation effects on semiconductor devices

- *Section intended for beginner*
- *Provides background knowledge to understand to main topic of the HB*
- *Links to references*

Part 1: Radiation effects in semiconductors



Physical effects

- Charge deposition in insulating layers
- Creation of electron-hole pairs
- Etc.

- Atomic dislocation
- Nuclear displacement in lattice
- Reduction in mobility
- Etc.

- Local ionisation in active regions (transistors)

Electronic effects

- Threshold voltage shift
- Increase leakage currents
- Changes in circuit parameters
- Can lead to permanent failure
- Etc.

- Changes in circuit parameters
- Accelerated aging (reduce IC life time)
- Concerns mainly bipolar tr. and opto-electronic parts
- Etc.

- **SET**: transient current or voltage spike. Can propagate and be latched by memory element and result in a "bit-flip"
- **SEU**: temporary "bit-flip" of a memory element
- **SEL**: activation of a parasitic thyristor structure provoking high current flow. May lead to permanent failure
- Etc.

SET: Single Event Transient
SEU: Single Event Upset
SEL: Single Event Latchup

Part 2 : Choosing a design hardening strategy

① Radiation environment & effects on ICs

② Choosing a hardening strategy

③ List of mitigation solutions

④ Validation tools & methodologies

Countermeasures:

- What are they?
- Who apply them?
- At which level are they applied?
- How do I select a mitigation technique?
- Should I apply several techniques?

Part 2: Choosing a design hardening strategy

Goal: help the reader identifying the constraints of his project:

- What will the final environment of my application be: Nature, energy and density of the particles?
- What is the reliability I want to reach? (Mission duration -> TID threshold, Number of tolerated bit-flips -> SEU error rate)
- What is the deadline of this project? (Short term-> prefer commercial solutions, long term-> possible to develop the HW and SW, maybe an ASIC)
- What is the budget for the project? Low budget -> difficult to develop an ASIC.

Three hardening strategies:

- Full custom: develop the HW & SW + qualification. an ASIC will provide the best performance/power consumption ratio but it is costly and time consuming.
- COTS (Commercial parts): cheap and available but need to qualify them.
- Space qualified solutions: qualified but expensive and not always possible to acquire them (ITAR*)

Answering these questions helps choosing a hardening strategy.

Sometimes the constraints are too tight and there is not a solution => compromises must be found.

*ITAR: International Traffic in Arms Regulations

Part 4: Validation tools & methodologies

① Radiation environment & effects on ICs

② Choosing a hardening strategy

③ List of mitigation solutions

④ Validation tools & methodologies

- Real life tests
- Accelerated ground tests
  - Particle accelerators
  - Laser beams
- HW/SW fault injections at different levels (transistor, gate, device, etc.)

- *Section intended for beginner*
- *Provides an overview of the different means to validate a design*
- *Links to references*

Part 3: List of mitigation solutions

① Radiation environment & effects on ICs

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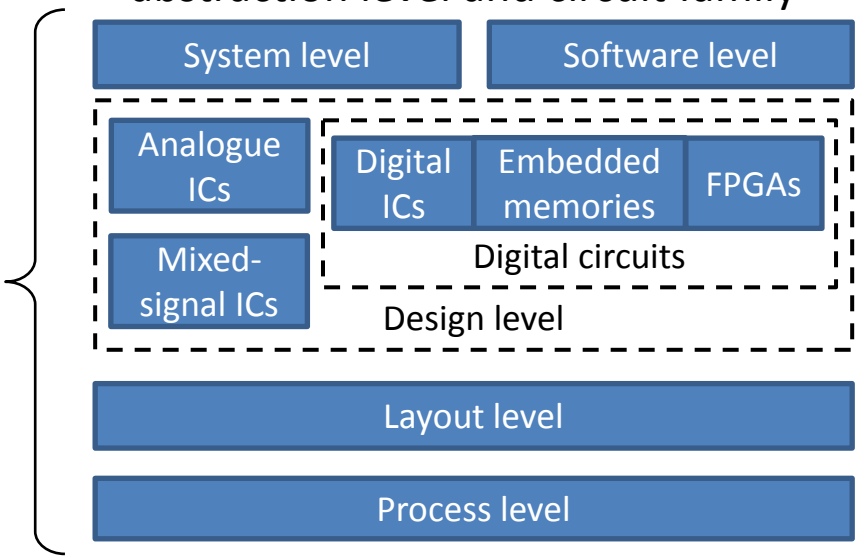
③ List of mitigation solutions

④ Validation tools & methodologies

Classification of the techniques by abstraction level and circuit family



Design level: need to classify techniques by circuit family and circuit type

- Analogue circuits
- Mixed-signal circuits
- Digital circuits
  - FPGAs
  - ASICs
  - Embedded memories

Handbook chapter structure

5. Radiation environment and integrated circuits

6. Choosing a design hardening strategy

7. Technology selection and process level mitigation
8. Layout
9. Analogue circuits
10. Digital circuits
11. Mixed-signal circuits
12. FPGAs
13. Embedded memories
14. Embedded software
15. System architecture

List of mitigation solutions

16. Validation methods

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Organization of a chapter

Chapters presenting mitigation solutions are organized as follow:

- Scope
  - What devices are concerned?
  - Which are the main radiation effects encountered?
  - The major strategies adopted by the techniques
  - Etc.
- Table of effects vs mitigation techniques
- List of mitigation techniques -> ID cards
- Additional information such as commercial solutions, radiation-hardened libraries, comparison of the techniques, etc.

Mitigation techniques vs radiation effects

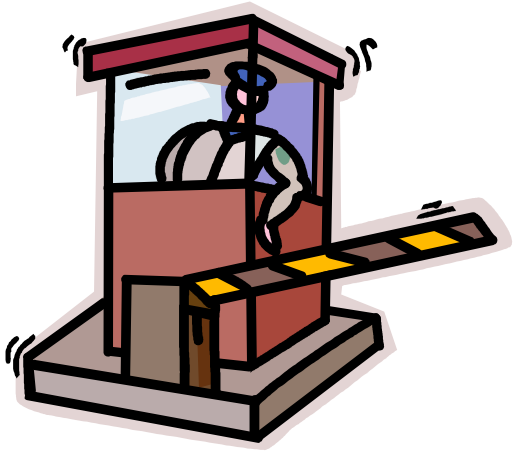
Example of table summarizing techniques applied at system level and the effects they mitigate

Mitigation techniques		Abstraction level	Radiation effects					Page
			TID	SEL	SET	SEU	SEFI	
15.3.1	Shielding	Architecture	X	X	X	X	X	167
15.3.2	Watchdog timers	Architecture					X	169
15.3.3	Latching current limiters	Architecture		X				171
15.3.4	Duplex architectures	Architecture			X	X	X	173
15.3.5	Triple Modular Redundancy	Architecture			X	X	X	177
15.3.6	Error Correcting Codes	Architecture			X	X		180

ID cards

Information for each presented technique are organized according to a predefined template

-> easier for the reader to find the information



ID CARD

- Description of the concept
- Figures/diagram
- Examples
- Available test data (simulation, radiation testing, in-fight)
- Added value
- Known issues
- Summary table (example below for a HIT memory cell)

IC family	Memories
Abstraction level	Design
Pros	SEU hardness
Cons	Area penalty: ~10% Power consumption penalty : ~30%
Mitigated effects	SEU
Suitable validation methods	Accelerated ground tests HW/SW fault injection HDL simulation
Automation tools	N/A
Vendor solutions	N/A

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Mitigation solutions @ process level

- Mitigation techniques

Mitigation techniques		Radiation effects				Page
		TID	SET	SEU	SEL	
7.3.1	Epitaxial layers				X	36
7.3.2	Silicon On Insulator		X	X	X	37
7.3.3	Triple wells		X	X	X	41
7.3.4	Buried layers		X	X	X	43
7.3.5	Dry thermal oxidation	X				44
7.3.6	Implantation into oxides	X				46

- Technology scaling and radiation effects
  - Effects of technology scaling on TID sensitivity
  - Effects of technology scaling on SEE sensitivity

Mitigation solutions @ layout level

- Mitigation techniques

Mitigation techniques		Radiation effects					Page
		TID	SEL	SET	SEU	MBU/MCU	
8.3.1	Enclosed Layout Transistor	X		X	X		51
8.3.2	Contacts and guard rings		X			X	53

- Radiation hardened libraries
  - ESA DARE (Design Against Radiation Effects)
  - CERN 0.24 µm
  - BAE 0.15 µm
  - Ramon Chips 0.18 µm and 0.13 µm
  - Aeroflex 0.6 µm, 0.25 µm, 0.18 µm and 90nm
  - Atmel 0.35 µm and 0.18 µm
  - Etc.

Mitigation solutions for analogue circuits

- Mitigation techniques

Mitigation techniques		Abstraction level	Radiation effects	
			SET	SEU
9.3.1	Node separation and Interdigitation	Design/Layout	X	X
9.3.2	Analogue Redundancy	Design	X	
9.3.3	Resistive Decoupling	Design	X	X
9.3.4	Filtering	Design	X	X
9.3.5	Modifications in Bandwidth, Gain, Operating Speed, and Current Drive	Design	X	
9.3.6	Reduction of Window of Vulnerability	Design	X	X
9.3.7	Reduction of High Impedance Nodes	Design/Layout	X	
9.3.8	Differential Design and Dual Path Hardening	Design/Layout	X	X

Mitigation solutions for digital circuits

- Mitigation techniques

Mitigation techniques		Radiation effects		Page
		SET	SEU	
10.3.1	Spatial redundancy	X	X	90
10.3.2	Temporal redundancy	X	X	94

- Others mitigations strategies
  - Memory cell hardening (see chapter 13)
  - Information redundancy: error detection and error correcting codes (see section 15.3.6)
- Commercial solutions
  - Radhard circuit manufacturers (Aeroflex, Atmel, Honeywell, Intersil, Xilinx, etc)
  - Radhard processors: architecture, radiation test results, missions (Honeywell RH32, Atmel AT697, etc)
  - Radhard computers : processor, radiation test results, missions (Space Micro Proton products, Maxwell SCS750, etc)

Mitigation solutions for mixed-signal circuits

- Mitigation techniques

Mitigation technique		Abstraction level	Radiation effects	Page
			SET	
11.3.1	Triple Modular Redundancy	Design	X	101

Mitigation solutions for FPGAs

- Mitigation techniques

Mitigation techniques		Abstraction level	Radiation effects			Page
			SET	SEU	SEFI	
12.3.1	Local TMR	HDL		X		106
12.3.2	Global TMR	HDL	X	X		108
0	Large grain TMR	HDL	X	X		111
0	Embedded user memory TMR	HDL	X	X		113
12.3.5	Voter insertion	HDL	X	X		114
12.3.6	Reliability-Oriented place and Route Algorithm	FPGA layout	X	X		117
12.3.7	Temporal redundancy	HDL	X			119
12.3.8	Embedded processor redundancy	HDL	X	X	X	121
12.3.9	Scrubbing	System		X		122

- Vendor solutions (Aeroflex, Actel, Xilinx, etc)
- Device comparison for space applications

Mitigation solutions for embedded memories

- Mitigation techniques

	Mitigation techniques		Abstraction level	Radiation effects		Page
				SEU	MBU	
Optimization of cell layout	13.3.1	Resistor memory cell	Design	X		135
	13.3.2	Capacitor memory cell	Design	X		137
	13.3.3	IBM hardened memory cell	Design	X		139
	0	HIT hardened memory cell	Design	X		141
	13.3.5	DICE hardened memory cell	Design	X		142
	13.3.6	NASA-Whitaker hardened memory cell	Design	X		144
	0	NASA-Liu hardened memory cell	Design	X		146
Optimization of memory layout	13.3.8	Scrambling	Architectural	X	X	147

- Error detection and error correcting codes (see section 15.3.6)
- Comparison between hardened memory cells

Mitigation solutions for embedded software

- Mitigation techniques

Mitigation techniques		Radiation effects				Page
		SET	SEU	MBU	MCU	
14.3.1	Redundancy at instruction level	X	X	X	X	153
14.3.2	Redundancy at task level	X	X	X	X	159
14.3.3	Redundancy at application level	X	X	X	X	163

Mitigation solutions @ system level

- Mitigation techniques

Mitigation techniques		Abstraction level	Radiation effects					Page
			TID	SEL	SET	SEU	SEFI	
15.3.1	Shielding	Architecture	X	X	X	X	X	167
15.3.2	Watchdog timers	Architecture					X	169
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- Description of commercial solutions
  - Space Micro Proton platform
  - Maxwell SCS750
- Examples of adopted architectures onboard satellites

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Present & future

Presentation of the final draft @ ESTEC on Dec. 9, 2011. About 100 attendees to judge the quality of the HB.

A questionnaire was proposed for attendees to give their opinion:

- Finding information
  - 65% easily found
  - 20% found with difficulty
  - 15% not found
- Do you think the content is adapted to your needs?
  - 65% yes
  - 5% no
  - 30% moderately
- What do you think of an electronic version of the handbook in relation to your activity?
  - 30% essential
  - 60% useful
  - 10% why not

Present & future

What's coming next?

Short future:

- Submission of the handbook to the ECSS* committee in order to become an ECSS handbook

Proposition to ESA:

- Website version of the HB, depending on ESA good will. There is a real demand from the community
- Search engine where the user enters his mission parameters and the tool outputs techniques compatible with the user's constraints

* European Cooperation for Space Standardization

Any questions?

If you have any corrections, suggestions or remarks please contact:

- Raoul Velazco: raoul.velazco@imag.fr
- Fabrice Pancher: fabrice.pancher@imag.fr
- Myself: gilles.foucard@cern.ch

- Any questions?