Contribution ID: **90** Type: **Poster**

Production Test Engineering in FE-I4 System-on-Chip to boost the Reliability and High-Quality demands in IBL applications

Thursday, 20 September 2012 17:36 (1 minute)

The article addresses production test development effort of the ATLAS FE-I4 integrated circuit. This particular production test targets manufacturing faults in the ICs and has been taken as a supplementary approach, besides standard functional test, to decrease further the risk of potential application failures. The Design-for-Test structures inside the digital part of the chip together with the specially devised top-level simulations enabled straightforward test development and debug in the production test environment. The production test itself has been commissioned to the external test company, with the supervision of the FE-I4 team at the test floor.

Summary

The ATLAS Insertable B-Layer (IBL) detector will make use of a large number of FE-I4 pixel readout chips with DC-coupled sensors mounted on top with negative charge collection. The FE-I4B samples from the second engineering run arrived at the end of 2011. Consequently, a new round of characterization and functional test, including the high-volume production wafer-testing, kicked off. However, the first production test development efforts can be traced back to the design implementation phase, i.e. to the DfT circuitry generation followed with the automatic test pattern generation (ATPG) and the test assembly. The test assembly produces the test vectors in the so-called STIL (Standard Test Interface Language) format, which is the IEEE standard and can be read at any industrial tester platform. Only one module at the time can be selected for a test, whereas the DfT architecture provides an isolation of the selected module in the test mode with respect to its environment. The ATPG is calculated on the design after the layout generation, whereas the test patterns are subsequently simulated using the Verilog testbench together with the STIL test vectors at the top-level. This approach verifies the complete test setup and smoothen the debug process at the test floor itself.

The initial production test vector trial has been carried out using CERN Credence Sapphire platform. However, the production wafer-test itself had to be commissioned to the external company, because the tester platform at CERN does not have the wafer handler. The test house has carried out the wafer test on a similar tester (Credence Diamond) according to the test specification and protocol obtained from the FEI4 team. The following tests have been specified: continuity (contact) test, power supply test, scan-chain tests and IDDQ (quiescent current measurement) tests. In addition, the scan chain tests have also been carried out in different process corners, creating thereby a graph with the device operating range (Shmoo plot). Even though the test execution is up to the large extent automated due to the pre-verified standard STIL files, it was still necessary to perform the final tuning and pre-conditioning at the tester platform itself. This preconditioning concerns e.g. the power supply setup and the Shmoo plot generation, where the already mentioned test setup verification approach through the simulations played a crucial role.

The production testing with the external test house has been performed on a majority of FE-I4B wafers, which found a couple of faulty chips that escaped the functional tests performed at other sites, thereby justifying the decision to go for a production test. In addition, there is an on-going effort to try to use the test house facilities for the characterization of the blocks that cannot be tested at the FEI4 collaboration sites, such as LVDS and PLL.

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Session Classification: POSTERS