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Instrumentation of a Level-1 Track Trigger at ATLAS with Double Buffer Front-End Architecture

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The increased collision rate and pile-up produced at the HLLHC requires a substantial upgrade of the ATLAS level-1 trigger in order to maintain a broad physics reach. We show that tracking information can be used to control trigger rates, and describe a proposal for how this information can be extracted within a two-stage level-1 trigger design that has become the baseline for the HLLHC upgrade. We demonstrate that, in terms of the communication between the external processing and the tracking detector frontends, a hardware solution is possible that fits within the latency constraints of level-1.

Summary

The HLLHC, the planned high luminosity upgrade for the LHC, will increase the collision rate in the ATLAS detector by approximately a factor of 5 beyond the design, and increase the number of pile-up collisions in each event by a similar factor. The level-1 trigger must therefore achieve a higher rejection factor in a more difficult environment. The ATLAS upgrade for the HLLHC will include a complete replacement of the inner detector (tracking system). The current design is to have an all silicon tracker with a combination of pixel and silicon strip detectors. Recent studies using simulations of high luminosity collision events have shown that usage of tracking information early in the trigger decision enables the trigger rates to be kept low enough whilst not compromising the physics potential of the detector. One possible solution is to use a region of interest driven readout for triggering. The level-1 trigger would be split into two steps: level-0 and level-1. The level-0 would be based on the calorimeter and muon systems, and would reduce the rate from ˜40MHz to a few hundred kHz by defining regions of interest where a candidate particle has passed. The geometric location of these regions would define a subset of the tracking modules from which the data would be read out and used in a fast tracking algorithm for the level-1 decision. Over the past year, a clearer picture of the latency constraints on such a system have emerged. The primary focus will be on studies which demonstrate that a potential hardware solution has been identified for the communication between the external processing and the tracking detector frontends that fits within the tight latency constraints.

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