Contribution ID: **58** Type: **Poster**

New prototypes for components of a control system for the new ATLAS pixel detector at the HL-LHC

Thursday 20 September 2012 17:43 (1 minute)

In the years around 2020 an upgrade of the LHC to the HL-LHC is scheduled. In this upgrade, the inner detector of the ATLAS experiment will be replaced including the pixel detector. This new pixel detector requires a control system which complies with the strict requirements in terms of radiation hardness and material budget in ATLAS. The University of Wuppertal is developing a DCS (Detector Control System) network consisting of two kinds of ASICs: the DCS Chip and the DCS Controller. Both are manufactured in 130nm technology. We present results from measurements from new prototypes for the DCS network.

Summary

Together with the upgrade of the LHC to the HL-LHC the inner detector of the ATLAS experiment will be replaced. This includes a new pixel detector which requires a new detector control system (DCS) due to the increased radiation level and the larger number of read out channels. This control system is developed from scratch and will have to meet strict requirements for the electronics in ATLAS. The most important are: the lowest possible material budget and radiation tolerance for up to 570 MRAD in 10 years of operation. As one of the control systems tasks is to switch on and off serveral parts of the detector, a reliable protection against single event upsets (SEU) is very important. The concept of this DCS is split into three parts:
the safety path (hard wired interlock system), the control and feedback path (controlling the detector) and the diagnostics path (high granularity read out during calibration). We will concentrate on the control and feedback path, which consists of a star shaped network, the DCS network. This network is spanned by two types of ASICs: the DCS Chip which is located on the End-Of-Stave (EOS) cards at the end of each half stave of the pixel detector and the DCS Controller which is located in the outer regions of ATLAS. The DCS Chip is a mixed signal design, which contains analog circuitry to measure environmental conditions and digital circuitry to switch power of the pixel detector's modules and transmit data to the DCS Controller. The DCS Controller is a purely digital design and builds a bridge between the DCS Chip and the DCS computers in the counting room. For greater reliability of the network, the data between the two chips of the DCS network is transmitted differentially by a modified I2C bus.

In the last year two new chips were designed in 130nm technology. The first chip contains three types of voltage references which were tested for best applicability in the ADC of the DCS-Chip. This means it was tested for independence of temperature and supply voltage and manufacturing tolerance. The second chip is an improved version of the DCS-Controller which corrects teething problems of the first version. This chip was created in two versions, one with redundant registers (triple modular redundancy) for protection against SEU and one with normal registers to study the sensitivity of the chip's operation to SEU. Both Chips were exposed to radiation and tested for functionality afterwards. The new DCS-Controller was also operated and monitored during the irradiation. The outcomes of these functionality and radiation studies are presented.

Author: PÜLLEN, Lukas (Uni-Wuppertal)

Co-authors: ZEITNITZ, Christian (Bergische Universitaet Wuppertal (DE)); BOEK, Jennifer (Bergische Universitaet Wuppertal (DE)); KIND, Peter (Bergische Universitaet Wuppertal (DE)); MATTIG, Peter (Bergische Universitaet Wuppertal (DE)); KERSTEN, Susanne (Bergische Universitaet Wuppertal (DE))

Presenter: PÜLLEN, Lukas (Uni-Wuppertal)

Session Classification: POSTERS