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SPIROC: design and performance of a dedicated very front-end electronics for an ILC Hadronic CALimeter (HCAL) prototype with SiPM read-out

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The SPIROC chip is a dedicated very front-end electronics to read out a prototype of the Analog Hadronic Calorimeter (AHCAL) equipped with Silicon Photomultiplier (SiPM) for ILC (International Linear Collider). A first prototype of SPIROC has been fabricated in 2007 and a second version in 2010. Many testbench and testbeam measurements have been performed showing a good overall behaviour. However some limitations have been encountered. A new version has been submitted in February 2012 to correct them and to improve the ASIC performances. After an exhaustive description of the ASIC, the performances will be presented in this paper.

Summary

The SPIROC chip is a real System on Chip (SoC) that has been realized in the framework of CALICE collaboration and the European program EUDET to read-out the AHCAL calorimeter equipped with SiPM for ILC.
It is the first ASIC to readout SiPM detectors which are more and more used for numerous applications such as medical imaging, astrophysics, volcanology and nuclear physics.
SPIROC is the successor of the FLCSiPM chip designed in 2003 to equip a physics prototype of the AHCAL calorimeter.
One of the main constraints of this detector is to have a calorimeter as dense as possible. Therefore any space for infrastructure has to be minimized. One of the major requirements is consequently to minimize power to avoid active cooling in the detection gap. The power of the electronics located inside the detection gaps must be as low as 25 μW per channel (duty cycle 0.5%).
The ASIC is an auto-triggered, dual gain, 36-channel chip which measure on each channel the charge from 160 fC to 320 pC (from 1 to 2000 p.e. for a SiPM gain of 106) and the time with a precision of 1 ns.
The analog core is composed of 36 channels embedding an input DAC for SiPM high voltage adjustment on 5V to tune SiPM gain channel by channel.
Two preamplifiers allow the requested dynamic range and are followed by a trigger line made of a fast shaper and a discriminator.
The charge measurement line is made of two variable slow shapers and two 16-depth Switched Capacitor Arrays (SCA).
The time measurement is characterized by two different times'values: a time stamp performed by a 12-bit counter at a maximum frequency of 5MHz and a fine time obtained thanks to a TAC (Time to Amplitude Converter). The TAC signal is stored in the analog memory, in parallel with the charge.
A 12-bit Wilkinson ADC is used to digitize the analog charge and time values in digital data at the end of the acquisition period.
The digital part is very complex; it must handle the SCA write and read pointers, the ADC conversion, the data storage in a RAM and the readout process.
Different prototypes have been realized since the first version in 2007. A new version has been submitted in February 2012 to improve the ASIC performances.
Significant improvements have been implemented in the last version compared to the first ones such as:
-A new low noise preamplifier structure;
-A new input DAC with better channels uniformity ;
-A new TDC structure with less dead time.

This version will be the last one of the second generation of SPIROC ASIC, a third generation with a completely new architecture based on independent channels will be studied and designed next year.

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