Triggerless Readout Architecture for the Silicon Pixel Detector of the PANDA Experiment

Abstract : The readout architecture for the silicon pixel sensors of the PANDA MVD is presented. The pixel detector has to provide timing, position and energy information on a event-driven base, since no trigger signal is foreseen. The readout system is based on a custom ASIC, named ToPiX, directly connected to the GBT optical transceiver.

A reduced size prototype with most of the main functionality has been designed and tested. The ASIC has been bonded to a sensor based on the epitaxial technology and tested on a beam test. Both TID and SEU tests on the ToPiX prototype have been performed.

ToPiX v3



- \rightarrow Die size : 4.5 \times 4 mm²
- → Technology : CMOS 0.13 µm
- Single 1.2 V power supply
- Bump bonding pads
- \rightarrow 2 × 2 × 128 cells columns
- \rightarrow 2 × 2 × 32 cells columns
- → 32 cells EoC FIFO
- → SEU protected logic via TMR (pixel
- cell) or Hamming encoding (EoC)
- Serial data output
- → SLVS I/O

Readout system for tests



Based on Xilinx Virtex-6 ML605 Evaluation Kit

Remote control via TCP/IP. Up to 4 boards controlled in parallel by a single PC.

Limited number of external interconnections \rightarrow very flexible

Already used in a beam test at COSY (Jülich) and SPS (CERN)





