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Triggerless Readout Architecture for the Silicon Pixel Detector of the PANDA Experiment

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The readout architecture for the silicon pixel sensors of the PANDA MVD is presented.The pixel detector has to provide timing, position and energy information on a event-driven base, since no trigger signal is foreseen. The readout system is based on a custom ASIC, named ToPiX, directly connected to the GBT optical transceiver. A reduced size prototype with most of the main functionality has been designed and tested. The ASIC has been bonded to a sensor based on the epitaxial technology and tested on a beam test. Both TID and SEU tests on the ToPiX prototype have been performed.

Summary

The PANDA (antiProton ANnihilations at DArmstadt) experiment at the future FAIR facility currently under construction at Darmstadt, Germany, aims to the study of the antiproton-proton annihilation reactions. The detector layout is divided into a target section, positioned around the interaction point, and a forward section, positioned downstream.
The interaction point is defined by the intersection of the beam pipe, where the antiproton beam is circulated, and the target pipe, where the target (protons or ions) is injected.
The Micro Vertex Detector (MVD) is the innermost part of the detector and will consist of silicon pixel and strip sensors. The sensors are organized in a barrel section, with two pixel and two strip layers, and a forward section, with 6 disks with mixed pixel and strip sensors. A hybrid pixel solution was chosen as a baseline concept to accommodate the high radiation dose (up to 100 kGy) and the required time resolution. Pixel sensors based on an epitaxial layer grown a Czochralski substrate and then thinned have been chosen for their radiation resistance.
The pixel readout electronics has to provide space, energy and time measurements with a resolution of 100 um (in both directions), 200 e- and 6.4 ns, respectively, and an energy range corresponding to an injected charge up to 50 fC. The readout architecture will be event driven, since the system has to work trigger-less.
The readout architecture is based on a custom ASIC development, named ToPiX. ToPiX will consist of a matrix of 116x110 cells with a pixel size of 100x100 umˆ2, a column readout logic and 320 Mb/s serializers for data transmission. A CMOS 130 nm technology has been used to reduce the size of the circuitry and to provide tolerance to radiation effects related to the Total Ionizing Dose (TID). ToPiX will be designed to be directly connected to the GBT radiation tolerant optical transceiver under development at CERN.
A prototype of the ToPiX ASIC, with 640 pixels divided into two 2x128 cells and two 2x32 cells double columns has been designed and tested. The prototype includes also the end of column FIFO and control logic and a 160 Mb/s serializer. Triple Modular Redundancy (TMR) has been used to protect the pixel cell control logic from Single Event Upset (SEU), while the end of column FIFO and the control logic is based on a Hamming encoding. A new version of the prototype, with the same number of cell and the e-link interface at 320 Mb/s is currently under design.
Four epitaxial silicon pixel sensors produced by FBK, Trento have been bump bonded to the ToPiX prototypes by IZM, Berlin. The four modules have then been tested on a beam test at the COSY facility at the Forschungszentrum Juelich with a 2.7 Gev/c proton beam. Both TID and SEU irradiation tests have been performed on the ToPiX prototype at thecX-ray facility of the CERN PH-ESE and at the Tandem facility of the INFN LNL.

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