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Front End ASIC design for SiPM Readout

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A Front End ASIC for the readout of Silicon Photo-Multipliers is presented with the following features:
wide dynamic range, high speed, multi channel, low input impedance current preamplifier, low power (7mW per channel), DC coupled input with common mode voltage control and separated timing and charge signal output.
A detailed description of the SiPM modeling and parameter extraction is also included allowing the emulation of the signal generated by different commercial devices in the design simulation stage.
This prototype includes basic blocks for 3 channels with: preamplifier with two separate signal paths and fast current discriminator with digital output.

Summary

Silicon Photo-Multipliers (SiPM) are recently developed electronic devices with photon counting capabilities improving current state of the art detectors regarding high voltage requirements, signal gain and magnetic field insensitivity, while keeping at the same time excellent timing characteristics and
wide dynamic range. SiPM are semiconductor devices still under development by some manufacturers in order to improve yield, to provide multi-channel architectures and to increase light sensitivity spectrum.
Immunity to magnetic field and compact form factor make SiPM an ideal choice for their usage in particle detectors
(specially for calorimeters and Scintillating Fibre Trackers) and also medical applications such as PET (Positron Emission Tomography) scanners when used with an optically coupled scintillating material able to provide the conversion between high energy particles to light pulses.
A Front End Readout ASIC for Silicon Photo-Multipliers is presented with the following features: wide dynamic range, high speed (around 400MHz bandwidth), multi channel, low input impedance current preamplifier, low power (7.3mW per channel), SiPM voltage control and timing and charge signal outputs. Special stress in a detailed description on the SiPM modeling and parameter extraction to be used in the design stage is also included. This model makes possible the emulation of the signal generated by different commercial devices in the design stage using SPICE simulations. The parameters needed by the model are simple enough to be measured directly on the devices with standard equipment. This basic building blocks prototype includes 3 channels with: preamplifier with two signal paths (one high gain, high speed timing path and a lower speed, lower gain energy measurement path) and fast current discriminator with digital output.
The preamplifier stage includes a novel circuitry with saturation control that permits to be operational on the two signal paths (timing and charge) even when the high gain is completely saturated. This circuitry permits the correct operation of the measurement outputs in a wide input dynamic range.
The prototype was submitted on June 2011 and manufactured by AustriaMicrosystems 0.35 microns technology.
The summary of the tests results is also included with their comparison to the simulations performed using the sensor model extracted from commercial devices.
This work is presented as the first stage in the design of a multichannel highly integrated generic front-end ASIC including digital output and control.

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