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# Research of long distance clock distribution system

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The ARA project requires precision clock synchronization in electronic waveform capture circuits deployed in separate 200 m boreholes at the South Pole. Simultaneously digitized data must be transferred to trigger and readout electronics at the surface. We have tested two methods of embedding the clock distribution and recovery into the communications system: one using 4 LVDS pairs in CAT5 cable to transfer a 10MHz clock and 80Mbps data separately, the other using optical fiber to transfer 1.25 Gbps data and a 125MHz clock. Skew jitter between original and received clocks is less than 50 ps in both systems.

## Summary

The Askaryan Radio Array (ARA) is a new detector to be deployed in the ice at the South Pole designed to detect ultrahigh energy neutrinos (E > 100 PeV) by means of radiofrequency emission from electro-magnetic cascades formed when these neutrinos interact with nuclei in the ice. The completed array will contain 37 stations that cover 160 km2 surface area. Each station consists of 4, 15 cm diameter boreholes spaced up to 70 m apart and 200 m deep. The 2 VPOL and 2 HPOL antennas in each hole operate between 100 MHz and 1 GHz near the thermal noise floor to pick up the weak RF emission. Signals from a station are combined to trigger a full waveform readout from all 16 antennas later used to identify neutrino events from thermal and anthropogenic noise and reconstruct possible neutrino events for energy and direction. A custom designed ASIC digitizes the waveforms in excess of 3 GSPS. In doing so and in order to perform event reconstruction, it requires synchronized clocks for all channels within a station: clocks in each hole need exactly the same frequency and must maintain a fixed phase difference amongst each other, a jitter less than 50 ps being acceptable.

There are two options for signal transport out of the antenna holes to the station surface trigger and data acquisition computer. One is to transfer the RF signal from each antenna to a surface process board through individual analog optical fibers, the other option is to distribute a master clock from surface to each hole and transfer the digital signal to the surface after A/D conversion in the hole. The latter solution has substantial advantages in cost and power which drives our development effort to realize this technology.

Last year we implemented a first version of a long distance clock synchronization system by using 4 LVDS pairs in CAT5 cable to transfer a 10MHz clock and 80Mbps data separately over cable lengths as long as 250 meters with the help of cable driver and clock recover chip pairs. Additionally, this year we have updated our solution to optical fiber: by using GTP blocks (Gigabit Transceiver) in Spartan 6 FPGAs, a master clock on the surface data acquisition card can be embedded into the data stream and distributed to the various holes. In each hole, a clock of identical frequency can be recovered from the received data by action of the embedded CDR circuit. In this way, we have implemented a 1.25 Gbps data link and a 125MHz clock over a bidirectional communication system fulfilling the requirements of ARA. Furthermore, by using a wavelength-division multiplexing transceiver, this system can run over a single optical fiber which can decrease the cost and deployment complexity of stations.

The note describes our efforts on the latter solution: technical details as well as methods of maintaining fixed phase difference between two clocks after power cycle and reset.

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