

# BPM for TBL: status of the amplifier

Gabriel Montoro\*, Antoni Gelonch, Yuri Kubyshin  
Universitat Politècnica de Catalunya (UPC)

\*E-mail: [montoro@tsc.upc.edu](mailto:montoro@tsc.upc.edu)



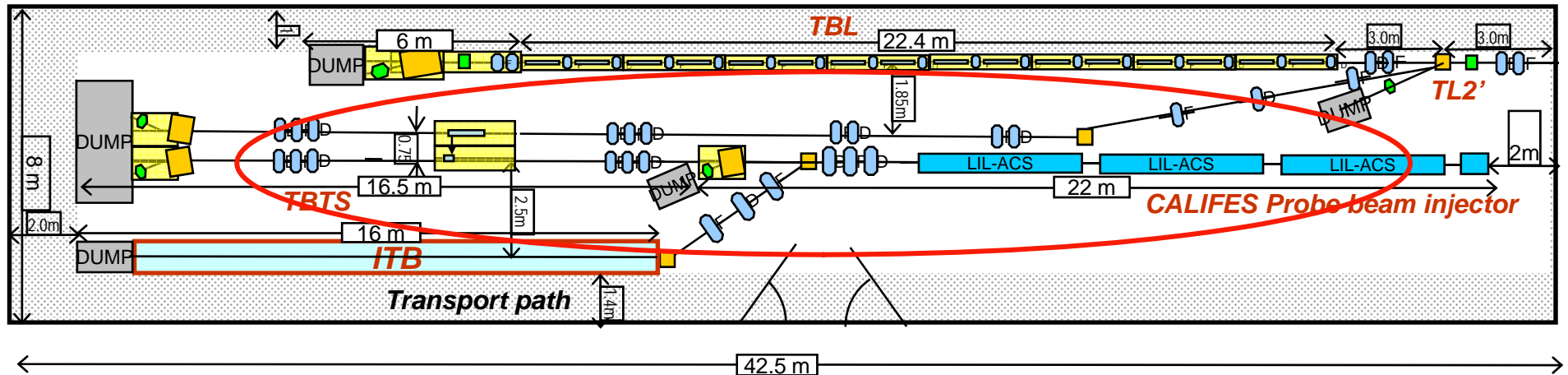
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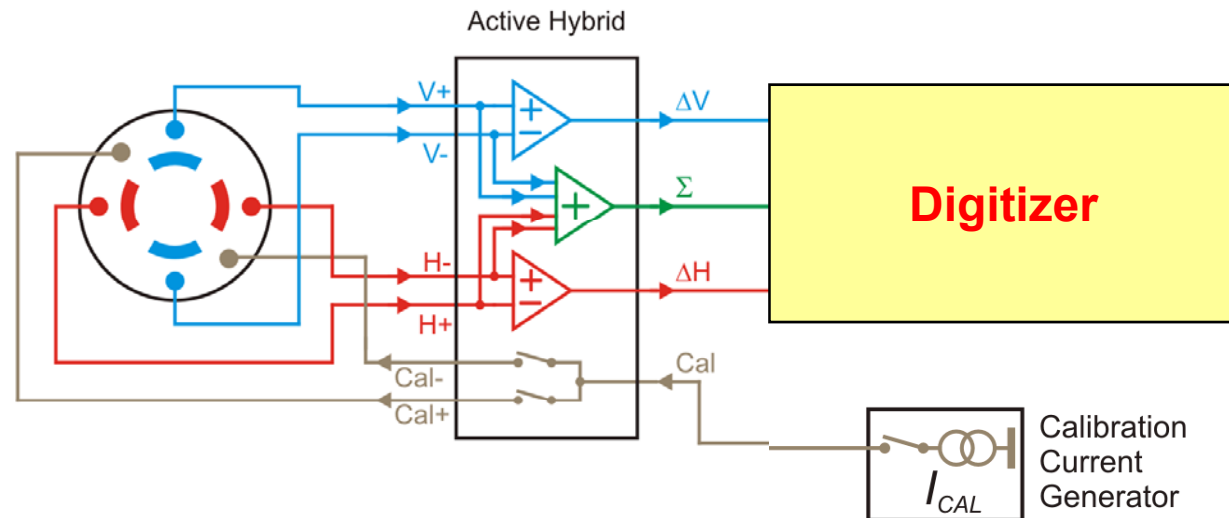
# BPM Amplifier for Test Beam Line



- The signals ( $V+$ ,  $V-$ ,  $H+$  and  $H-$ ) sensed by the IPU must be processed in order to obtain the signals difference and sum before being digitized
- It must work as a digitizer front-end



# General scheme of the analog head electronics



Previous design by M. Gasior

<b>Tentative parameters of the BPMs for the TBL</b>	
BPM analog bandwidth (BPM with associated electronics)	10 kHz -100 MHz <b>(200 MHz is highly desirable)</b>
Beam position range of interest	+/-5 mm horizontal and vertical
Beam aperture diameter	22.5 mm
Overall mechanical length	< 100 mm
Number of BPM's in TBL	18
Resolution at maximum current	<5 $\mu\text{m}$
Overall precision	<50 $\mu\text{m}$
Typical radiation levels	<1000 Gray/year

**The BPM design for the DBL by M. Gasior cannot be applied directly. Modifications are required:**

- a) **The dimensions of the IPU should be reduced (by a factor of 0.6 approximately)**
- b) **The amplifier bandwidth should be increased (desired up to 200 MHz)**



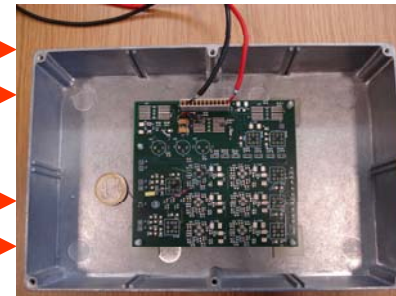
## Inductive pick-up



H

V

## Analog front-end electronics



$\Delta H$

$\Delta V$

$\Sigma$

- Mechanics
- IPU electronics

- Amplifier



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# Analog amplifier of the BPM for the TBL

Work done:

1. Specifications of the interface between the analog amplifier and the digitizer (Lapp) defined
2. Design an schematics of the amplifier
3. CAD design of the PCB
4. Manufacturing of PCB
5. Partial building and test of PCB



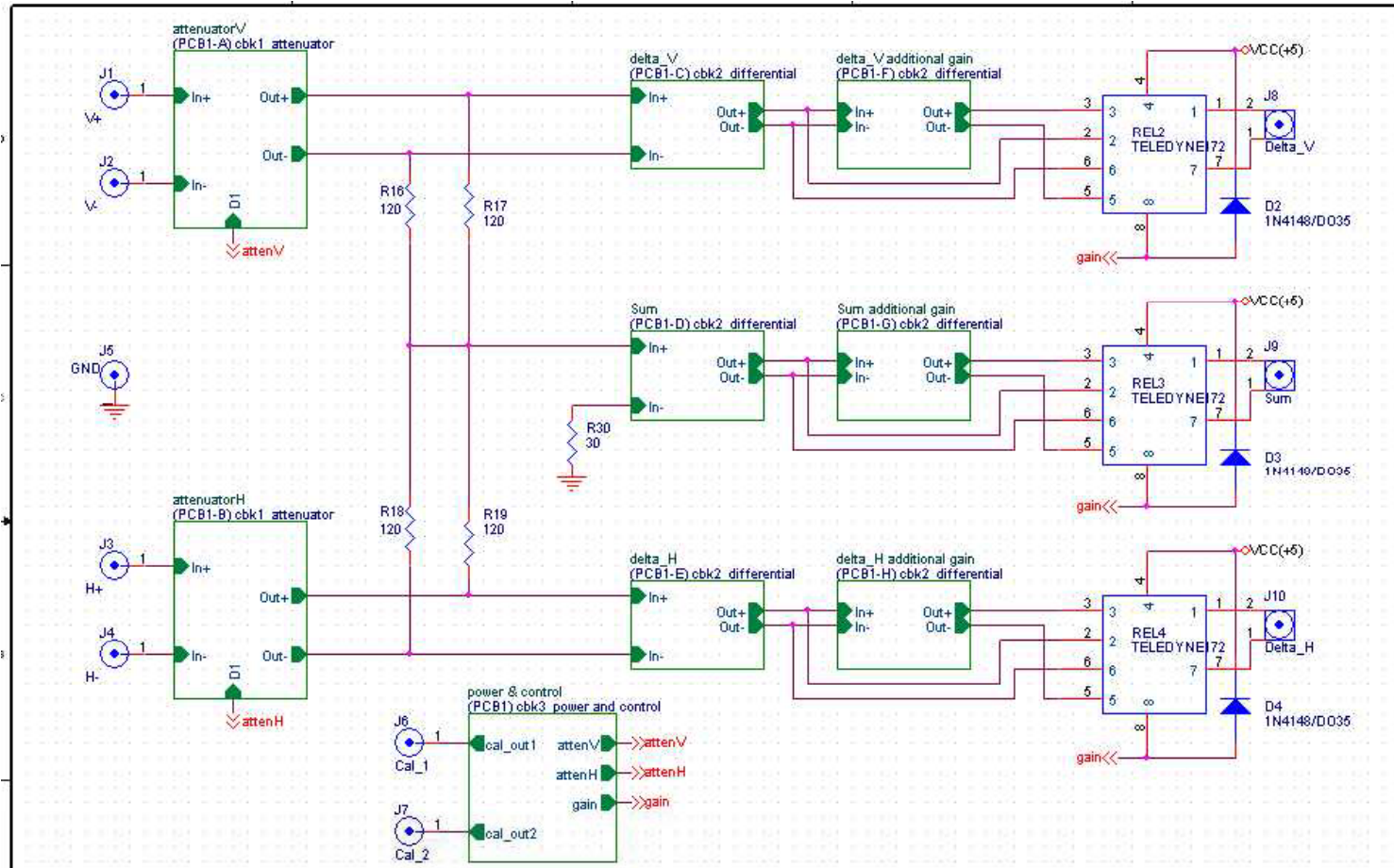
# Specifications of the interface between the analog amplifier and the digitizer

The following information was obtained from the Lapp group:

- The analog outputs are bipolar
- Levels:  $\pm 2V$  max.
- The power and control connector pinout has been determined
- The signal output consist in 3 double (balanced) signals: 1 sum and 2 differences



# Schematics done according to the previous specifications





WIDEBAND, LOW NOISE, LOW DISTORTION FULLY DIFFERENTIAL AMPLIFIER

FEATURES

- Fully Differential Architecture
- Common-Mode Input Range Includes the Negative Rail
- Minimum Gain of 2 V/V (6 dB)
- Bandwidth: 2 GHz
- Slew Rate: 6400 V/ $\mu$ s
- 1% Settling Time: 2 ns
- HD<sub>2</sub>: -72 dBc at 100 MHz
- HD<sub>3</sub>: -79 dBc at 100 MHz
- OIP<sub>2</sub>: 78 dBm at 70 MHz
- OIP<sub>3</sub>: 42 dBm at 70 MHz
- Input Voltage Noise: 2.3 nV/ $\sqrt$ Hz (f > 10 MHz)
- Noise Figure: 19.2 dB (G = 10 dB)
- Output Common-Mode Control
- 5-V Power Supply Current: 39.2 mA
- Power-Down Capability: 0.65 mA

APPLICATIONS

- 5-V Data-Acquisition Systems
- High Linearity ADC Amplifier
- Wireless Communication
- Medical Imaging
- Test and Measurement

DESCRIPTION

The THS4508 is a wideband, fully-differential operational amplifier designed for single-supply 5-V data-acquisition systems. It has very low noise at 2.3 nV/ $\sqrt$ Hz, and extremely low harmonic distortion of -72 dBc HD<sub>2</sub> and -79 dBc HD<sub>3</sub> at 100 MHz with 2 V<sub>pp</sub>, G = 10 dB, and 1-k $\Omega$  load. Slew rate is very high at 6400 V/ $\mu$ s and with settling time of 2 ns to 1% (2 V step) it is ideal for pulsed applications. It is designed for minimum gain of 6 dB, but is optimized for gain of 10 dB.

To allow for dc coupling to ADCs, its unique output common-mode control circuit maintains the output common-mode voltage within 5-mV offset (typical) from the set voltage, when set within 0.5 V of mid-supply. The common-mode set point is set to mid-supply by internal circuitry, which may be over-driven from an external source.

The THS4508 is a high-performance amplifier that has been optimized for use in high performance, 5-V single supply data acquisition systems. The output has been optimized for best performance with its common-mode voltages set to mid supply, and the input has been optimized for best performance with its common-mode voltage set to 0.7 V. High performance at a low power-supply voltage makes for high-performance single-supply 5-V data-acquisition systems with a minimum parts count. The combined performance of the THS4508 in a gain of 10-dB driving the ADSS500 ADC, sampling at 125 MSPS, is 82-dBc SFDR, and 68.3-dBc SNR with a -1-dBFS signal at 70 MHz.

The THS4508 is offered in a Quad 16-pin leadless QFN package (RGT), and is characterized for operation over the full industrial temperature range from -40°C to 85°C.

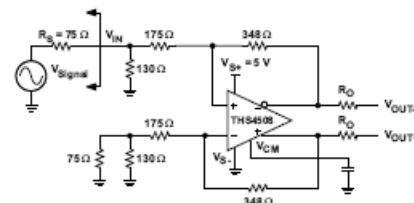
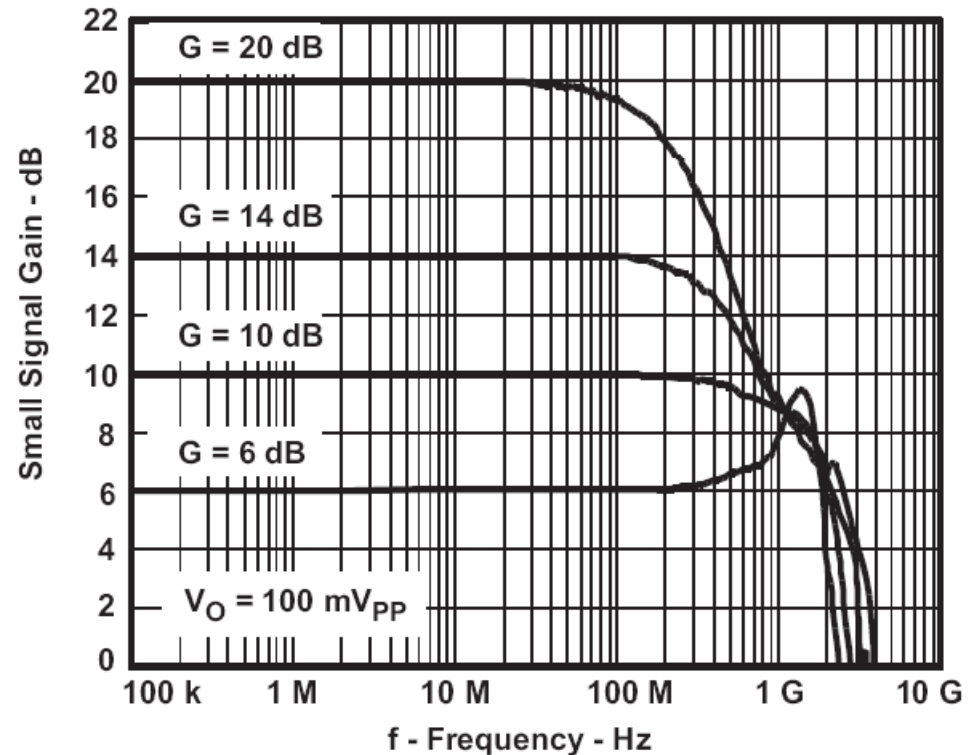
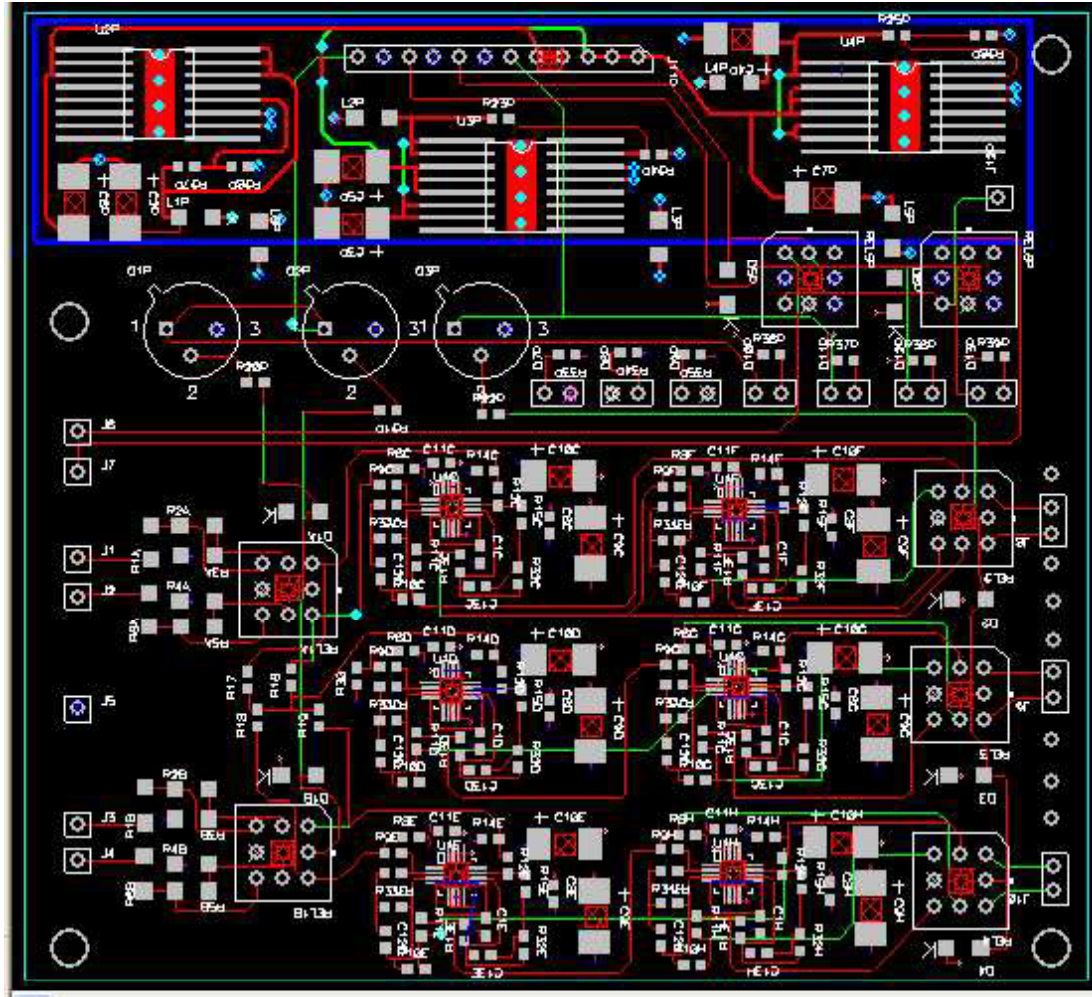


Figure 1. Video Buffer

SMALL-SIGNAL FREQUENCY RESPONSE



# The CAD design of the PCB has been also finished

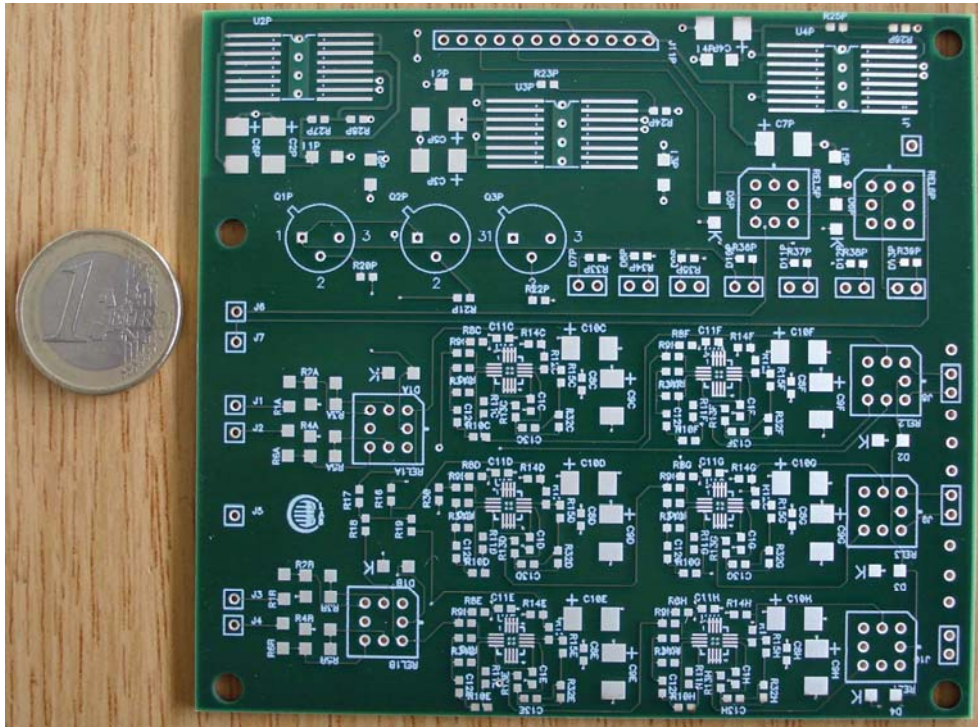


# The Bill Of Materials (BOM)

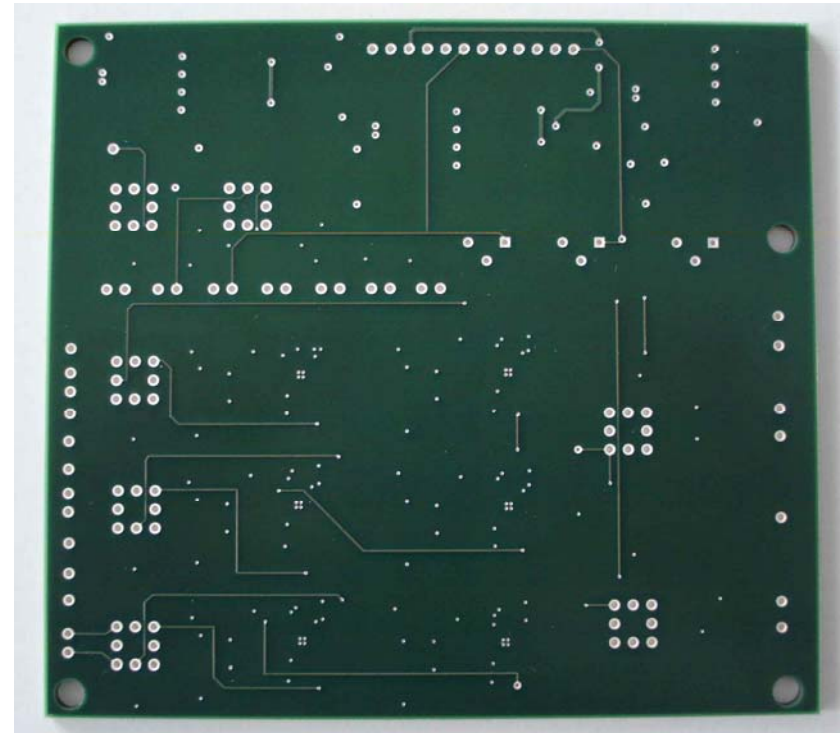
Item	Quantity	Reference	Part	Footprint	Manufacturer	Distributor	Price
1	18	C1H,C1G,C1F,C1E,C1D,C1C,C8H,C8G,C8F,C8E,C8D,C8C,C11H,C11G,C11F,C11E,C11D,C11C				100n	SMD0603
2	6	C2P,C3P,C4P,C5P,C6P,C7P	22u	EIA-6032-28			
3	12	C9H,C9G,C9F,C9E,C9D,C9C,C10H,C10G,C10F,C10E,C10D,C10C	1u	EIA-6032-28			
4	12	C12H,C12G,C12F,C12E,C12D,C12C,C13H,C13G,C13F,C13E,C13D,C13C	CAP-NP/0603			SMD0603	
5	7	D1B,D1A,D2,D3,D4,D5P,D6P	1N4148/DO35	DO35			
6	7	D7P,D8P,D9P,D10P,D11P,D12P,D13P	LEDPCB2/PIN	2PIN			
7	1	J1	V+	1PIN			
8	1	J2	V-	1PIN			
9	1	J3	H+	1PIN			
10	1	J4	H-	1PIN			
11	1	J5	GND	1PIN			
12	1	J6	Cal_1	1PIN			
13	1	J7	Cal_2	1PIN			
14	1	J8	Delta_V	2PIN			
15	1	J9	Sum	2PIN			
16	1	J10	Delta_H	2PIN			
17	1	J11P	CONPCB12/PIN	12PIN_100MIL			
18	1	J12P	CALIN	1PIN			
19	6	L1P,L2P,L3P,L4P,L5P,L6P	EMI_IND	SMD1206			
20	3	Q1P,Q2P,Q3P	IRHLF770Z4/TO39	TO39			
21	7	REL1B,REL1A,REL2,REL3,REL4,REL5P,REL6P	TELEDYNE172	TELEDYNE172			
22	12	R1B,R1A,R2B,R2A,R3B,R3A,R4B,R4A,R5B,R5A,R6B,R6A	R/1206	SMD1206			
23	12	R7H,R7G,R7F,R7E,R7D,R7C,R15H,R15G,R15F,R15E,R15D,R15C	348	SMD0603			
24	12	R8H,R8G,R8F,R8E,R8D,R8C,R14H,R14G,R14F,R14E,R14D,R14C	287	SMD0603			
25	12	R9H,R9G,R9F,R9E,R9D,R9C,R12H,R12G,R12F,R12E,R12D,R12C	16.5	SMD0603			
26	12	R10H,R10G,R10F,R10E,R10D,R10C,R13H,R13G,R13F,R13E,R13D,R13C	50	SMD0603			
27	6	R11H,R11G,R11F,R11E,R11D,R11C	100	SMD0603			
28	4	R16,R17,R18,R19	120	SMD0603			
29	21	R20P,R21P,R22P,R23P,R24P,R25P,R26P,R27P,R28P,R31H,R31G,R31F,R31E,R31D,R31C,R32H,R32G,R32F,R32E,R32D,R32C					
30	1	R30	30	SMD0603			
31	7	R33P,R34P,R35P,R36P,R37P,R38P,R39P	1K	SMD0603			
32	6	U1H,U1G,U1F,U1E,U1D,U1C	THS4508	QFN16	TI	TI	6
33	1	U2P	RHFL7913A	FLAT16			
34	2	U3P,U4P	RHFL4913	FLAT16			



# The 6-layers manufactured PCB



TOP



BOTTOM

# The most critical components

- Rad-hard wideband amplifier: THS4508 (manufactured by TI)

Status:

We have received 12 samples from AVNET-SILICA (a TI distributor)



# The most critical components

- RHFL4913 (positive regulator)
- RHFL7913A (negative regulator)
- STRH8N10STF3 (FET transistor)

Status:

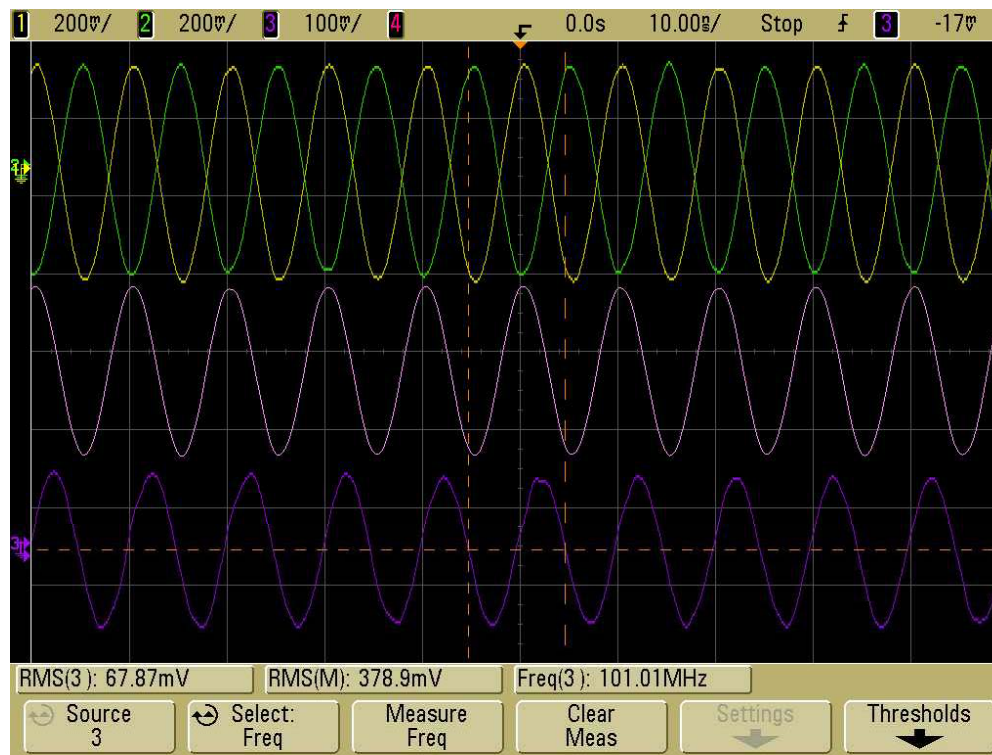
- All these components are manufactured by ST
- It is not possible to obtain them by conventional distributors. We expect that the RHFL4913 and the RHFL7913A can be obtained with the help of CERN: these regulators are considered to be used in the ATLAS experiment





# Testing one channel

- Adjusted to have a gain of: 10
- Adjusted to have an input impedance of: 50 ohms
- Measured bandwidth: 80 MHz (It must be improved !!!)





## Future work to be done

1. To finish the board assembly
2. To test the amplifier in the UPC lab.
3. To start testing it at CERN (together with the mechanical part - IPU)

After this: It is possible that after tests at the UPC and CERN some rework or further adjustments of the amplifier can be necessary

