CLIC TRACKING WITH TIME STAMP READOUT

The challenge of CLIC tracking, due to superimposed vertices, is to associate the excellent position resolution and granularity of the pixel detectors with 100 ps precise time resolution and time-stamp readout capability in order to allow bunch identification of hits/tracks.

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OUTLINE

- **Vertex and bunch identification**
  - **Time stamp**
    - Time stamp pixel concept for CLIC
    - NA62 Gigatracker
- Topics of R&D
  - Ultrafast silicon sensor
  - Fast electronics with time stamp readout
  - Optimization, power, sensor, readout architecture
  - Not discussed here:
    - packaging, cooling, mass, construction, etc…
- **Conclusions**
  - R&D proposal of a time stamp pixel demonstrator
    - Description of the demonstrator work package in preparation

CLIC versus LHC and ILC

	LHC ATLAS VX	ILC	CLIC	NA62 [1)]
BX spacing [ns]	25	300	**0.667**	avg 1ns
Nb of BX/train	2808	2820	**311**	$2*10^9$
Bunch train length	70µs	1ms	**207 ns**	2 s
Repetition rate [Hz]	40M	5	50	0.07
Nb of Bunch/s	36M	11400	15550	10^9
Hit/mm^2/Bunch max	0.05	0.05	**0.1-1[2)]**	$6*10^{-4}$
Radiation level fluence	**~10^{15}/10 y**	**~10^{13}**	**~10^{14}**	**~$2\cdot10^{14}$/y**

1) bx = particles; train = spill
2) Daniel's talk: background pairs and muons at r=3 cm @ 5T and r=1 cm @ 3T

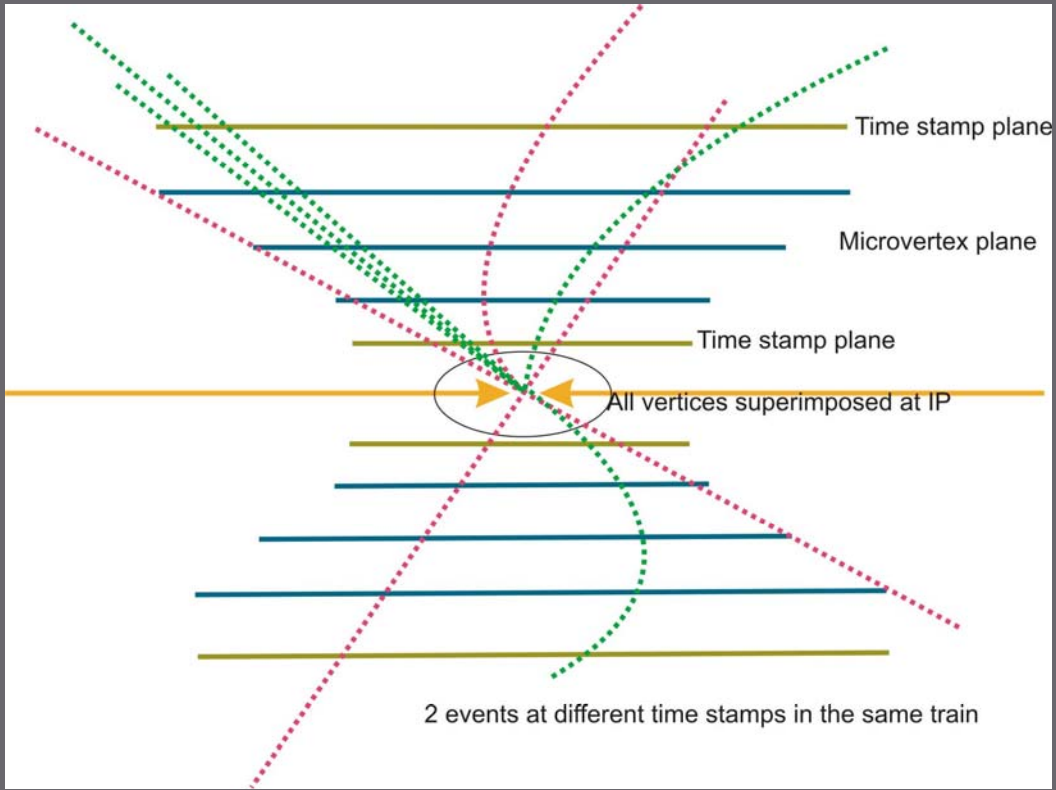
Material budgets of various experiments

Experiments	% X_0
CLIC	0.1 ?
NA62	0.5
ILC	0.1 ?
LHC - ATLAS pixel	~2-3
LHC - ALICE pixels	~1

Timing Issue at CLIC

- Time tagging of vertices
  - 331 BX's piled up in detector/electronics
- Issue of track reconstruction ambiguities
  - No longitudinal spread of BX interactions
    - Precise vertex IP space point
  - Bunch identification by time stamp
    - 10 µm longitudinal spread
    - If precision vertex senses 200 ns train
      - Disentangle vertices
    - Ideal time stamp precision
      - 1/6 of bunch separation 667ps
        - 100 ps rms
    - 331 frames/train
    - Questions
      - How precisely can we associate a time stamp with a track/event?
      - What is the total background?
      - What is the background rejection?

2 vertices in 2 different Bx's in one train



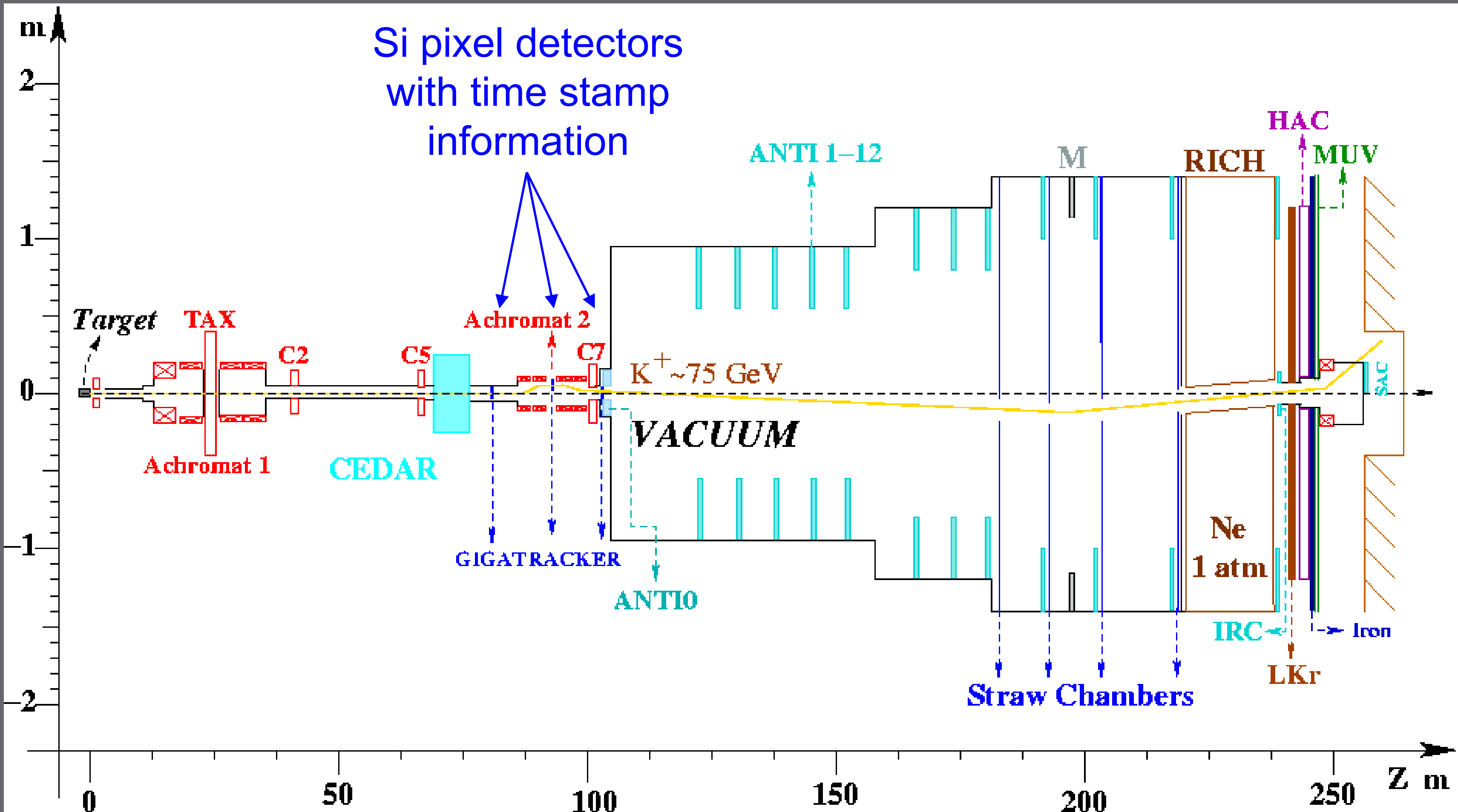
Time stamp of CLIC vertex

- **Basic concept**
  - A vertex detector complemented by one or 2 time stamp barrels
    - Why?
      - Hybrid pixel for time precision measurement
        - Coarse pixel segmentation
        - Too much functionality and power for 20-50µm pixel segmentation
        - Too much power consumption(ILC), CCD or analog integrating readout
      - Monolithic sensor pixel in integration mode
        - Space precision measurement
        - Cannot afford ultra fast processing in each pixel
        - Integrate signal over 200 ns train
        - No bunch identification
      - Estimate of the pixel multiplicity for jet's with time stamp barrel
        - Measurement of pixel signal amplitude
- **Goals**
  - Bunch identification
      - Associate hits/tracks of each train with bunch number (1 to 311)
    - Pixel multiplicity
      - Multiplicity estimate, important if one of the inner most layer is a TS pixel plane
    - Background rejection
      - Rejection based on time stamp identification of events
        - highly collimated hadronic jets.
        - Rejection of coherent pairs → hadrons events overlapping e+e- interaction

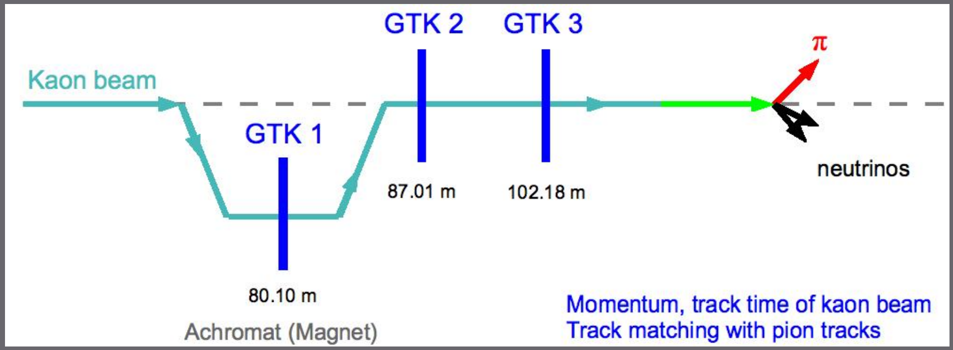
Layout of NA62

Proposed experiment to measure rare kaon decays at the CERN SPS:

$K^+ \Rightarrow \pi^+ \nu\nu$



Gigatracker Purpose



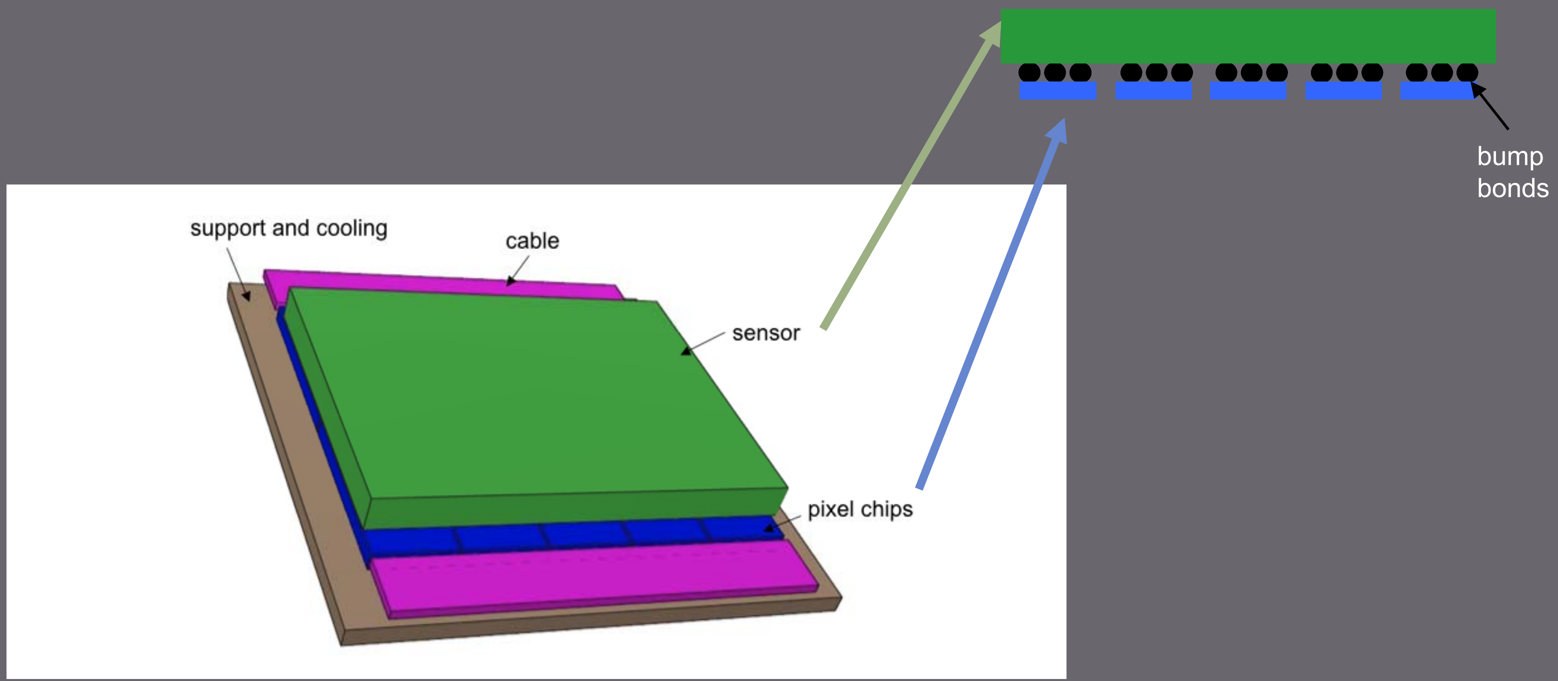
- **Momentum measurement** ($\Delta p/p$ ~0.5%)
- **Precise time information** to make a tight kaon-pion time

Specifications:

- Track up to 10^9 particles per second
- Time resolution per track of ~140 ps (~200 ps per station)
- Spatial resolution ~100 µm, Angular resolution ~10 µrad
- Minimum material budget (< 0.5 % X_0 per station)
- Operated in vacuum and in a high radiation environment

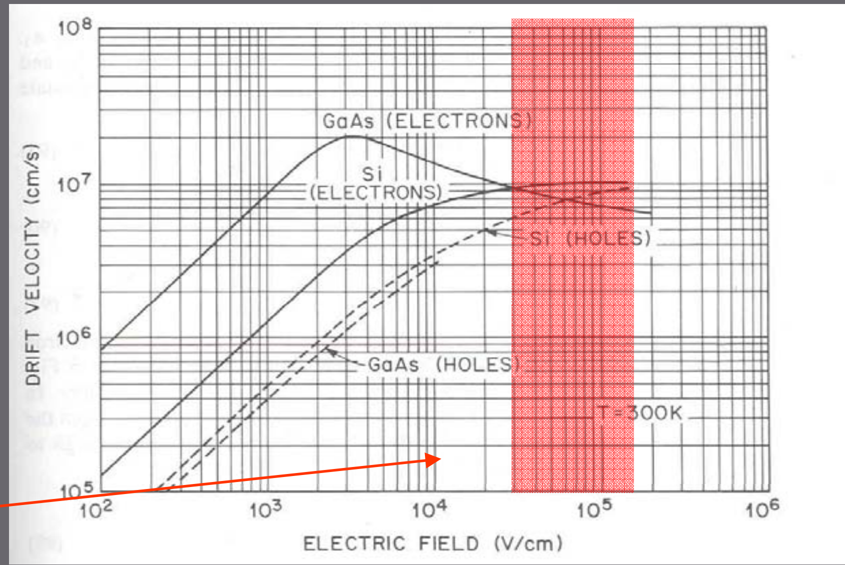
NA62 GTK module layout

- Current proposal
  - Each of the 3 stations will consist of one silicon pixel sensor connected to 10 readout chips:

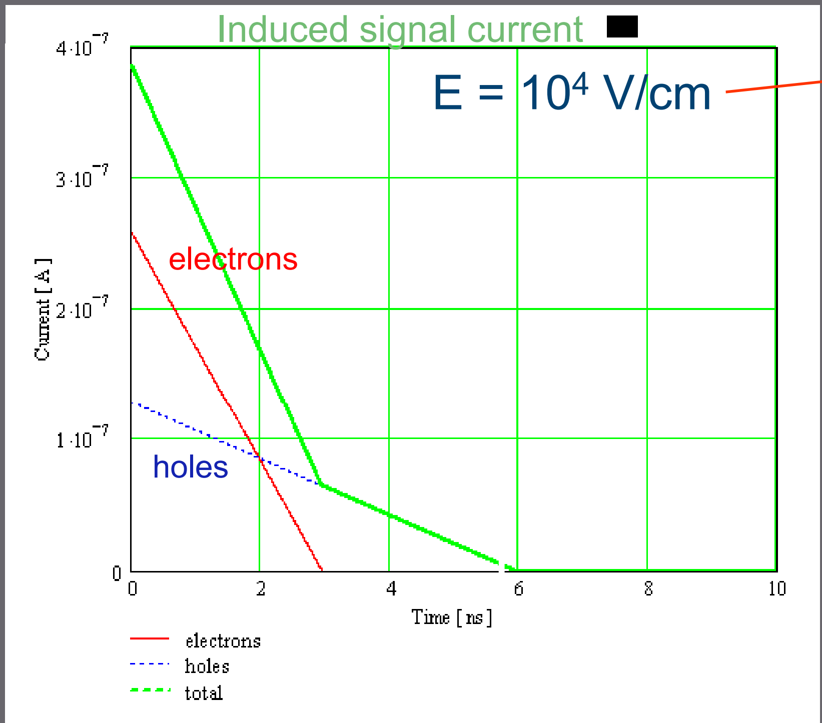


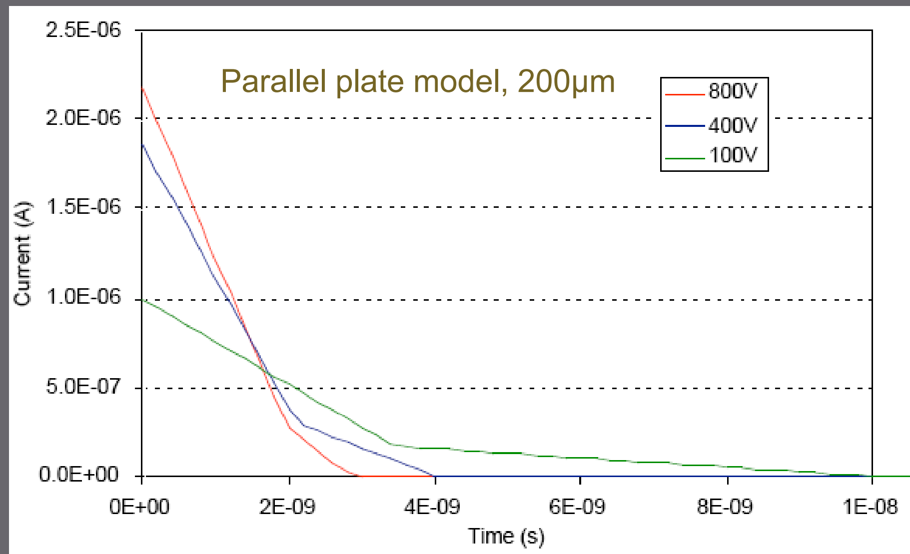
Ultimate speed of silicon sensor

- Charge drift time depends on electric field
- Slow signal component (holes) saturates around 10^5 V/cm
- High over-depletion required to reduce overall collection time and to provide high timing precision



From Sze, Semiconductor Devices 1985





Simulation C. Piemonte ITC-IRST

130 nino circuits

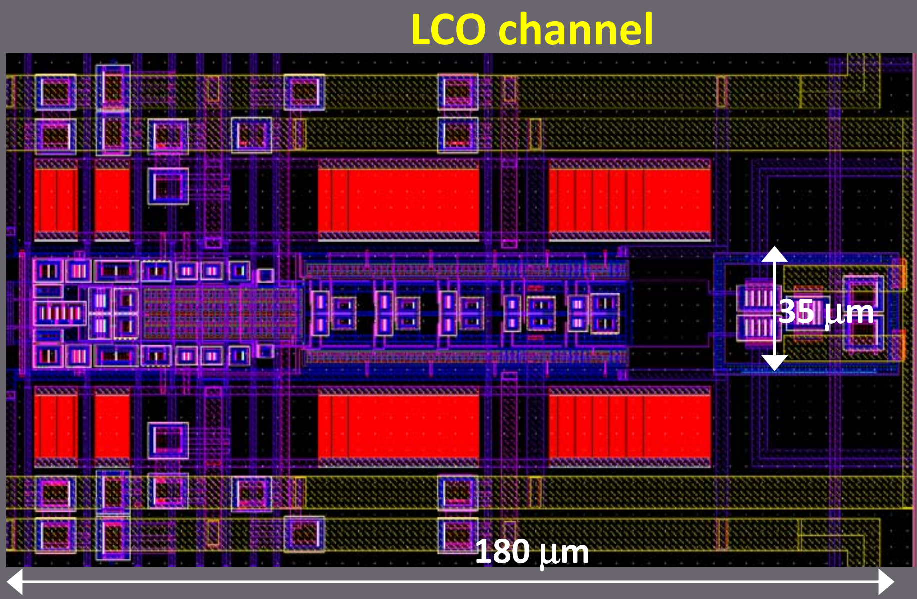
- **2 versions of NINO architecture implemented in 0.13 µm CMOS technology**

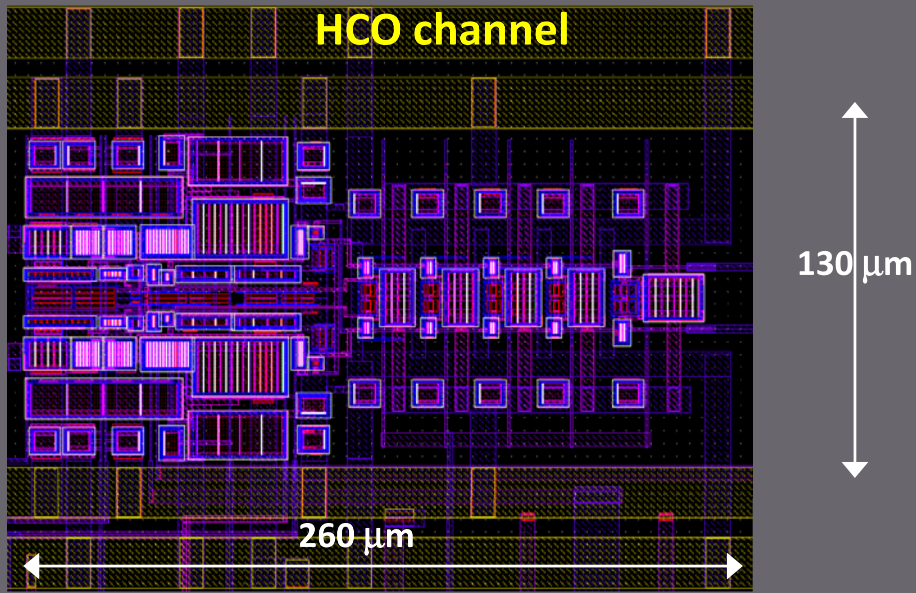
LCO version (for Cin ~ 200 fF)

- Noise < 1000 e- rms
- Rising time < 500 ps rms
- Power consumption : 300 µW
- Tunable threshold (0 to 4 fC)
- Differential output

HCO version (for Cin ~ 10 pF)

- Noise < 4000 e- rms
- Rising time < 200 ps rms
- Power consumption : 3 mW
- Tunable threshold (0 to 20 fC)
- Differential output



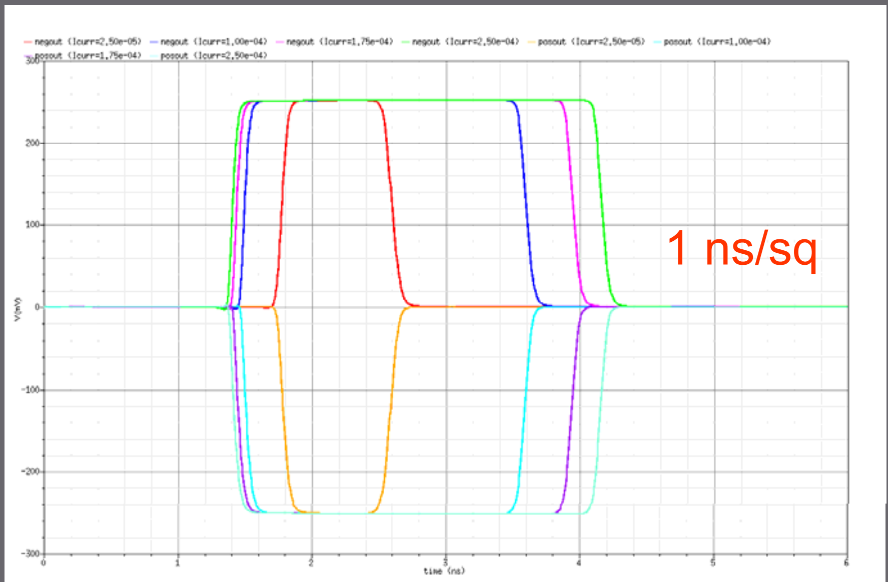


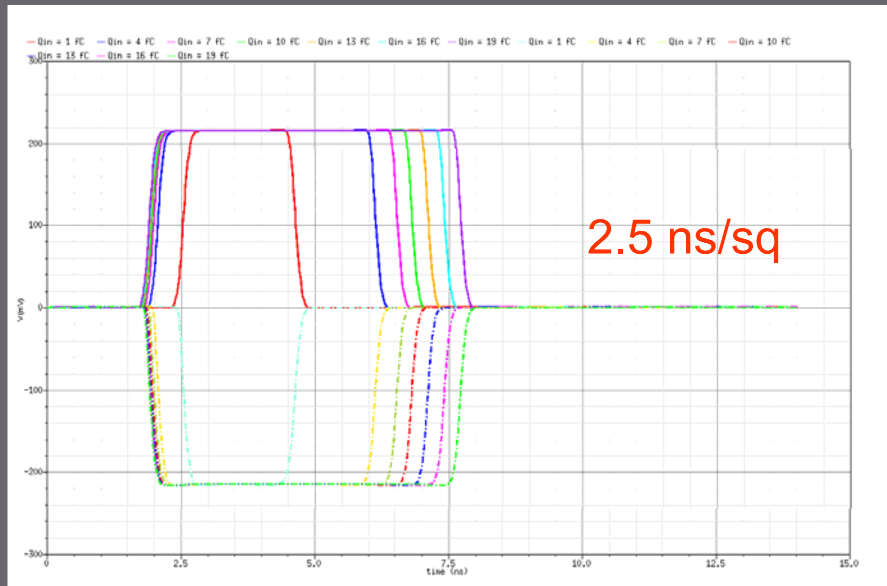
QTC Front end circuit response

- 10pF circuit
  - Power 3 mW

0.2 pF circuit

power 0.3 mW



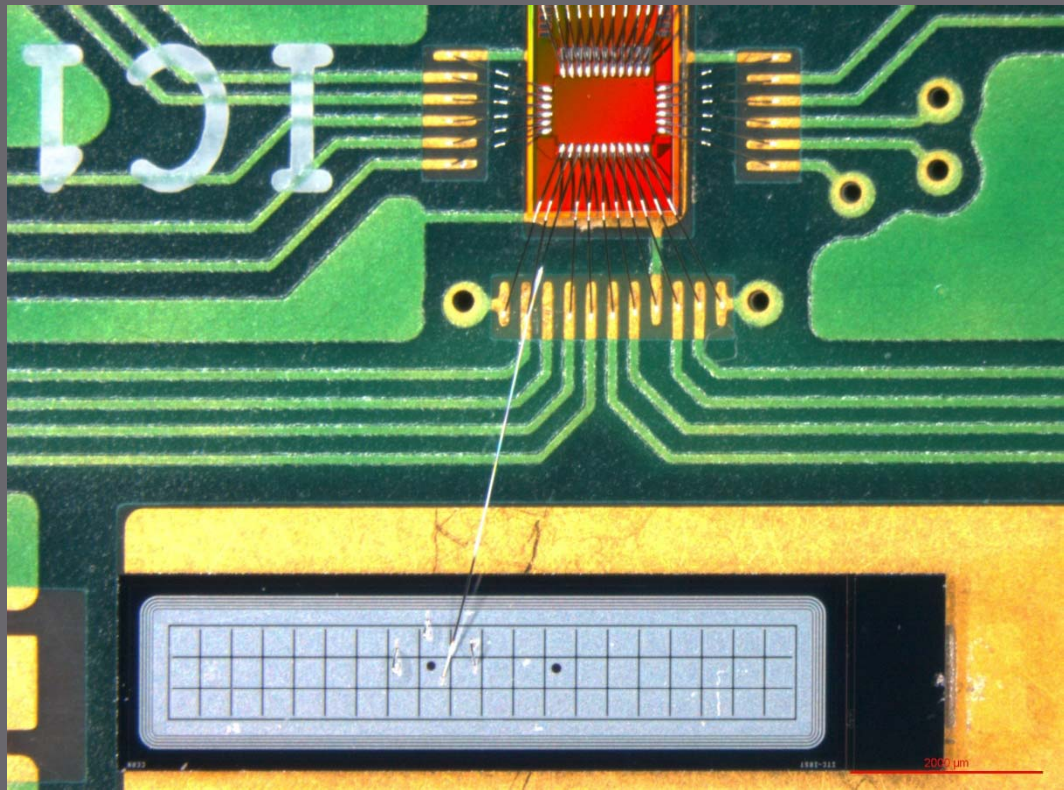


HCO output for Qin from 10 fC to 100 fC **Output signal for Qin from 1 fC to 19 fC**

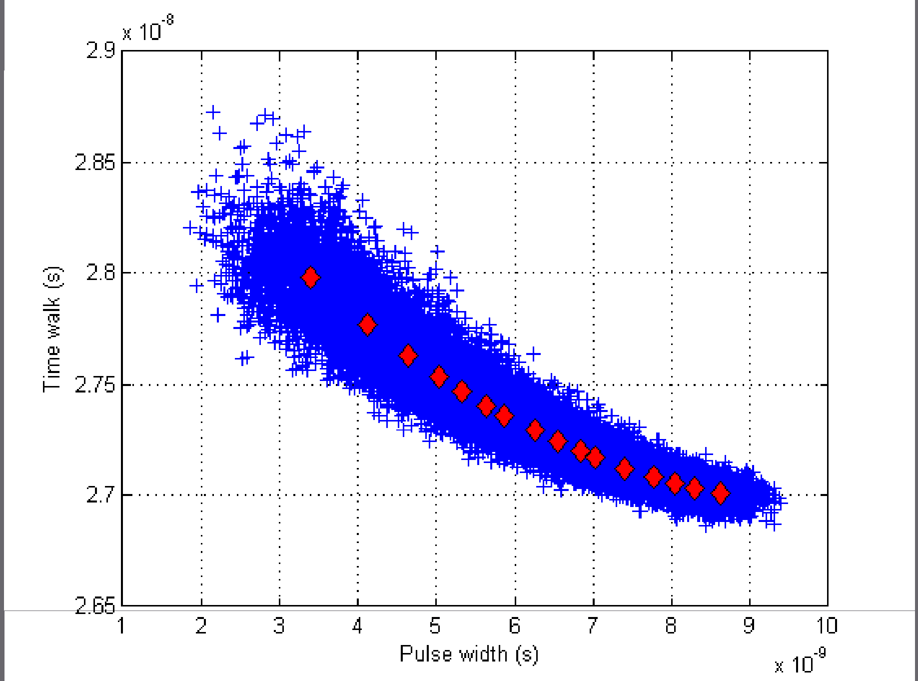
Pulse width proportional to input charge, capability to readout pixel multiplicity

Experimental results

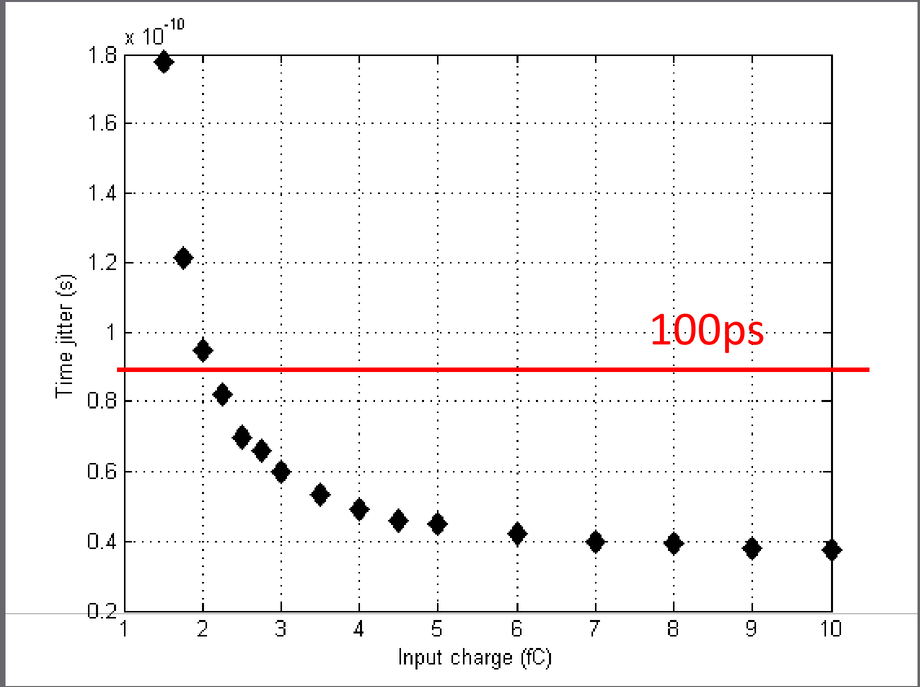
- NINO LCO 130 nm with 300x300µm pixel detector
  - Test done with a pulsed laser



NINO Electronic Jitter < 40 ps



Scatter plot of time walk versus pulse width

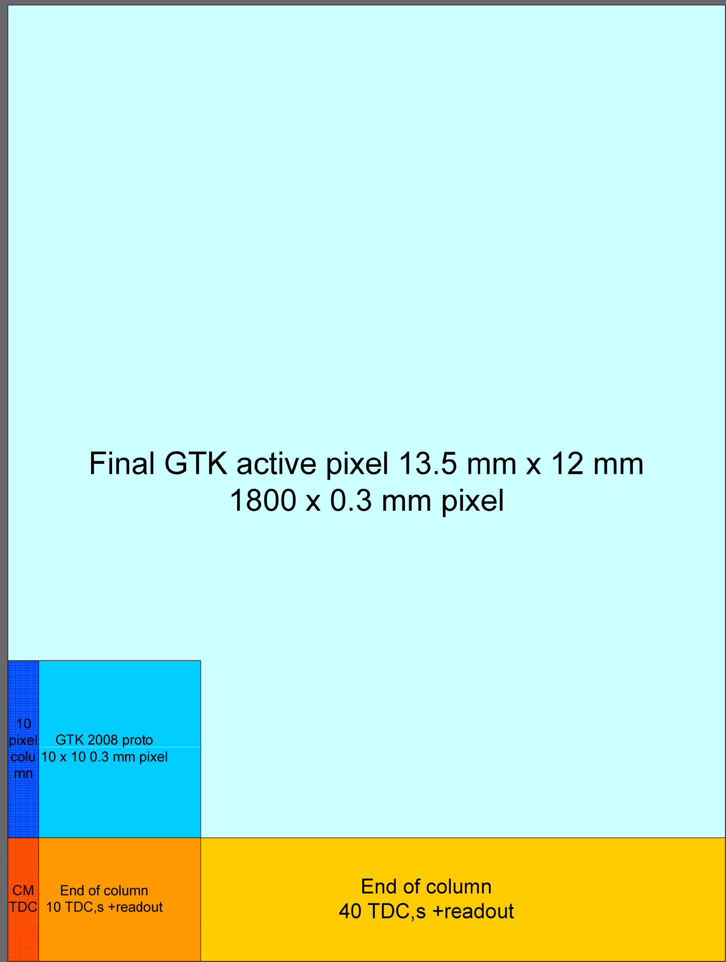


Jitter vs. input charge

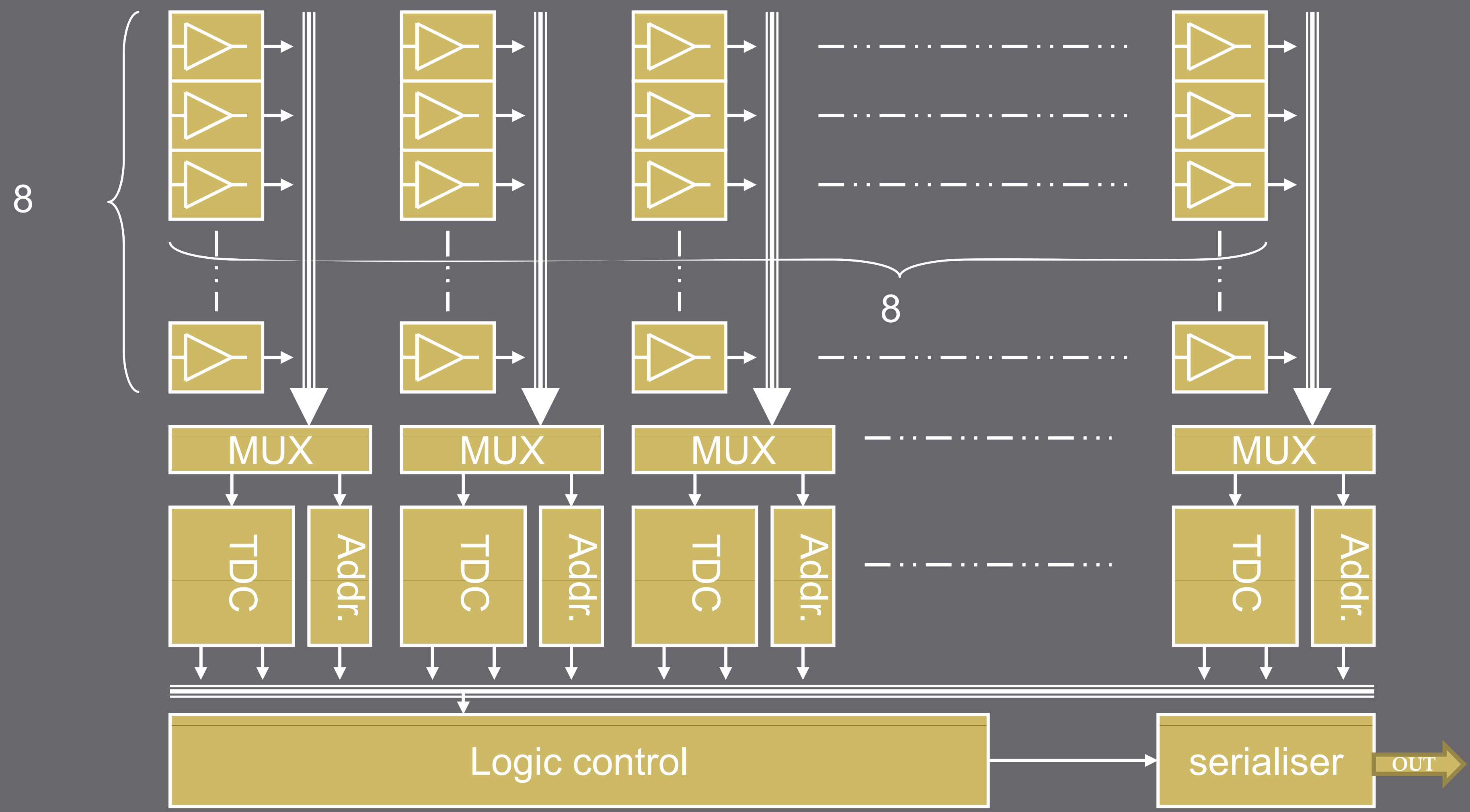
100fF calibration capacitance

NA62 Gigatracker demonstrator

- Ultra fast silicon pixel detector
  - Planar @ sat velocity
  - 3D
    - $1.\ 10^{14}\ p/cm^2$
- ASIC in 130 nm CMOS in development



Demonstrator TS Architecture



- Readout retrieves leading and trailing edges of front end's
- Time encoding of time stamps done by column's TDC

Conclusions

- Preliminary results of 130 nm FE circuits encouraging
  - 0.3 mm x0.3 mm pixel
    - Time resolution <100 ps for a power of 300 μW
    - Charge sensing feature makes possible pixel multiplicity estimate
- Fast sensors looks also encouraging
    - Silicon detector in carrier saturation regime 4 ns collection time
    - 3-D silicon , 1 or 2 ns collection time
- Feasibility of a time stamp pixel tracker
  - Proposal R&D for building a demonstrator pixel module of reduced size for NA62, CLIC and TOF applications
- Material budget is probably the most challenging issue
  - Optimization with time-space measurement precision, cooling and power budget