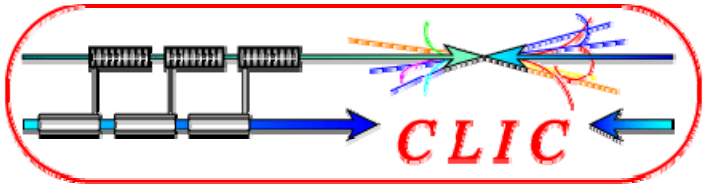


Beam diagnostics developments at LAPP

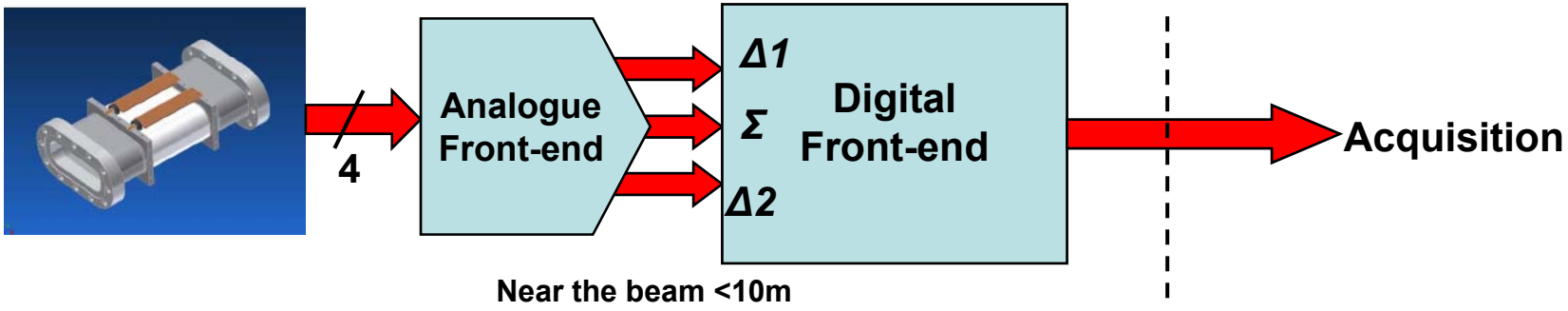
Louis Bellier, Jean Tassan, Sébastien Vilalte

CLIC Working group

17-10-2007

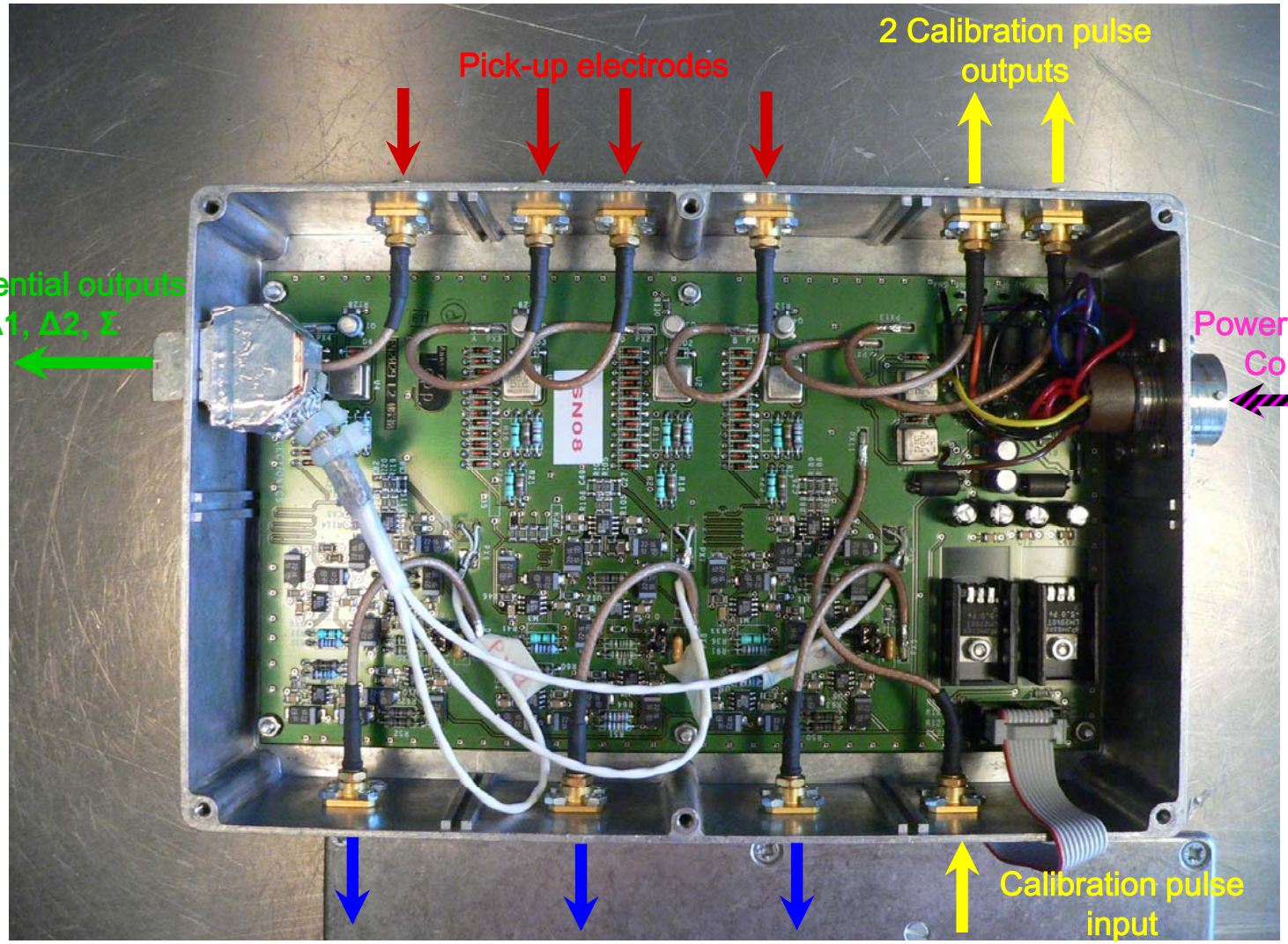
One Channel Architecture

- **Design divided in 3 parts:**
  - » **Analogue front-end board (4 inputs → 1 *Σ and 2Δ)***
  - » **Digital front-end board (sampling)**
  - » **PCI acquisition board (far from radiation)**



Full compatibility with BPI and BPM

Analogue Front-end

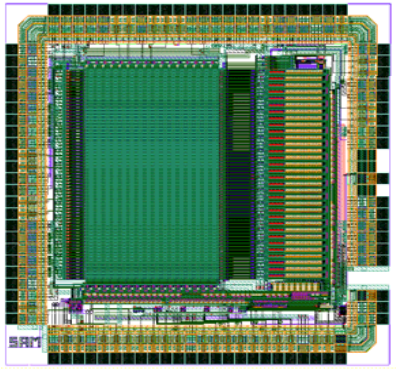


Digital Front-end

Sampling Solution:

Using the SAM analog memory.

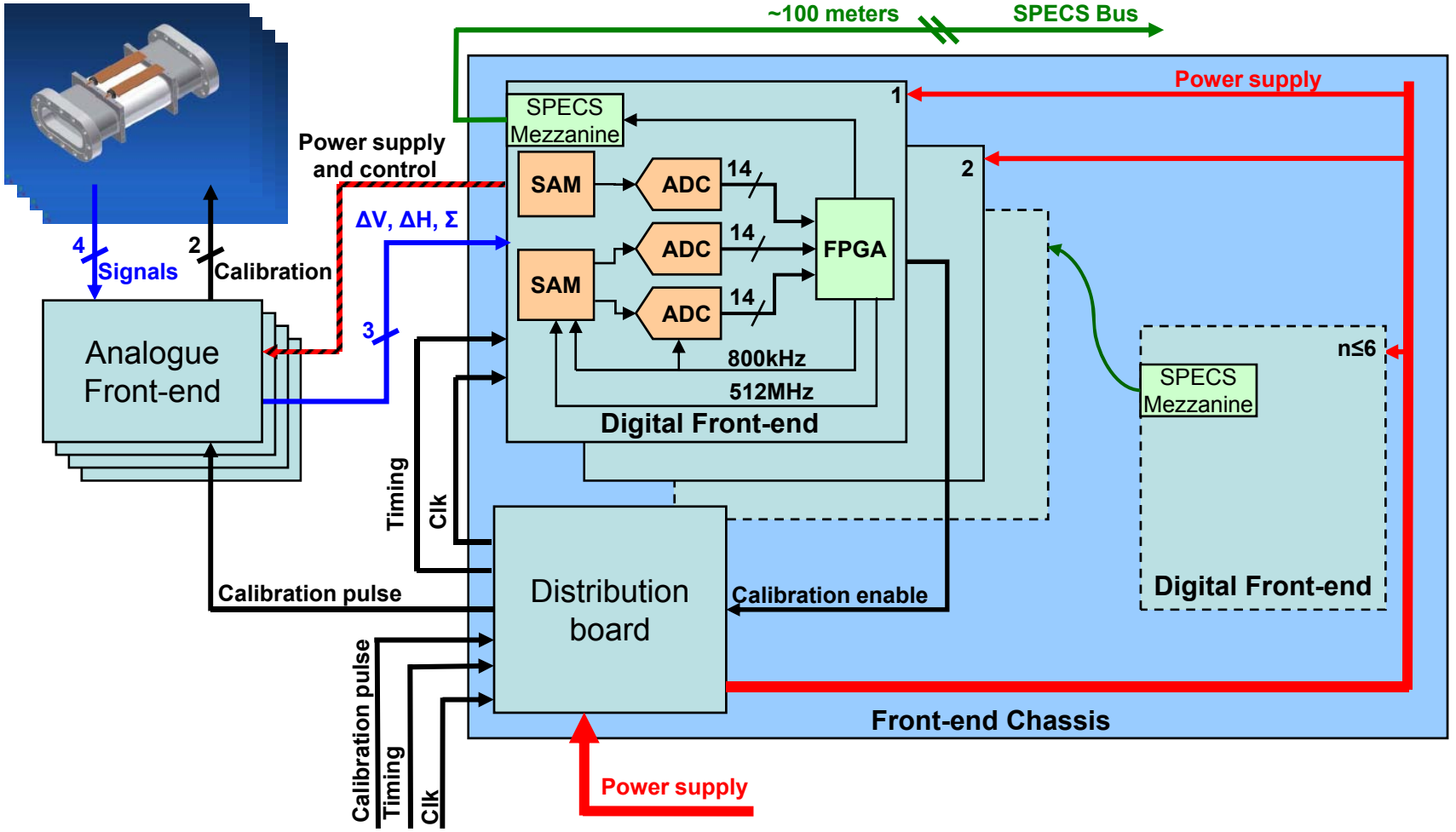
- **Developed by the CEA for HESS2.**
- **1 memory (256 points) per channel**
  - ***500ns of sampling***
  - ***A pulse of 140 ns after CR***
- **Sampling *512MSps***
- **Rad-Hard *200kRad***


CEA SAM Memory

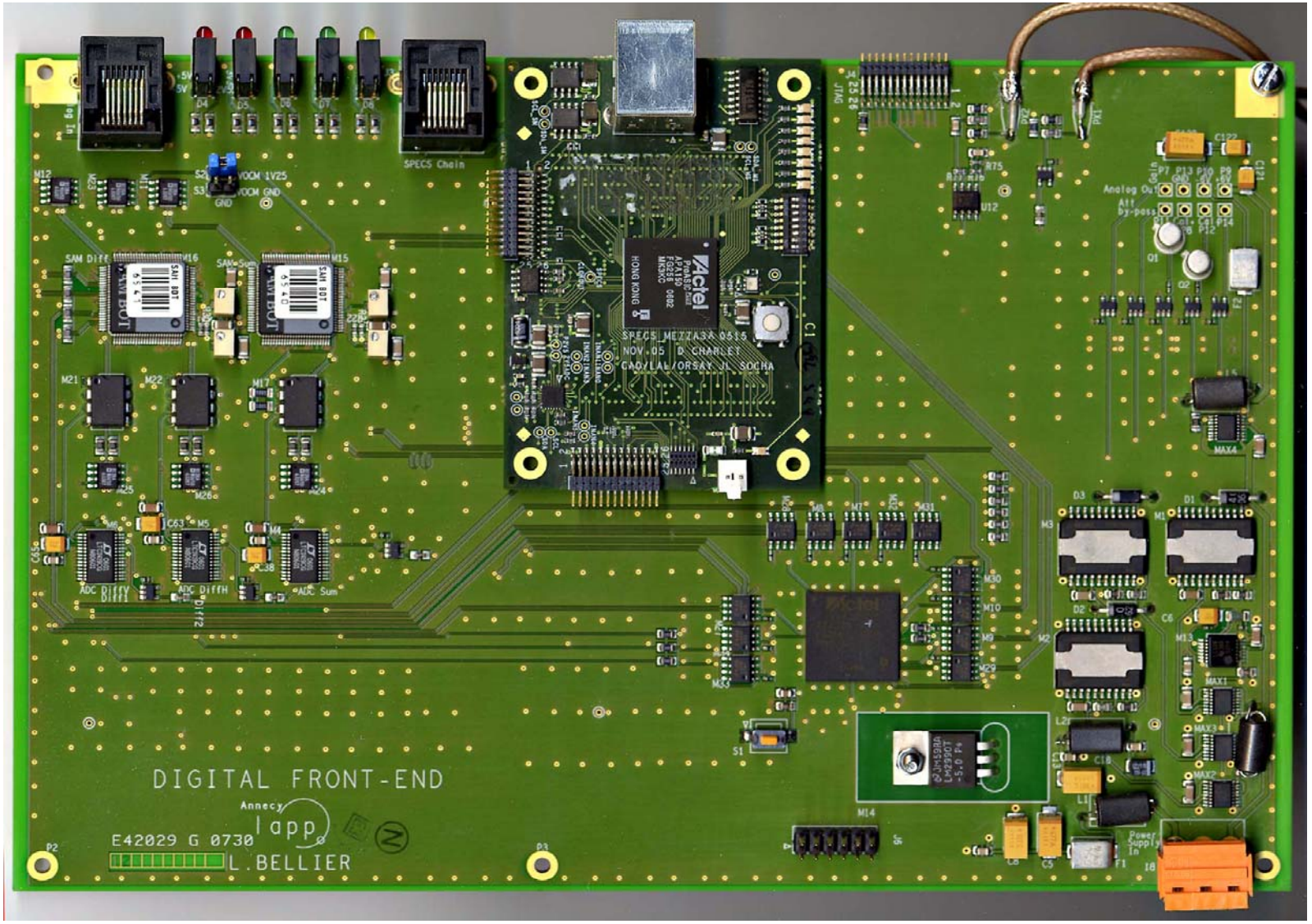
→ After the SAM: ADC rad-Hard, 14 bits, *800kSps*.
↳Synchronization with the SAM output

→ *35kRad* technology due to FPGA

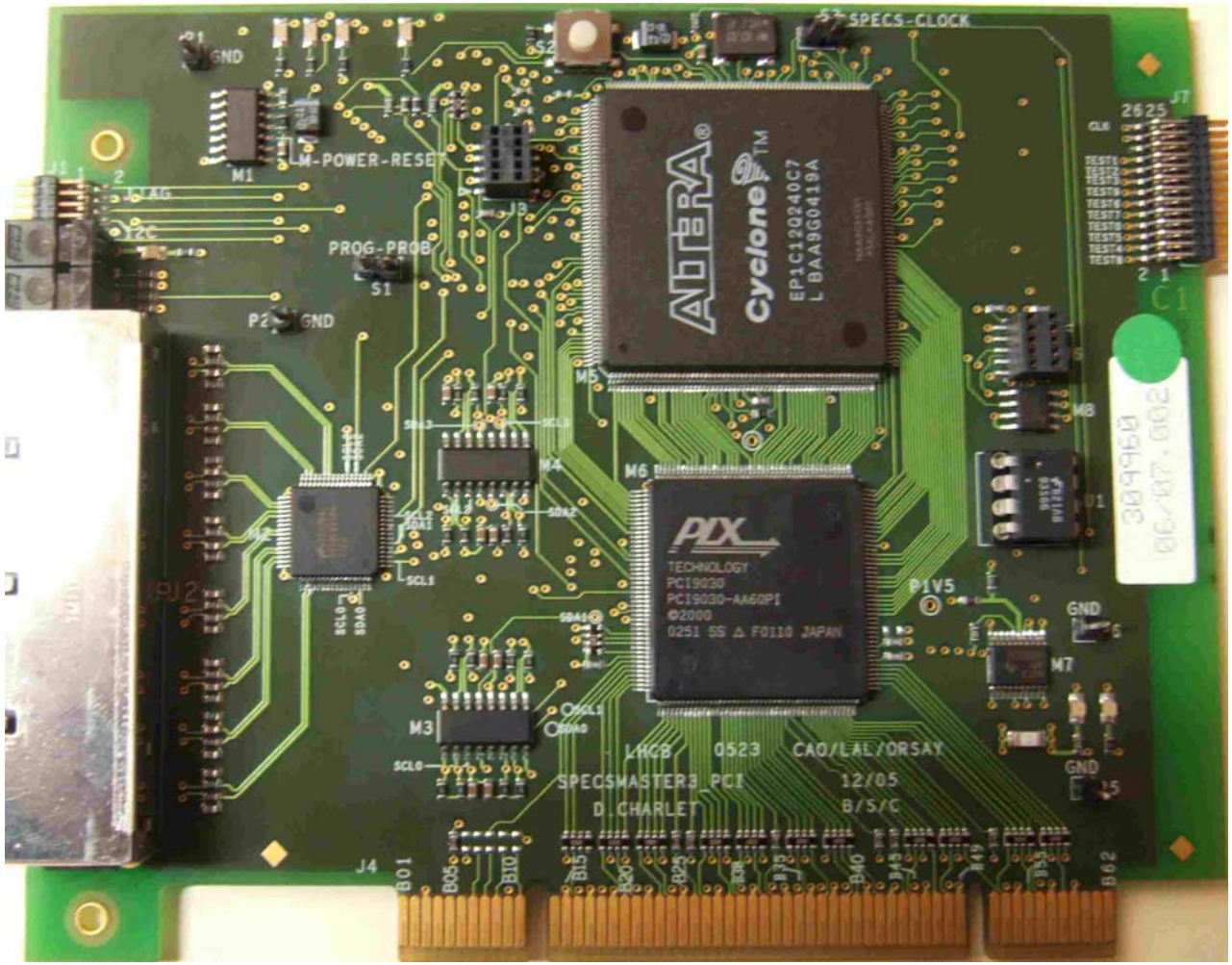
Digital front-end architecture



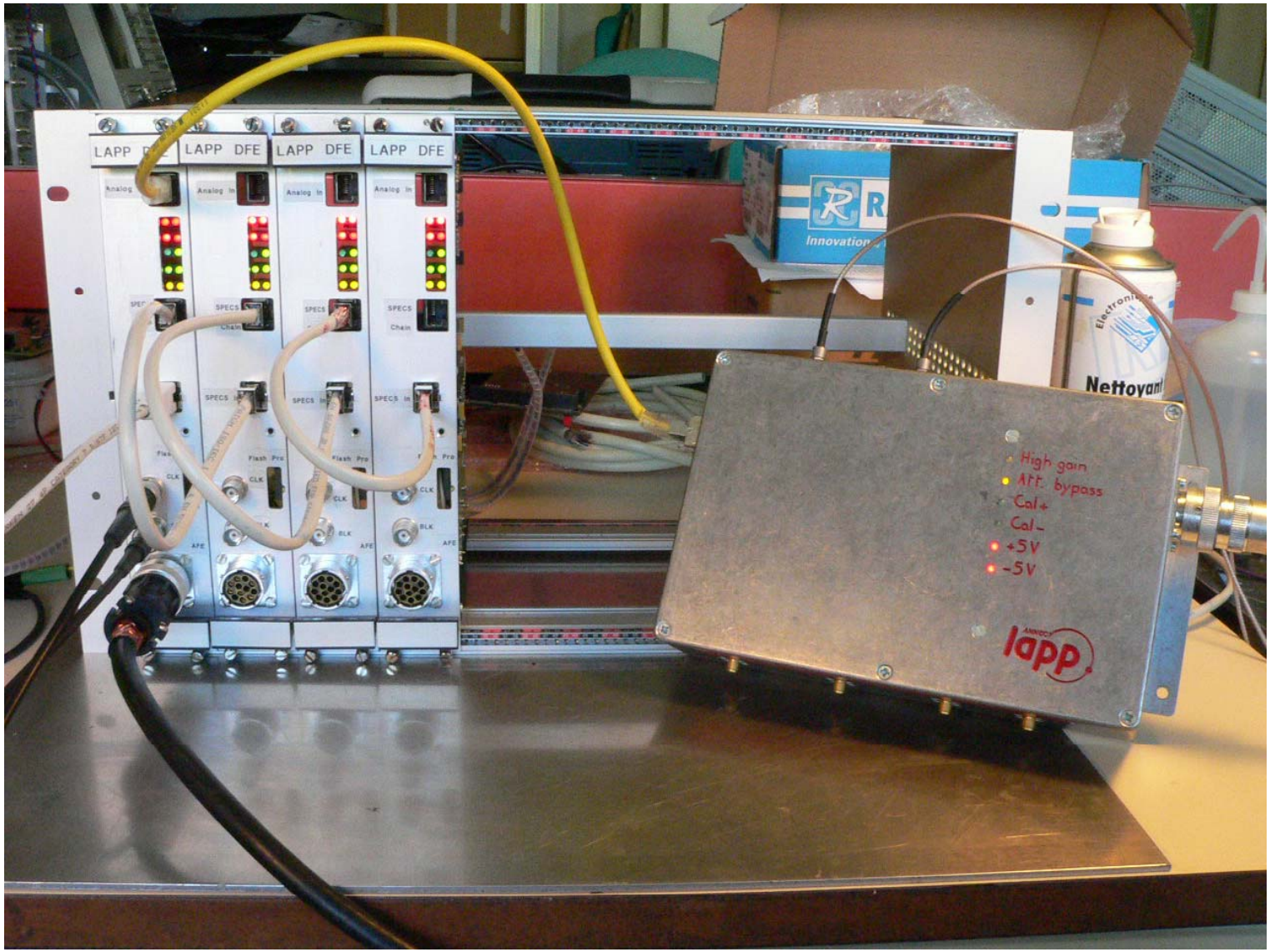
Lapp Digital front-end board



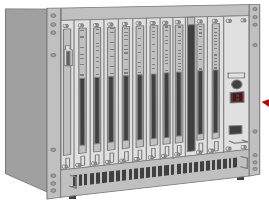
Specs PCI Board



Front-end


LAPP DFE
LAPP DFE
LAPP DFE
High gain
Att. bypass
Cal+
Cal-
+5V
-5V
Nettoyant

2 Solutions



Analogue cables (100m)

BPM

Analogue Front-end

BPM

Analogue Front-end

Digital cables (100m)

Digital Front-end

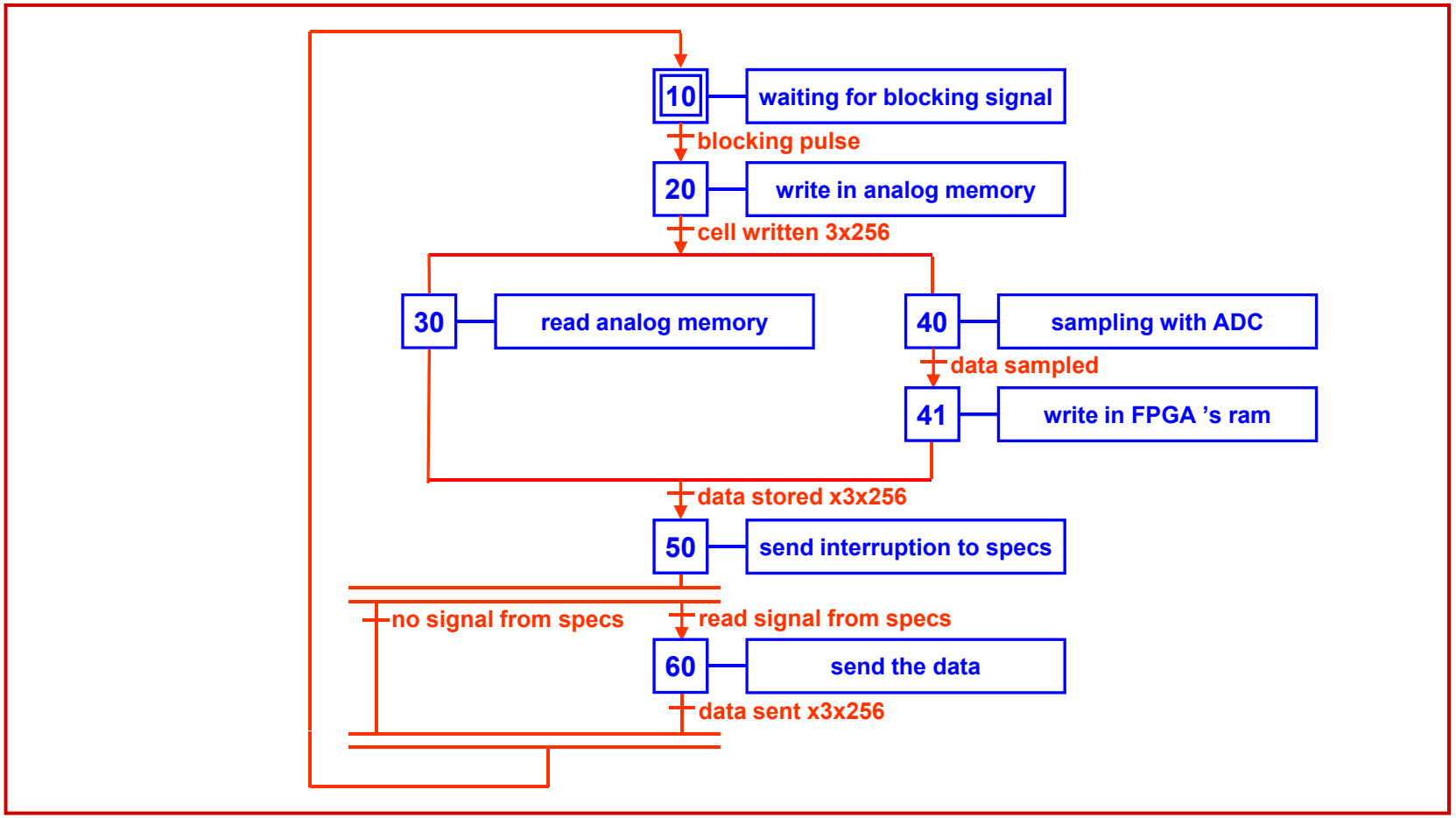
Linux gateway

Original Solution:
8 channels ADC board in VME crates. Long and expensive cables for analogue signals on a single ended transmission.
Total cost for 50 BPMs: **240 k€**

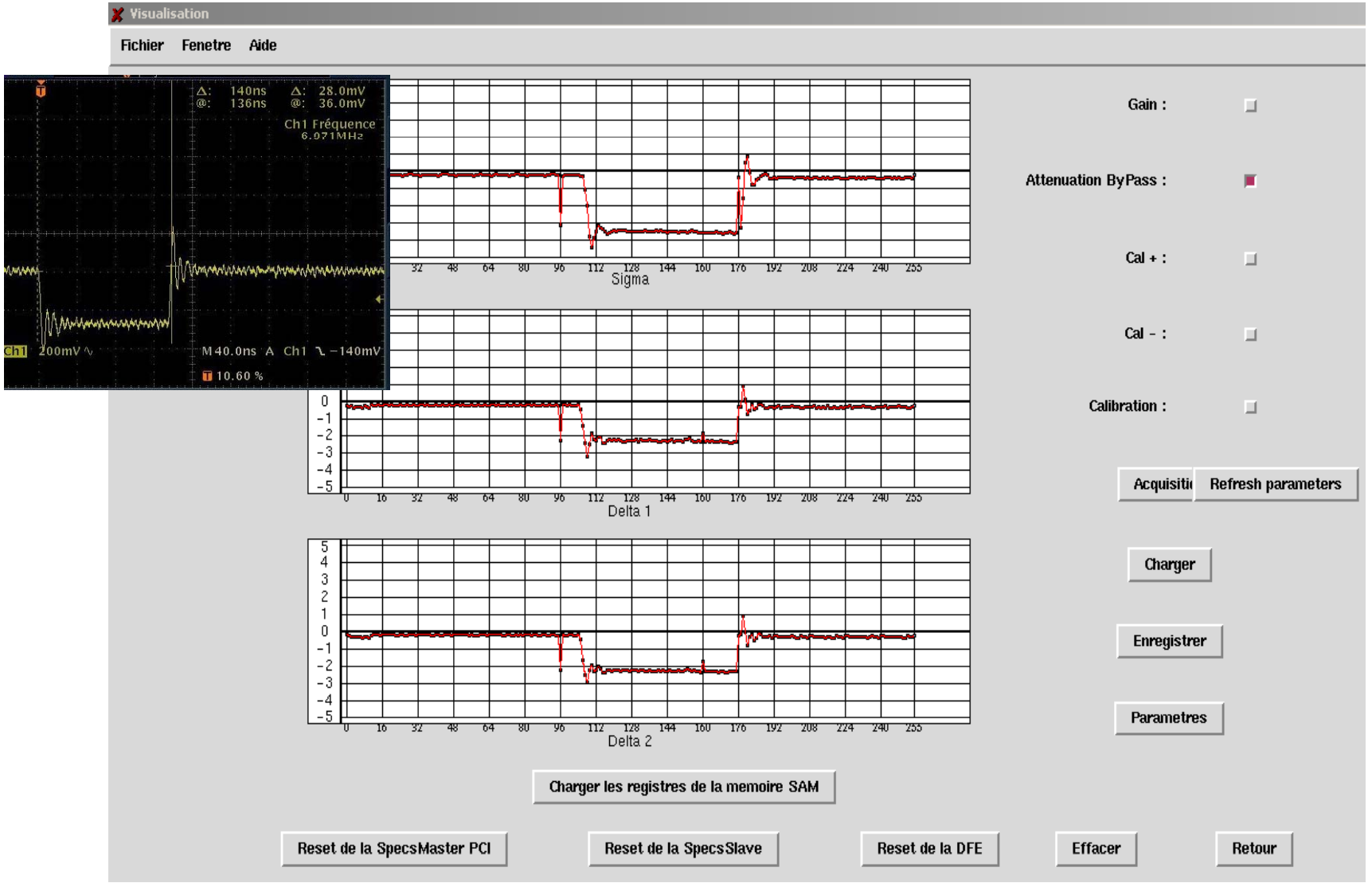
New Solution:
Digital front-end boards under the beam pipe. Differential transmission from analogue board. Just one Ethernet cable for up to six BPM.
Total cost for 50 BPMs: **80 k€**

New solution ⇒ 3 TIME$ CHEAPER!!!

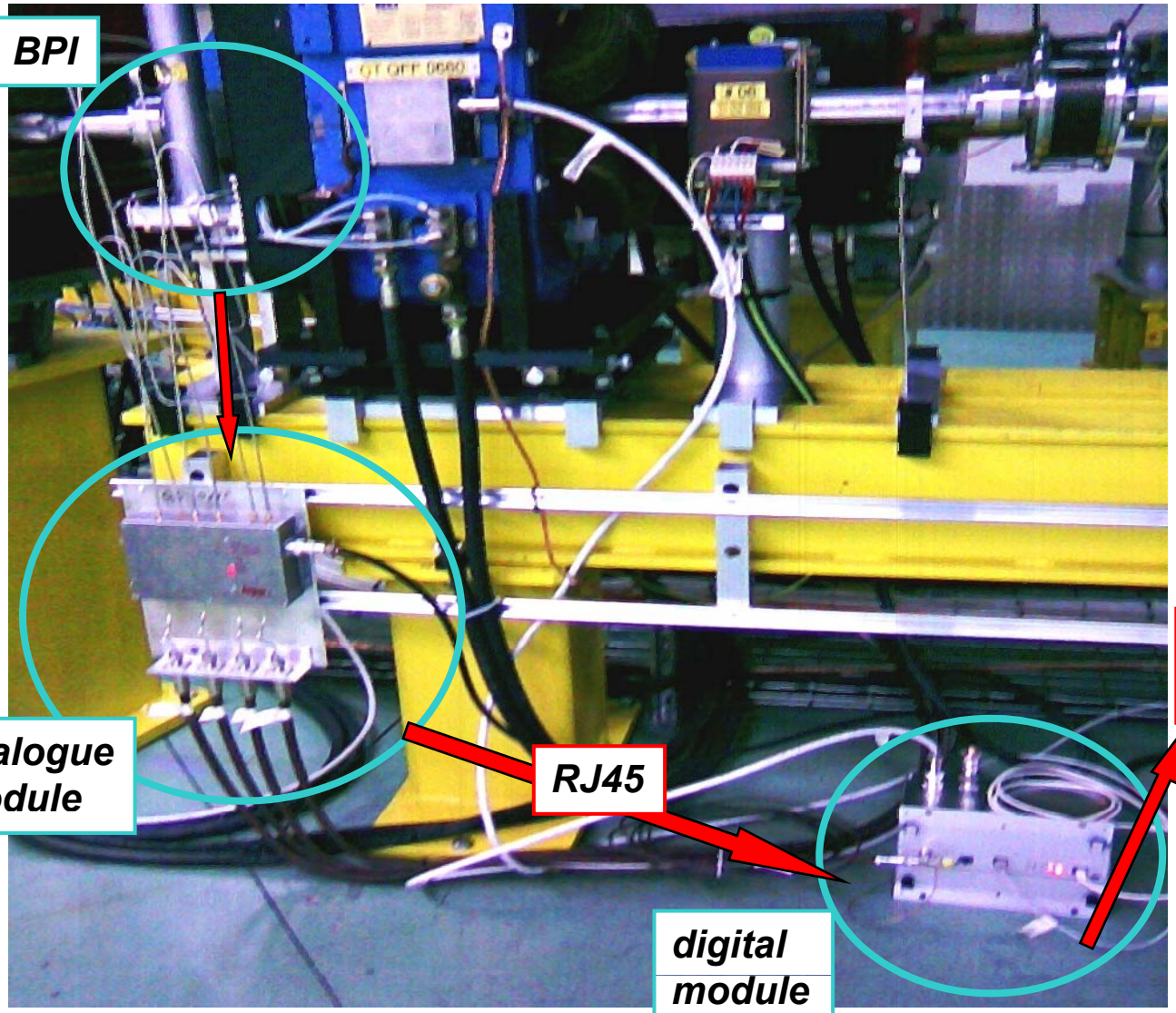
Sampling cycle



First Results



Inside CTF3, under TL1



Point of the activity(1)

History:

September 2005: CTF3 LAPP group creation.
February 2006: Proposal for a full front-end solution for the BPI readout.
November 2006: TL1 analogue modules installation (7) + 1digital FE for tests.
Spring 2007: ½ CR analogue modules installation (13) and BPI compensation tuning.
Summer 2007: ½ CR analogue modules installation (7).

TL1 & CR: 27 analogue readout electronics with BPI compensation filters for VME standard acquisition.

One digital front-end on TL1 for validation of the TL2/CLEX acquisition.

Man power: ~4.8 men.year since september 2005.

Point of the activity(2)

Next installation: *production for March 2008*

Analogue: ***16*** readout modules for BPI's in collaboration with Uppsala.
10 for TBTS → 40mm BPM's on Uppsala responsability.
6 for TL2 → Frascati BPI's on LAPP responsability.
4 spares.

Digital FE: ***43*** front-end boards for TL2, TBTS, TL2', TBL. (+7 spares)
9~12 crates with distribution boards for 4~6 FE boards each.
Production in collaboration with CERN and Uppsala.

Cost issues: digital FE cost for 1 BPM including cables and crates → ***~1.6k€.***
VME solution cost → ***~4.8k€*** due to expensive analog cables.

The future

For CLIC, the local front-end is well-appropriated for high number of pick-ups and long accelerator: no analogue signals to transmit.

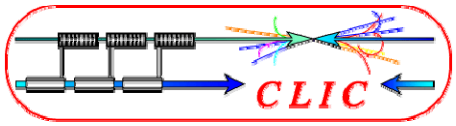
With an access every Km, solutions have to be found for:

- ***Power supplies:*** *low voltage power supplies not realizable due to voltage drop on long cables.*
  - → 220V Rad-hard power supplies implemented in crates.
  - → A better solution could be an intermediate DC power supply (i.e. 48V) locally converted with rad-hard DC-DC converters.
- ***Calibration:*** *local calibration current generation → hard in a radioactive environment due to MOS rad-hardness.*
- ***Clocks/Ethernet cables*** *need "relays" in the machine → possibility to use optic fiber transmissions.*

These functions could be implemented on the distribution board.

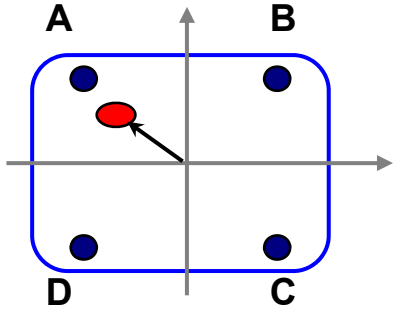
The maintenance of such a system has to be defined.

Conclusion



- Flexible solutions (good basis for CLIC development)
- A complete read-out electronic kit
- Complete design tested next spring
- LAPP very interested by CLIC studies

Beam diagnostic



The current distribution on the 4 electrodes depends on the beam deviation.

BPM Acquisition (DL & CR):
Current to voltage conversion /50Ω

- ***Σ*** *:* Beam intensity corresponds to the sum of the 4 voltages (A+B+C+D). *Σ constant if constant beam intensity.*

- ***Δ*** *:* Beam position obtained by combination of the two differences: (A-C) & (B-D).

Vertical Information (+)

$$V=\frac{(A+B)-(C+D)}{A+B+C+D}$$

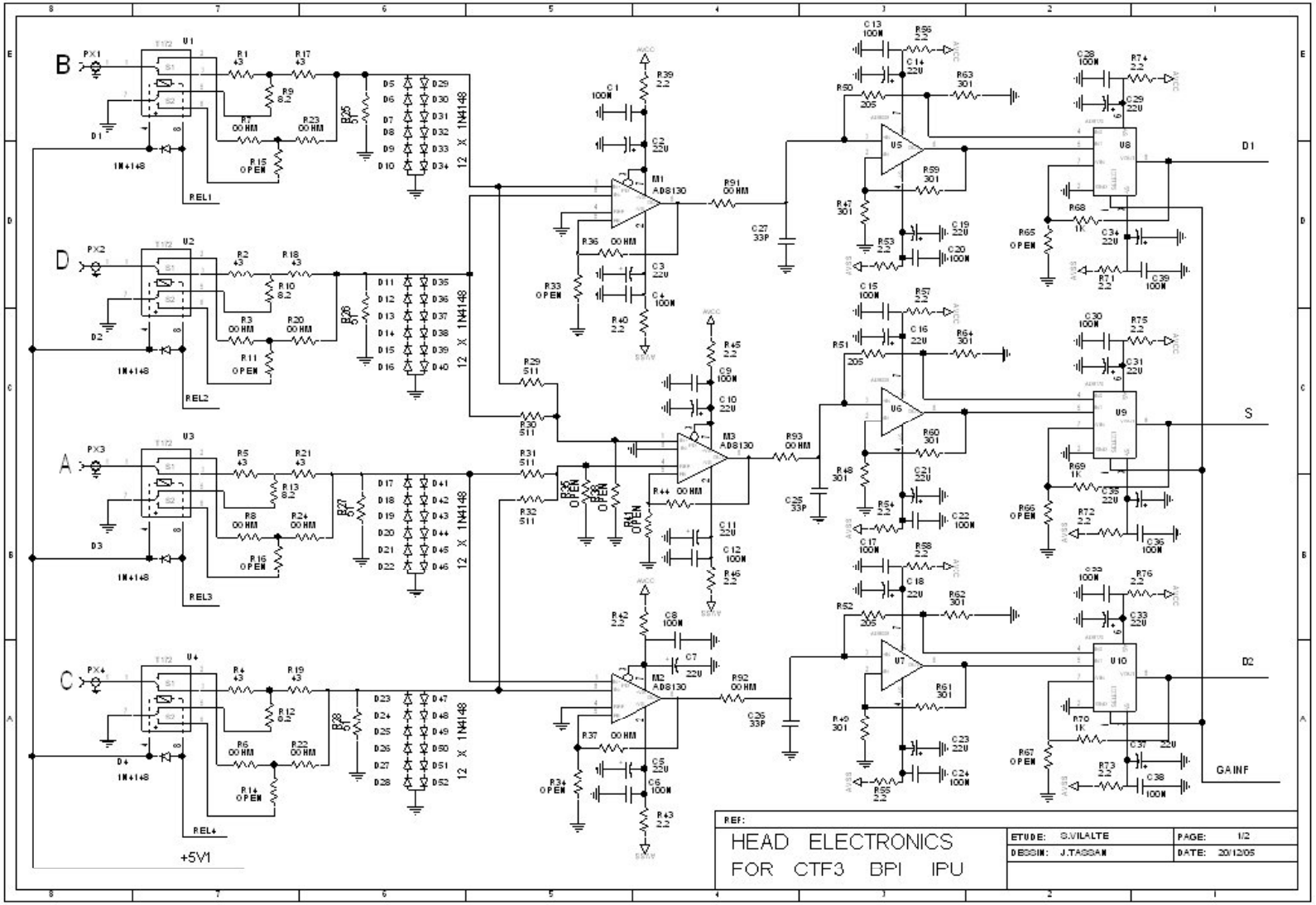
software

Horizontal Information (-)

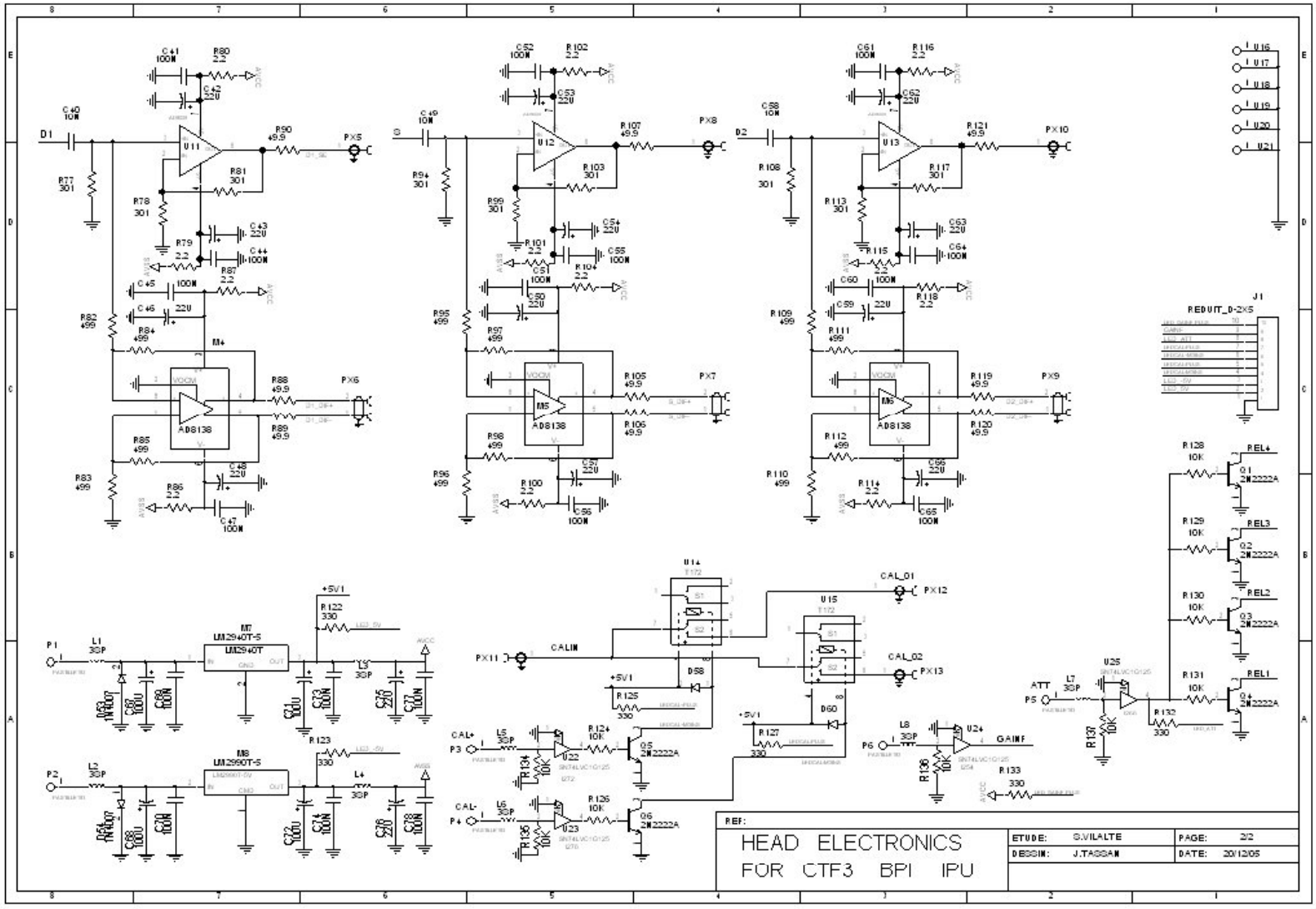
$$U=\frac{(B+C)-(A+D)}{A+B+C+D}$$

$$Y=k_{y0}.V+k_y(U,V) \qquad X=k_{x0}.U+k_x(U,V)$$

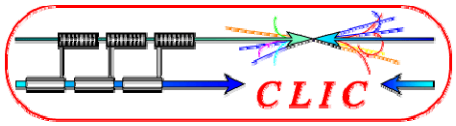
Developed Electronics (1)



Developed Electronics (2)



Developed Electronics



- Input passive attenuation by ***12*** to fit the signals to the electronics input range.
  → Bypassed for lower current configurations.
- 3 outputs: the sum ***(A+B+C+D)*** and two differences ***(A-C) & (B-D)***.
- 2 switchable output voltage gains.
- Attenuation ,gain and calibration remote-controlled by the digital part.
- Frequency bandwidth according to the BPI: *40kHz to 100MHz.*
- *BPI* frequency compensation
- Differential (digital FE solution) and Single ended outputs (VME ADC solution).
- BPM/BPI full compatibility.