LHC Upgrades for high luminosity

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CXD Work shop 19th April 2012

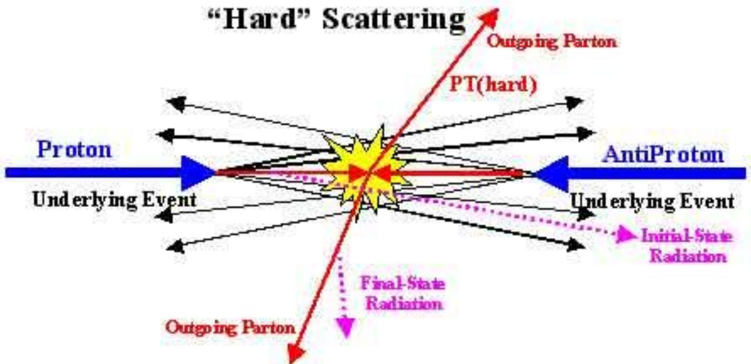
Upgrades for handling high data rates: focus on a few issues

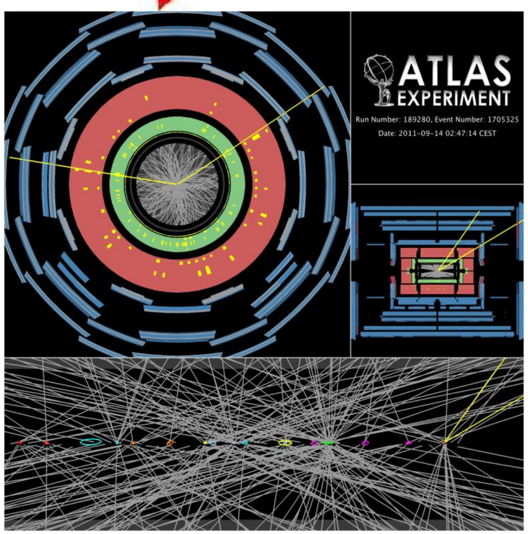
- ATLAS-UK centric, focus on few key area where ATLAS-UK is working
  - Pixel detectors: recording complex events
  - Triggering: selecting interesting events to record using hardware & software triggers
  - Computing & Software: handling large complex events in an efficient manner for speed & memory

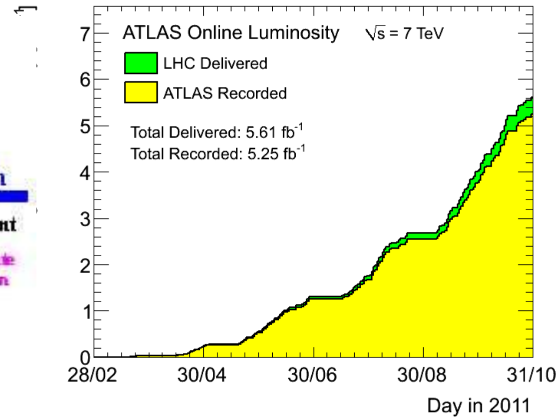
- A few words on LHCb
  - Avoiding hardware triggers: buffer the entire event using high-speed links and intelligence on chips

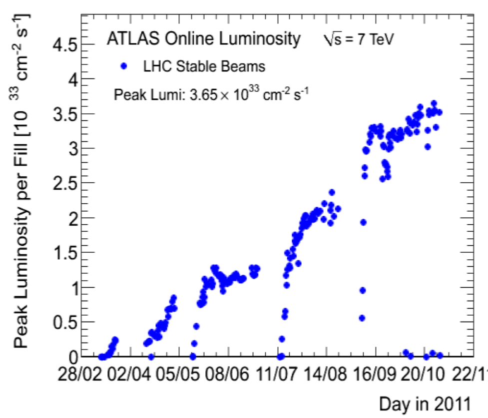
- Other experiments are available: ALICE & CMS

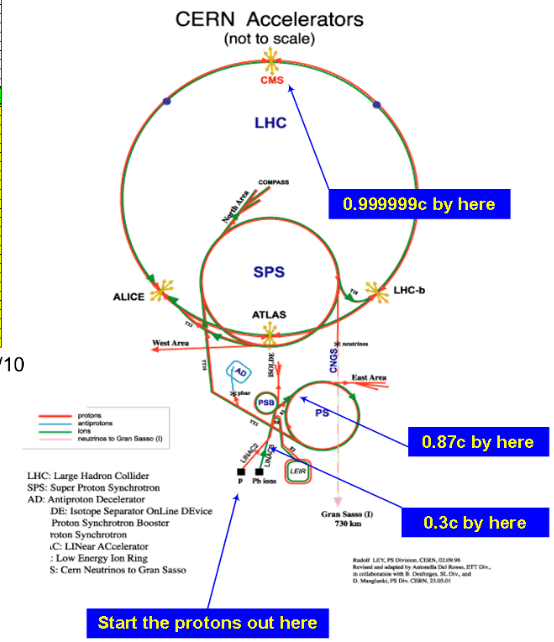
The Large Hadron Collider





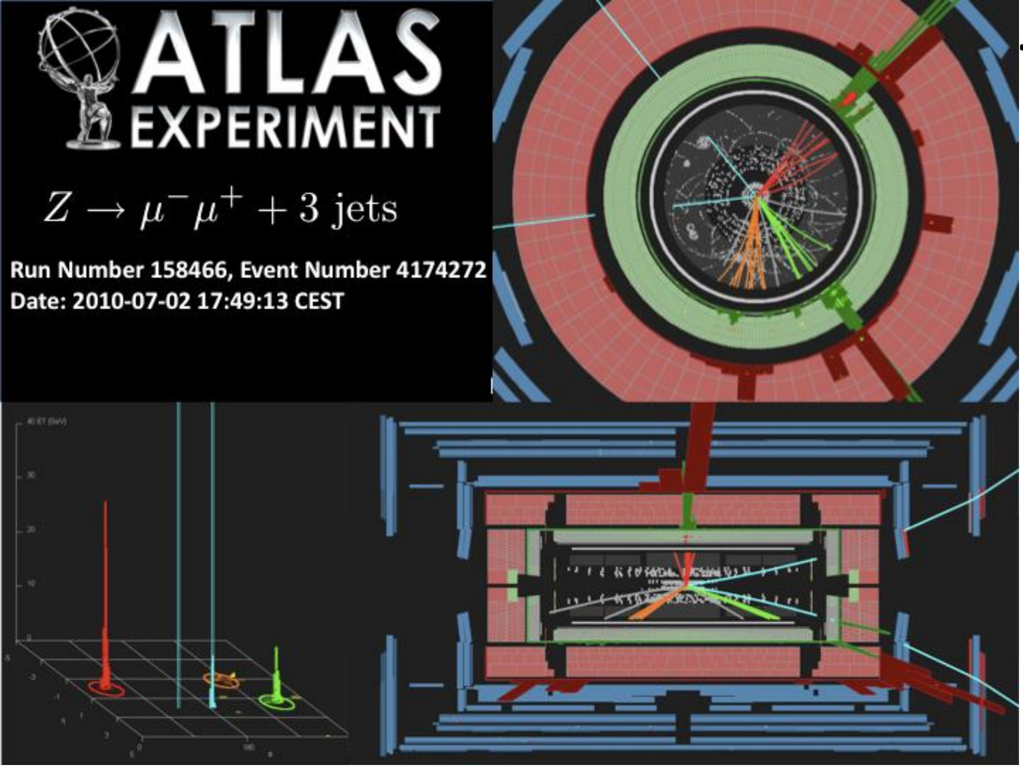






Design luminosity $10^{34}cm^{-2}s^{-1}$
Design energy 14TeV

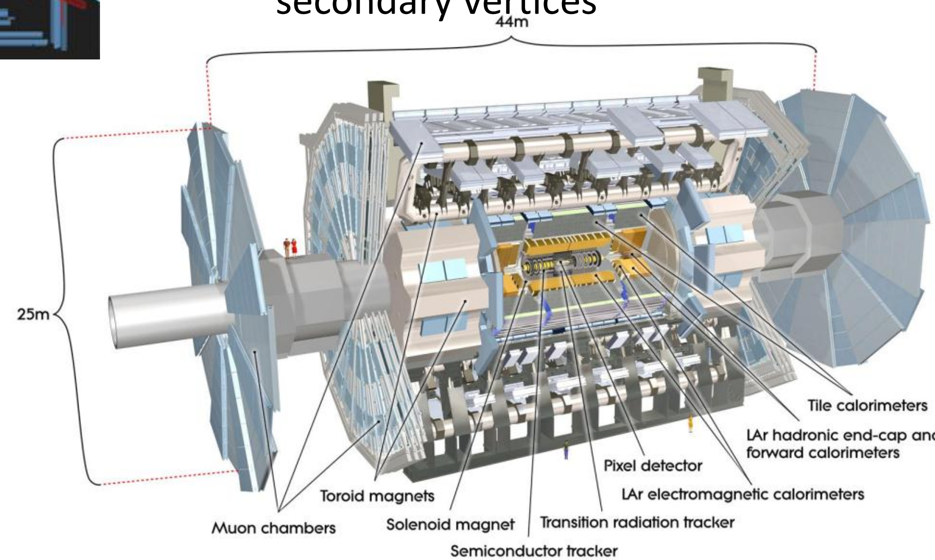
Interesting interactions accompanied by many "uninteresting" soft pp collisions -- pileup



The ATLAS experiment

ATLAS is a general purpose experiment designed to identify the elements of a high energy proton-proton collision

- Leptons: electrons, muons, taus
- Jets: the signatures of quarks and gluons
- Photons
- Missing energy
- Identify long-lived particles via secondary vertices



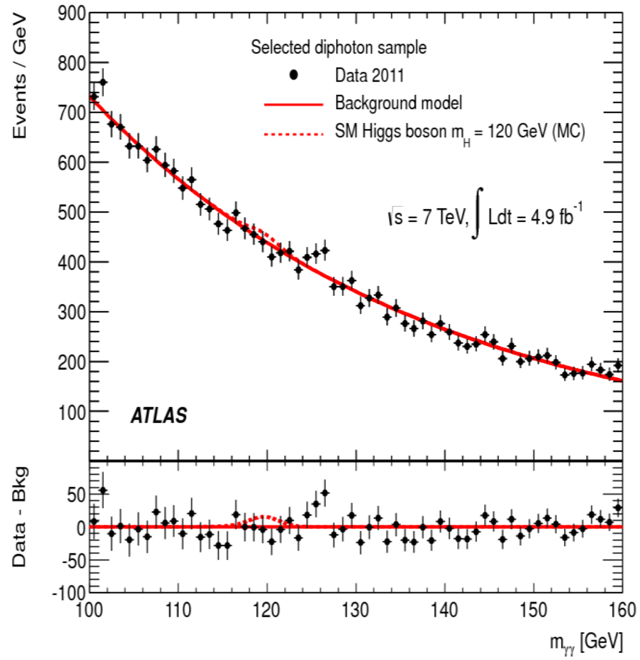
- **Tracking** (~86M channels)
  - Reconstructs trajectories of charged particles
  - Measures charge and momentum
  - Identifies vertices
- Calorimetry (~196k channels)
  - Measures energy of electrons, photons and jets (quarks/gluons)
- Muon system (~2M channels)
  - Identifies muons
  - Measures their trajectory (with the tracking system)
- **Trigger** & DAQ
- **Computing & Software**

3000 collaborators
UK ~10%

Performance in 2011

Subdetector	Number of Channels	Approximate Operational Fraction
Pixels	80 M	95.9%
SCT Silicon Strips	6.3 M	99.3%
TRT Transition Radiation Tracker	350 k	97.5%
LAr EM Calorimeter	170 k	99.9%
Tile calorimeter	9800	99.5%
Hadronic endcap LAr calorimeter	5600	99.6%
Forward LAr calorimeter	3500	99.8%
LVL1 Calo trigger	7160	100%
LVL1 Muon RPC trigger	370 k	98.4%
LVL1 Muon TGC trigger	320 k	100%
MDT Muon Drift Tubes	350 k	99.7%
CSC Cathode Strip Chambers	31 k	97.7%
RPC Barrel Muon Chambers	370 k	93.8%
TGC Endcap Muon Chambers	320 k	99.7%

88M ch



Homing in on the Higgs?

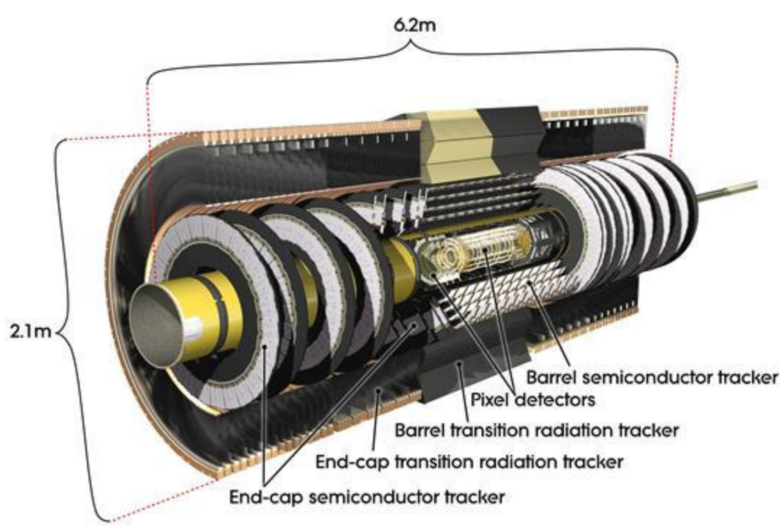
LHC & ATLAS Upgrade

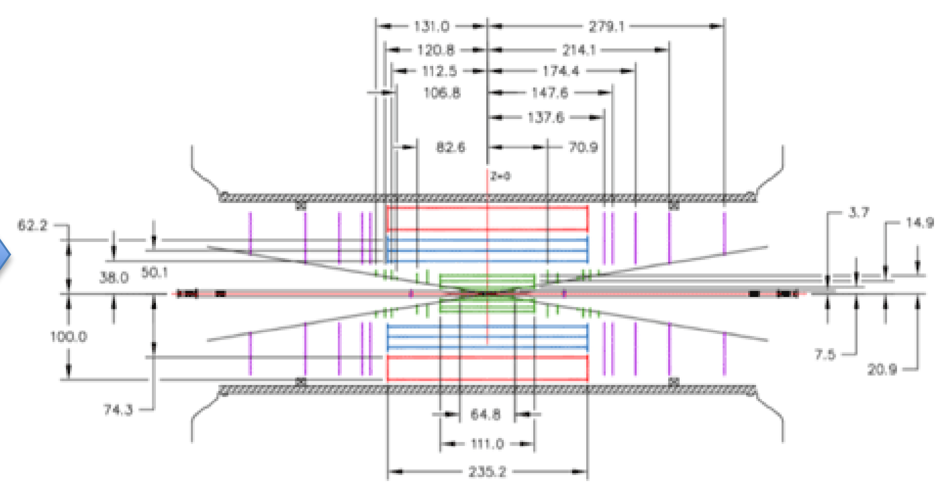
- Aims of the Upgrade
  - Increase the luminosity to $2\times10^{34}cm^{-2}s^{-1}$ (twice design luminosity) and to $5\times10^{34}cm^{-2}s^{-1}$
  - Probe electroweak symmetry breaking
    - Higgs couplings
    - VV-scattering at high mass
  - Search for new physics
    - Extend mass scale
    - Precision measurements of standard model (PP) parameters

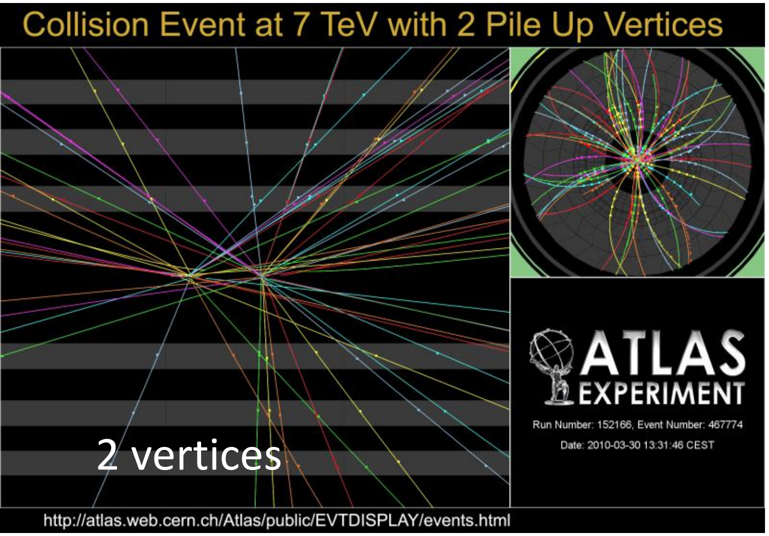
- Phases of the Upgrade
  - 2018 Upgrade to $\sim2\times10^{34}cm^{-2}s^{-1}$
    integrated luminosity $\sim300fb^{-1}$
  - 2022 Upgrade to $\sim5\times10^{34}cm^{-2}s^{-1}$
    integrated luminosity $\sim2500fb^{-1}$
- Aim for 5x increase in design luminosity
  - Pile-up from ~20 → 200
- Impact on ATLAS
  - Upgrade trigger & DAQ
  - Replace tracker
  - (calorimeter & muon systems)

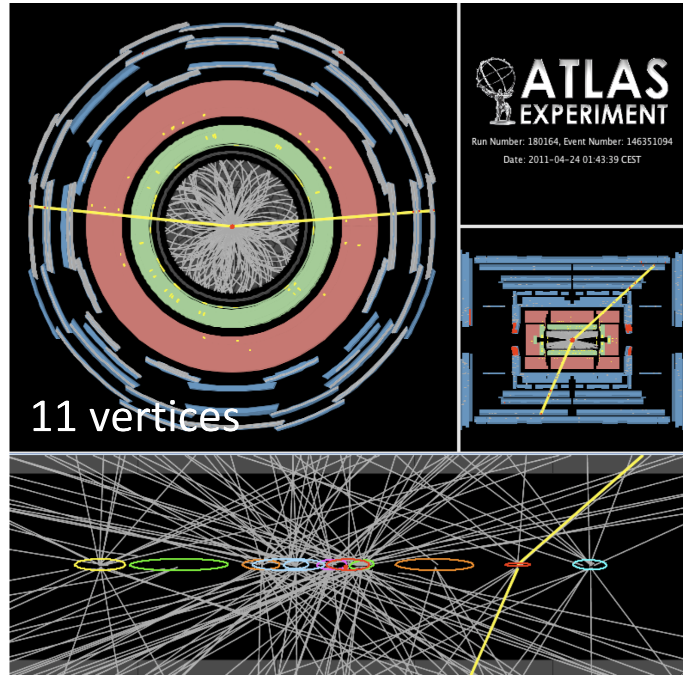
Tracking

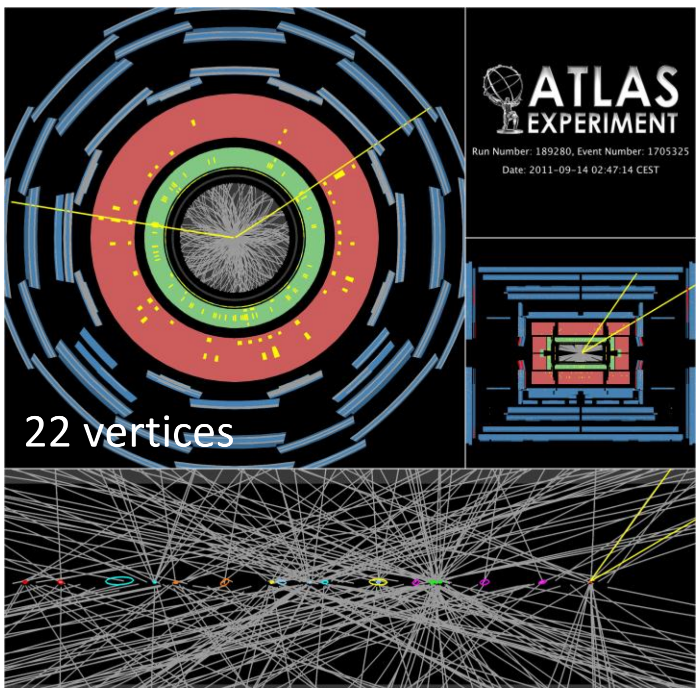
- Tracker currently consists of
  - Si pixels
    - 1.7m^2, 80M channels
    - Critical for pattern recognition and primary and secondary vertex reconstruction
  - Si microstrips (SCT)
    - 60m^2, 6M channels
    - Precision space points
  - Transition radiation – gas based
    - Extends radius – improve momentum resolution
- Granularity
  - Defined by detector occupancy
  - Maintain ~1% to ensure pattern recognition
- Need to maintain for upgrade
  - Average number of charged tracks ~30/pile-up event: ~20 → ~200
  - 80M→~400M pixels
  - 6Mstrips → 45Mstrips
  - Remove TRT
  - Total ~300m^2

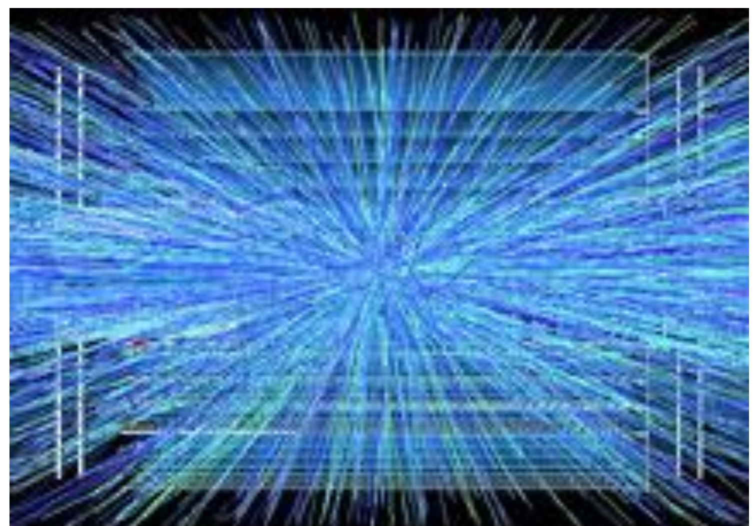








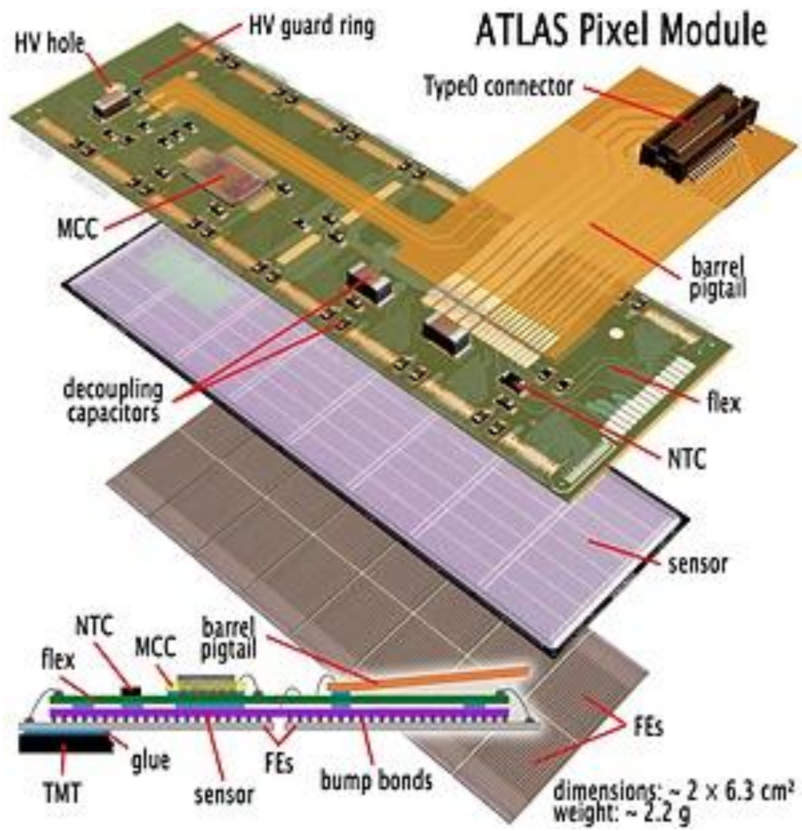


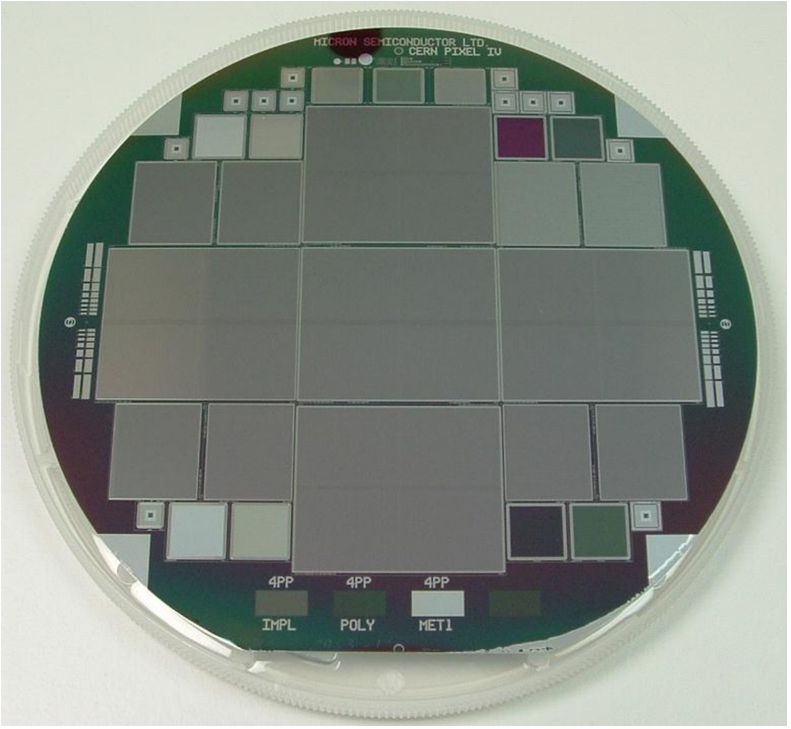


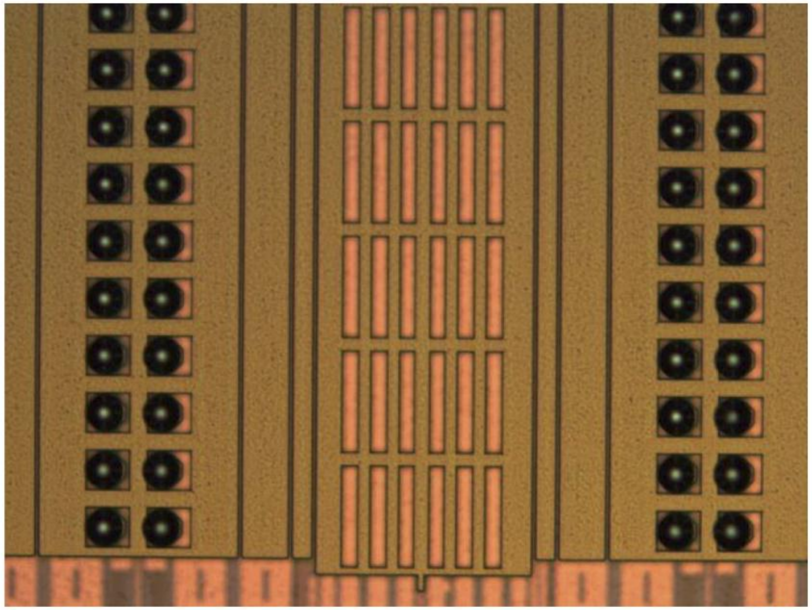
Simulated event with 200 pileup events

ATLAS-UK pixel programme

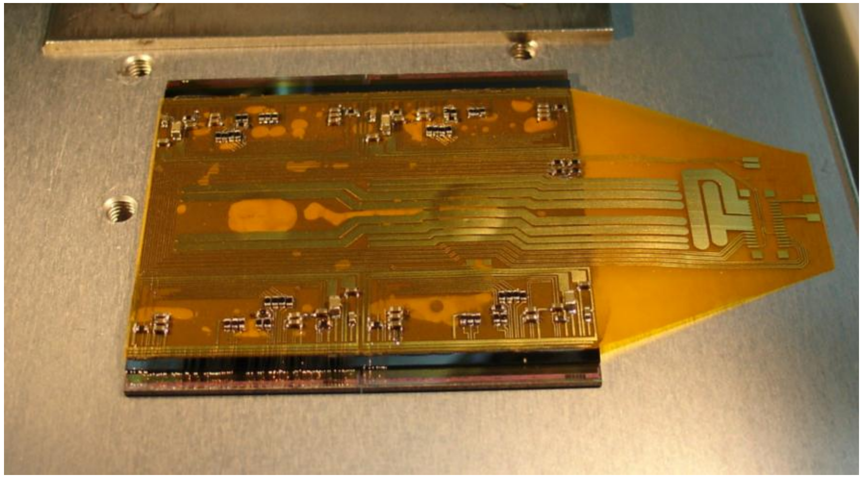
- Challenges
  - Radiation damage essentially scales with luminosity
  - Require sensors capable of operating at ~few $10^{16}ncm^{-2}$
  - Low mass to minimise conversions and degrade calorimetery
  - Low cost to allow large area coverage
- Sensors:
  - Si: planar and 3D
- Module fabrication
  - Thinning
  - Interconnects: bump-bonding and TSVs
  - High fill factor
- Engineering
  - Support structures







Solder bump bonding at VTT



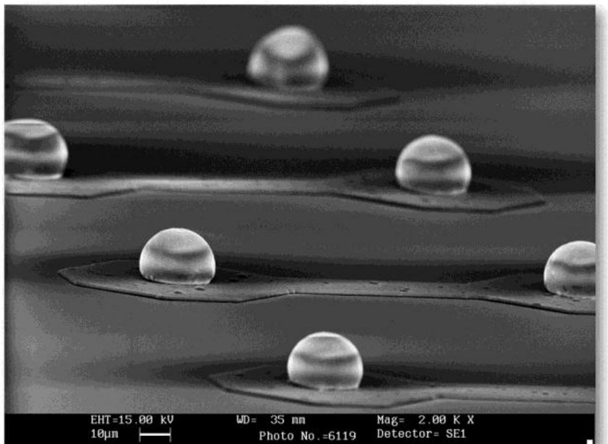
Assembled module

Quad pixel sensors from micron
2x2 FE-I4 readout chip ~4x4cm^2

Pixel size: 250µmx50µm
29,228 channels

FE-IX: 65nm, 3D technology development

Bump-bonding interconnects at RAL

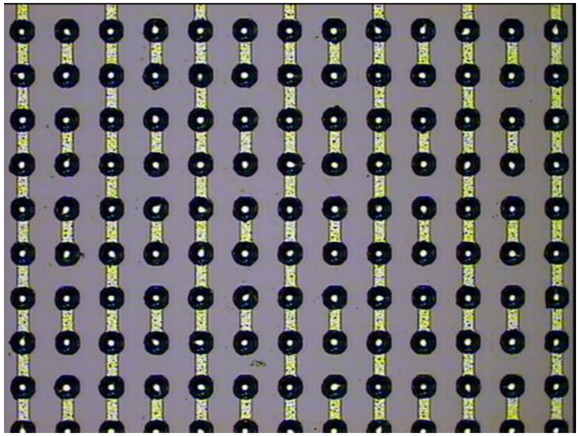


22micron bumps grown using evaporator and formed using reflow oven at RAL

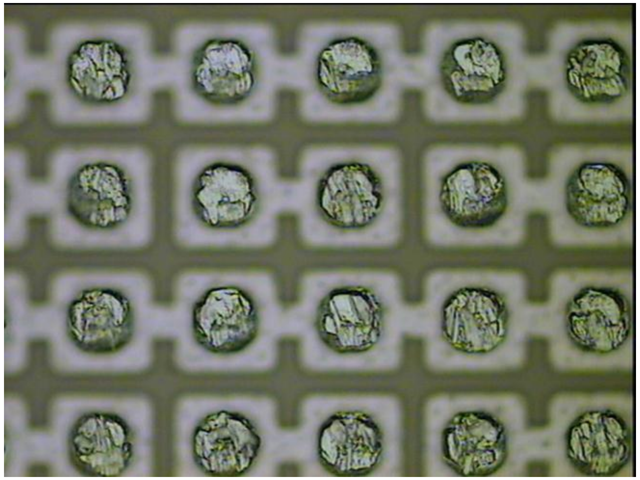
- In based process under development
  - Low temperature:
    good for assembling thin modules
    good for assembling irradiated modules
- Facility for UK prototyping and production
  - Limited capacity in Europe
- Requires external elements
  - 8” photolith
  - Underbump metalisation

In bump-bonding bonding at RAL

Test vehicle	Cold compression	Reflow
RAL	>99.9%	>99.7%
MPX	Not yet determined	>99.9%



A bumped medipix geometry test device prior to bonding (bumps formed at RAL, CNM under bump metallization).

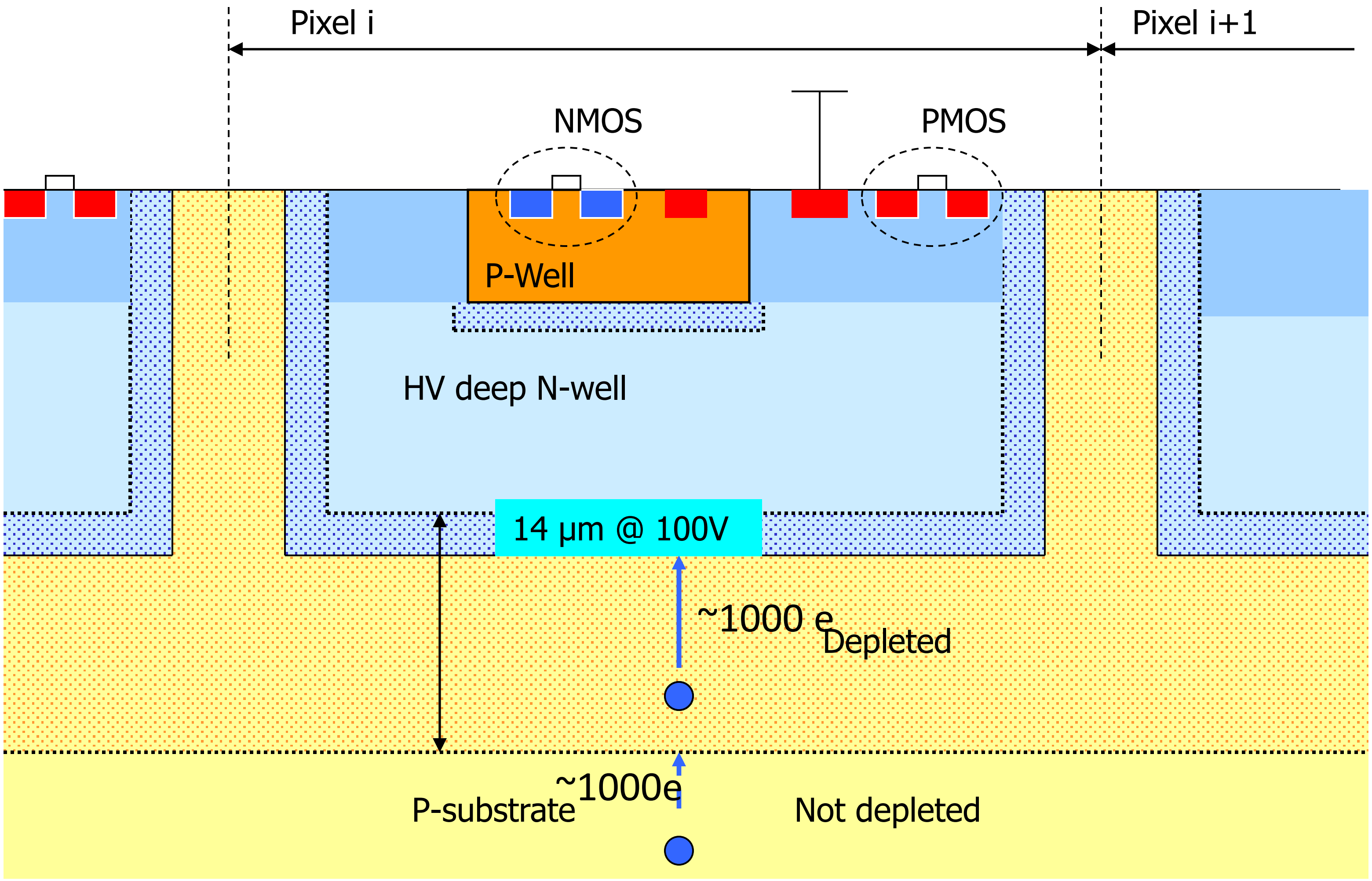


A medipix geometry test device after bonding and shear testing

HV-CMOS sensors

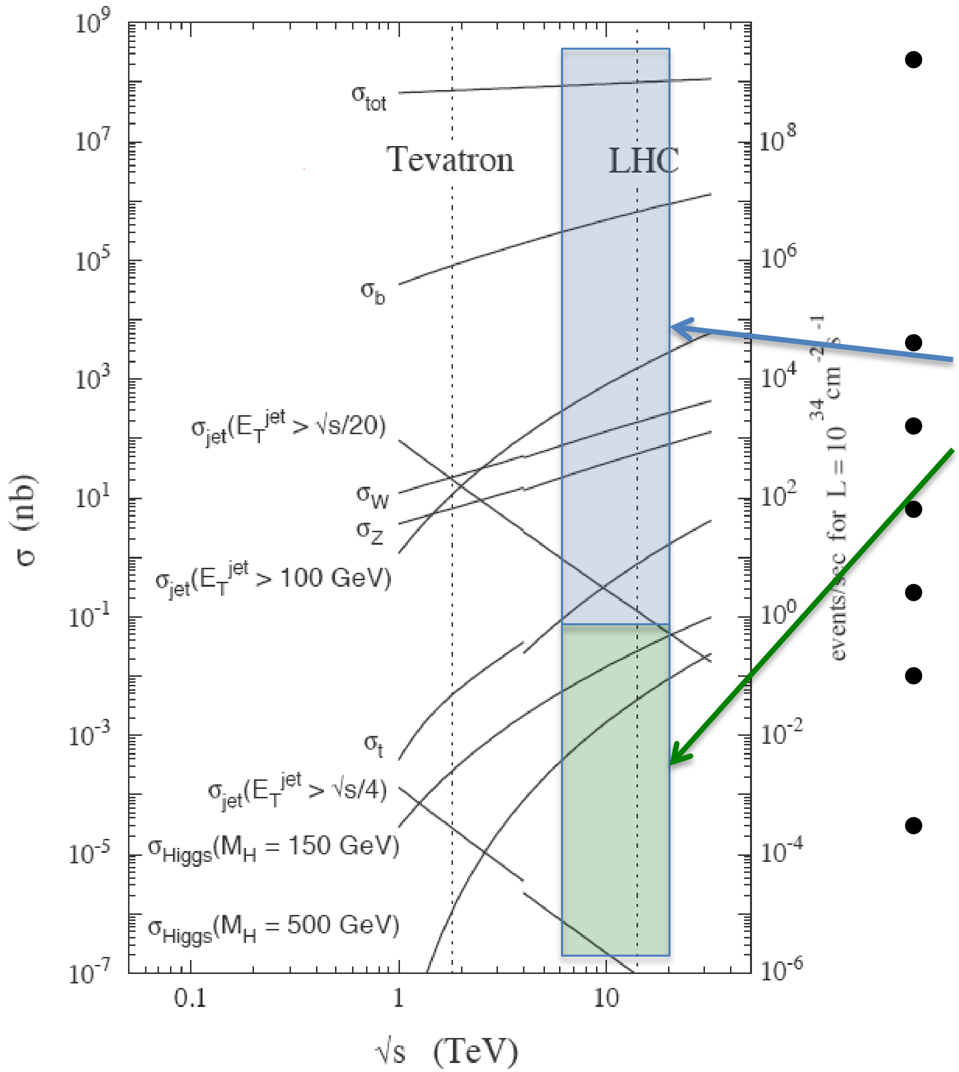
- Recent development
- HV process
  - Faster – collection via drift
  - radiation hard to $10^{15} ncm^{-2}$
  - Cheap process
  - Thinning to 50µm?
  - Smaller pixels for inner radii
- Require matching to readout electronics
  - Active pixels with built-in threshold or build readout on the chip ie FE-amplifier, discriminator…..

Electronics in the diode (smart diode array)



CMOS electronics placed inside the diode (inside the n-well)

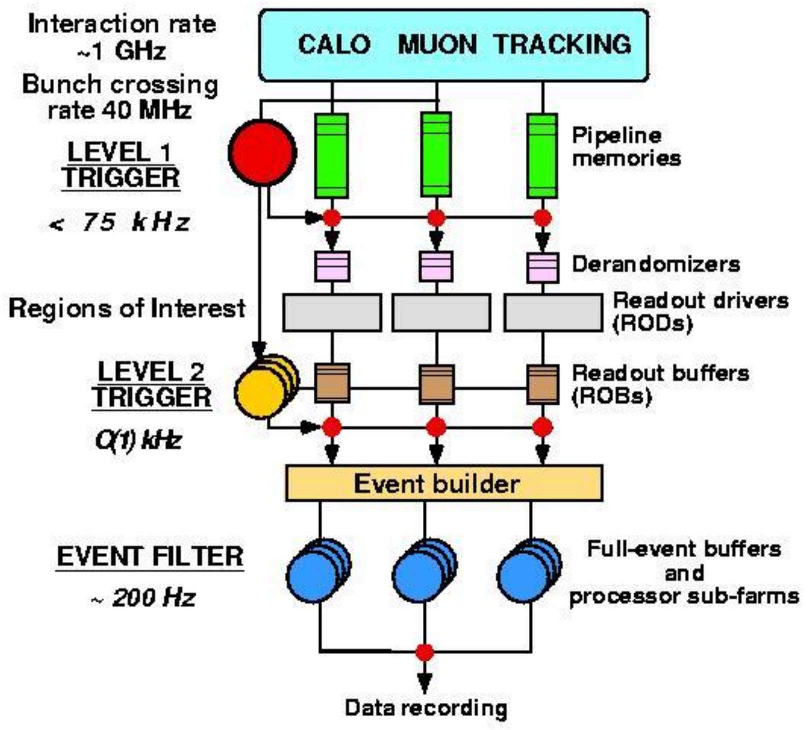
Data rates at $10^{34}cm^{-2}s^{-1}$



- Interaction rate ~ 1GHz
  Collision rate 20MHz in 2011
  (40MHz design)
  pileup ~20 events/collision
- Background $\sim 10^9$Hz
- Discoveries ≤ 1Hz
- $1:10^9$ defined by physics
- Event size 1.2-1.3MB
- Readout every bunch crossing ~50TB/s?
- Practical readout → ~200Hz (300MB/s)

Current trigger system

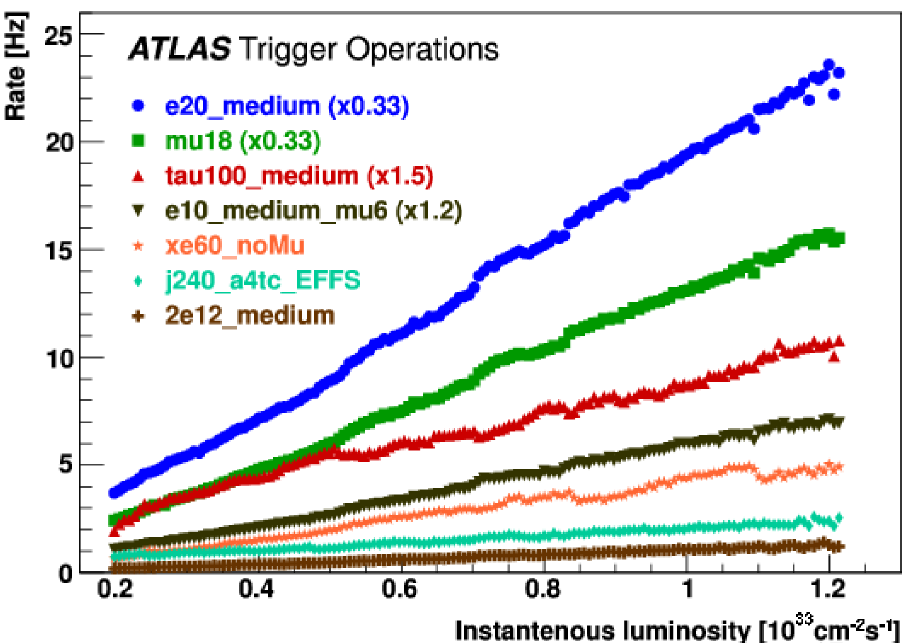
- Use trigger system to select interesting events for readout and reject uninteresting events
- L1 ASIC/FPGA
  - Analyse coarse grain information from muon and calorimeter system
  - Seed region of interest for L2
- L2 Software
  - Analyse full granularity in RoI ~2% of data
  - Algorithms for fast rejection
- EF Software
  - Full offline algorithms
  - Full event access
  - Seeds from L2



Triggering for the Upgrade

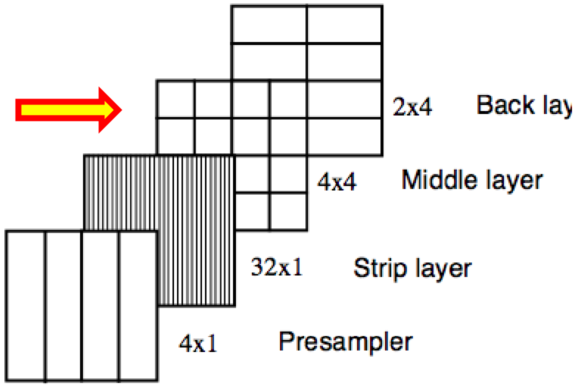
- Trigger rates rise linearly with luminosity
- Need to improve trigger algorithms to maintain low thresholds
  - Loss of acceptance ie low thresholds and good S/N → loss of physics
- L1 Calo
  - use fine-grain digital output from calorimeter
  - Allows improved algorithms
- Requires high speed processing
- UK-Programme
  - L1 calorimeter trigger (hardware)
  - L1 Track trigger (hardware)
  - High level trigger (software)

- Challenge for triggers in upgrade
  - Raise thresholds
  - Combine objects to focus on specific channels
  - But require single lepton channels to reduce trigger bias

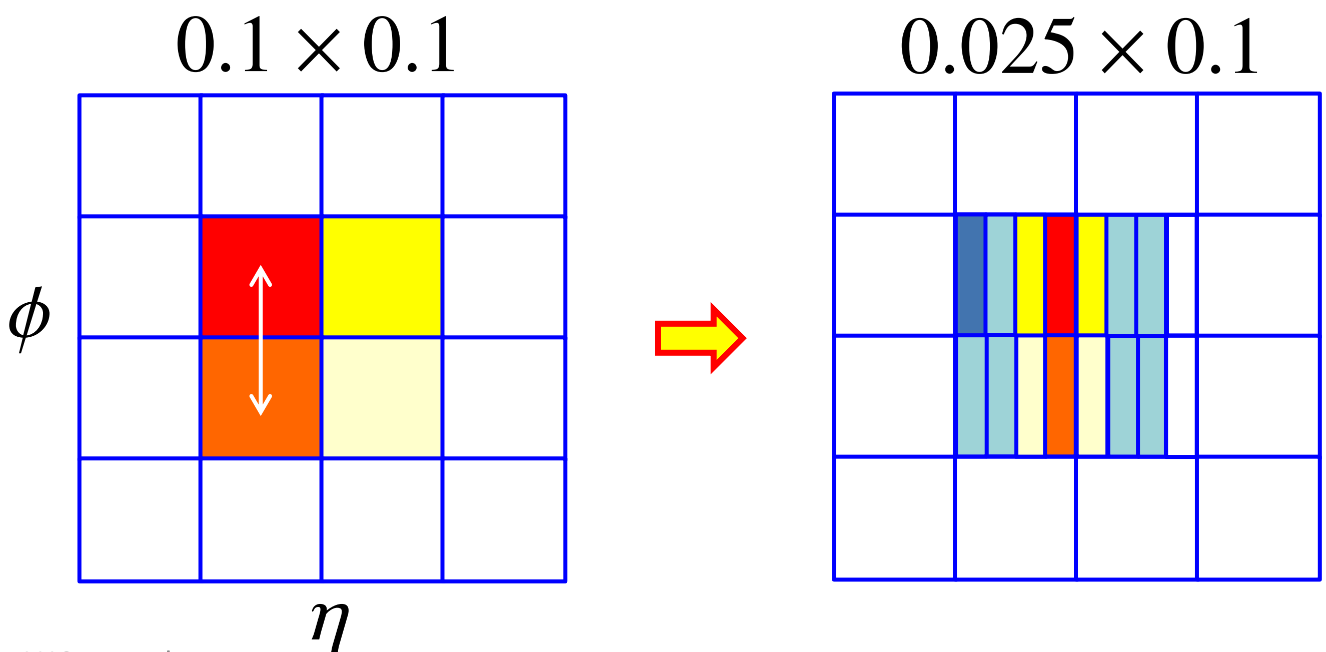


L1 Calorimeter trigger: Increased granularity

- Each 0.1 x 0.1 EM trigger tower is the analog sum of LAr sampling
- LAr move to digital trigger signals in Phase-I
  - increased segmentation
- Second sampling layer – most useful
- (still summed to 0.025 x 0.1)



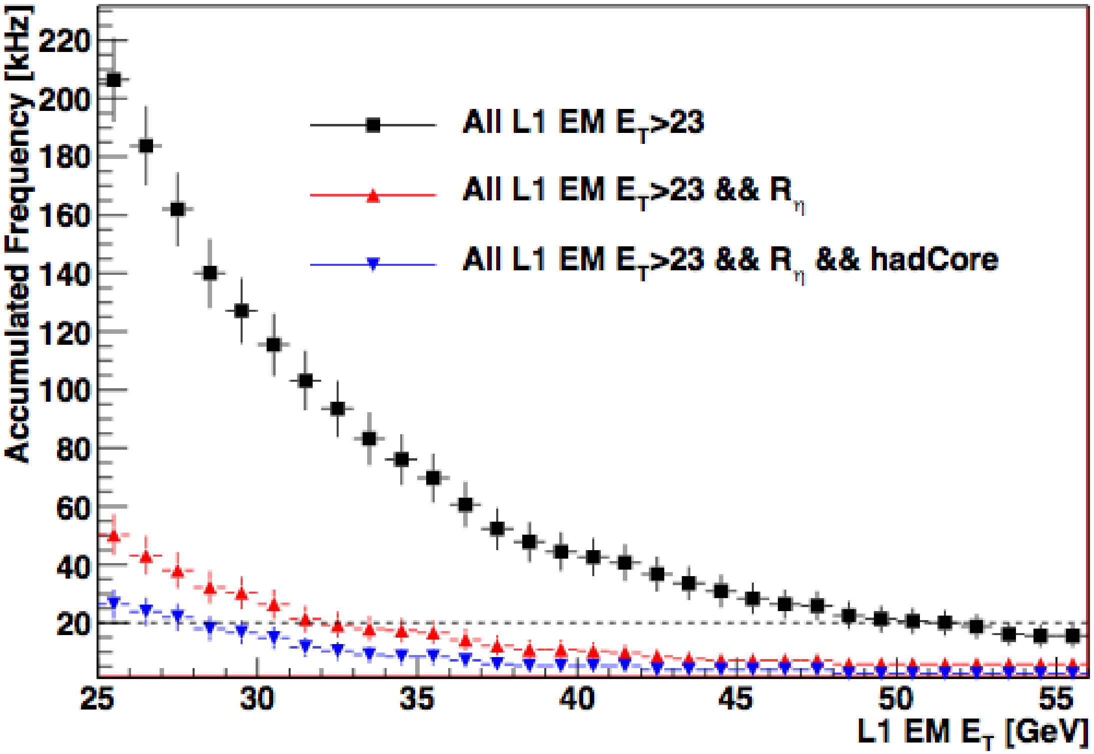
- Allows "HLT-like" algorithms at Level I – e.g. Ratio (3x2/7x2)



L1 Calorimeter trigger : Increased granularity

- Impact of use of Ratio (3x2 / 7x2) – use increased granularity in trigger algorithm

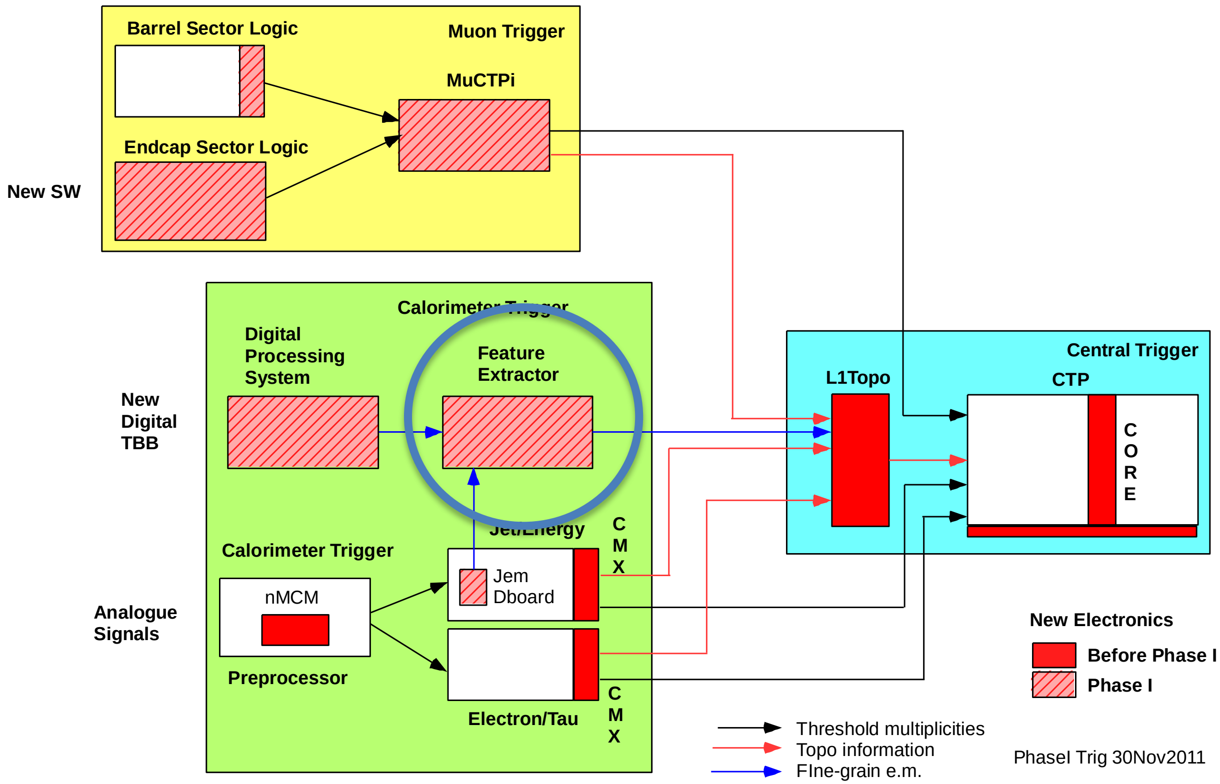
EM Rate (non isolated) Wigglesworth



- Factor ~2.5 reduction in rate for 96 % efficiency ← largest improvement
- Significant reduction in electron threshold possible

Phase I: L1 Calorimeter Upgrade

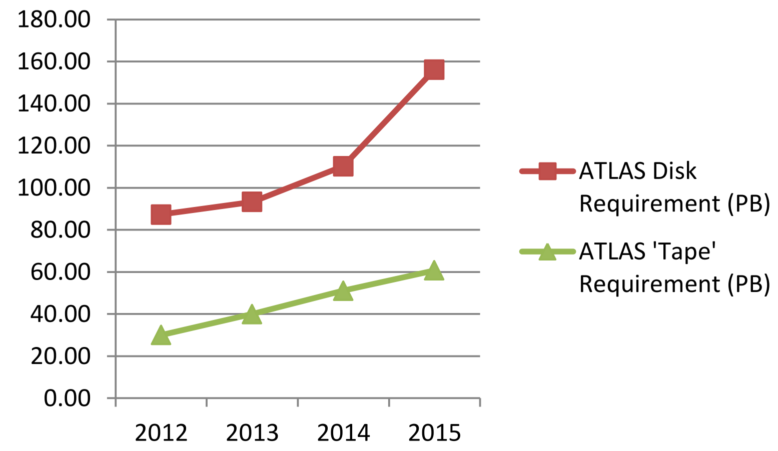
- Possible architecture for Phase I upgrade of L1
  - New LAr digital readout to trigger (Tower Builder Boards)
  - New electron feature extractor

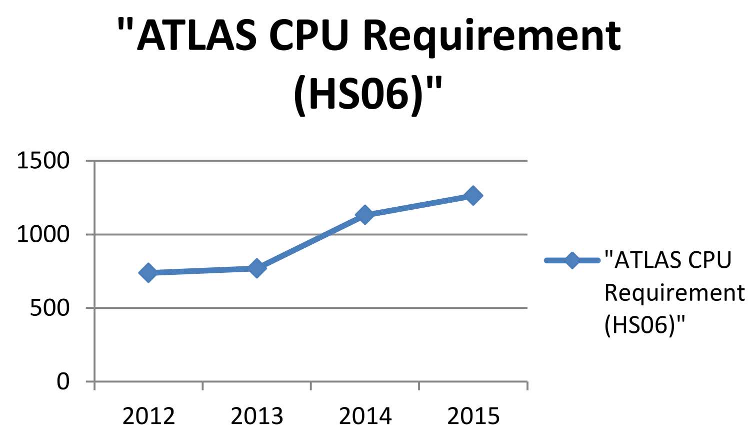


•Major upgrade – based on state-of-the-art FPGAs and very high speed real-time electronics 5-10 Gbps

Offline Computing: current ATLAS

- Offline computing already faces a continuing challenge
  - Increased data volume under analysis
- Increasing trigger rate to cope with increased beam intensity
- The upgrades will increase this pressure on resources

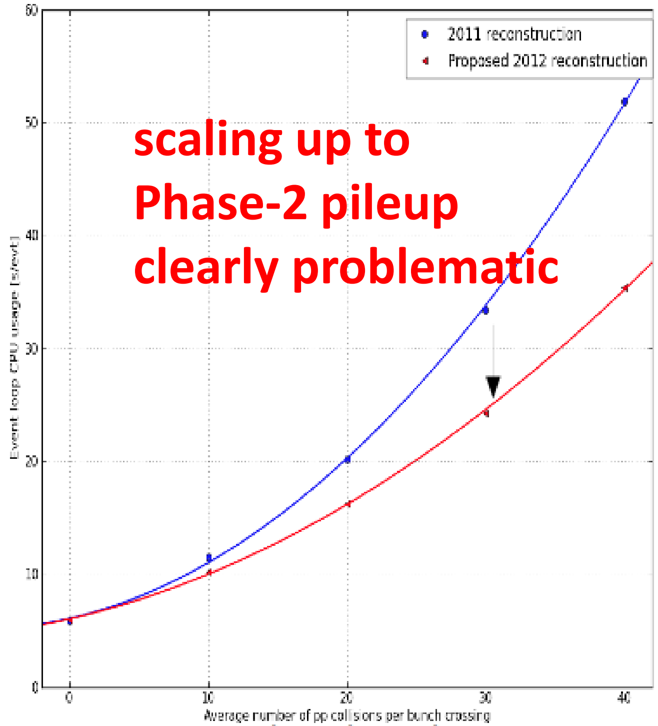




Further challenge: events get more complex and over-layed ("Pileup")

short wrap-up of release 17.2.

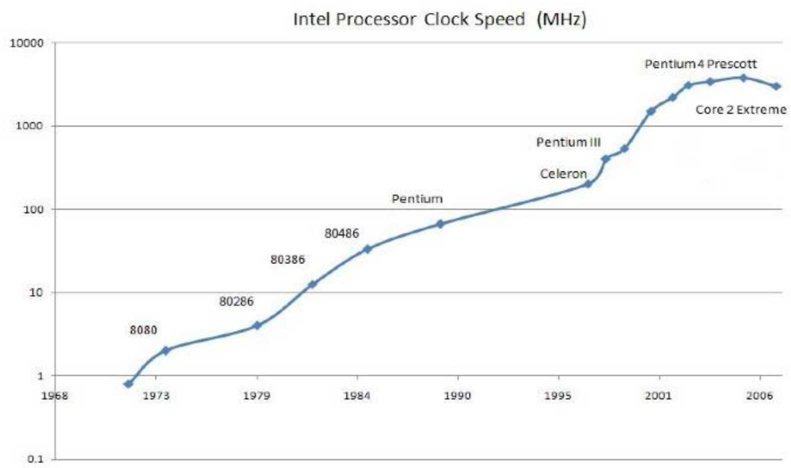
- hard work from various domains (PUTF, ID, Calo, etc) paid off, new release significantly faster at high pileup than last year's release with better physics output
- At mu=30 from 34s down to 24s !

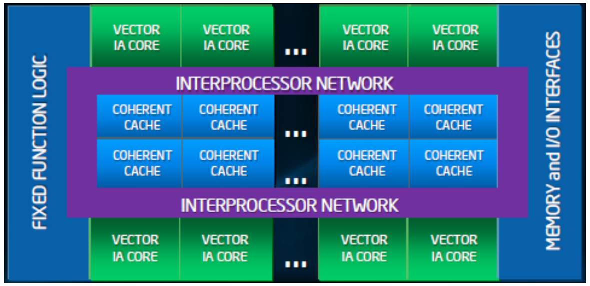


We'll have to see how well LHC will run, but we are at a good starting point.

Offline Computing Architectures

- Clock speeds have hit a plateau
- Moore's Law growth now comes through increasing core density
- Architectural changes
  - From multi-core to many-core
    - Coarse-grained parallelism (one event per core) does not scale
    - Tricks to share memory between concurrent processes being used, but have limits at about 32 cores
    - Deeper parallelism required in our algorithms
  - Co-processors (or more likely GPU onboard)
    - Efficient usage requires vector applications and local data to be identified and passed over
  - Languages again become an issue
    - The best is not the most standard
- New workflow/frameworks/coding required



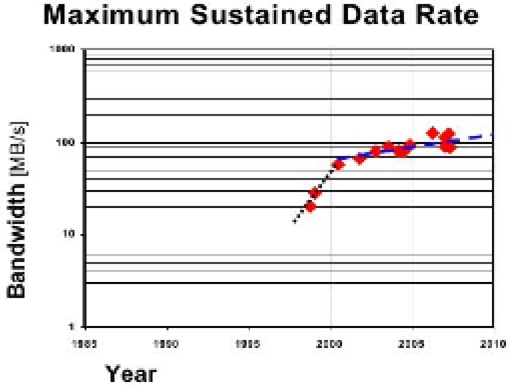


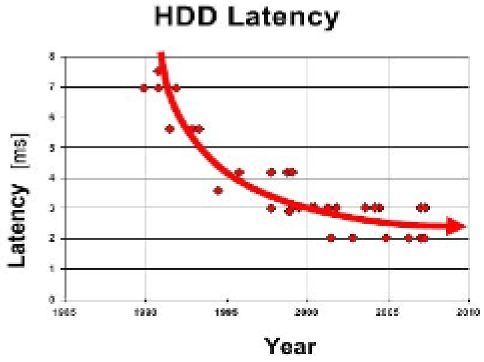
IO & Storage Challenges

- Asynchronous writing from many cores requires a stronger IO model
    - process chunks of events, not single events
    - Avoid merging bottlenecks
    - May require ability to write sequence of files because input size is large

- Also hardware scaling issues

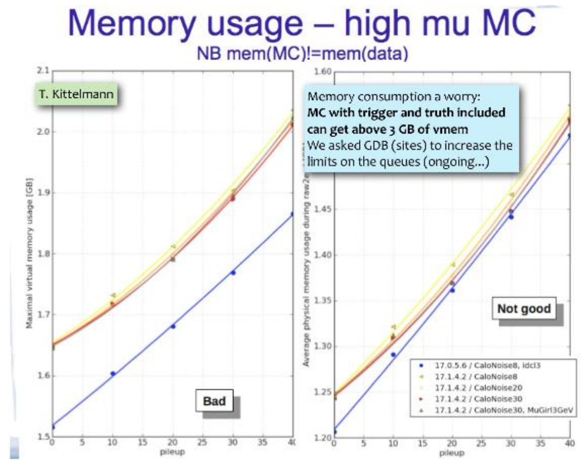
- IO and IO/$ are also not scaling
- Hard to see path past 1TB/in^2





New IO frameworks, new storage models!

Example of software changes needed: Tracking

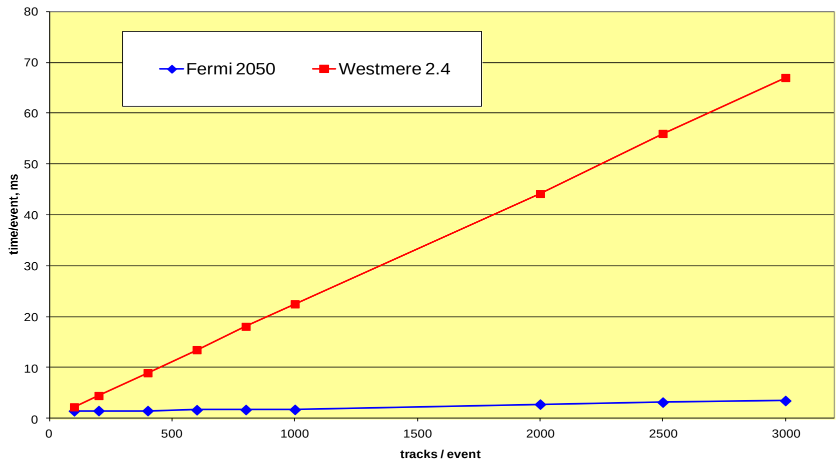


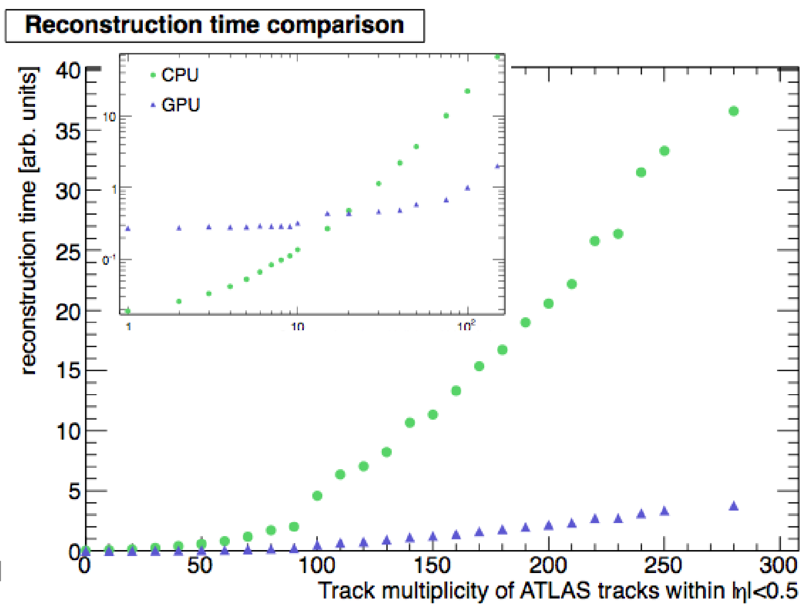
- resource needs scale fast
  - tracking will be (the) main resource driver
- global optimization
  - requirements on tracking evolved already with physics program
  - different luminosity regimes lead to different **working points**

2009 / early 2010	commissioning Min.Bias	pt > 50 MeV open cuts, robust settings min. 5 clusters
2010 stable running < ~4 events pileup	low lumi physics program (soft QCD, b-physics, ...), b-tagging...	pt > 100 MeV min. 7 clusters
2011 pp running ~11 events pileup	focus more on high-pt physics (top, W/Z, Higgs), b-tagging...	pt > 400 MeV, harder cuts in seeding min. 7 clusters
Phase 1 upgrade including IBL 24-50 events pileup	high-pt physics, study new physics (I hope), b-tagging....	pt > 900 MeV, harder tracking cuts, min. 9 clusters
SLHC up to 150-200 events pileup	replace Inner Detector to cover very high luminosity physics program	further evolve strategy... R-o-I or z-vertex seeding, reco. per trigger type, GPUs

Use of GPUs in High Level Trigger (&offline)

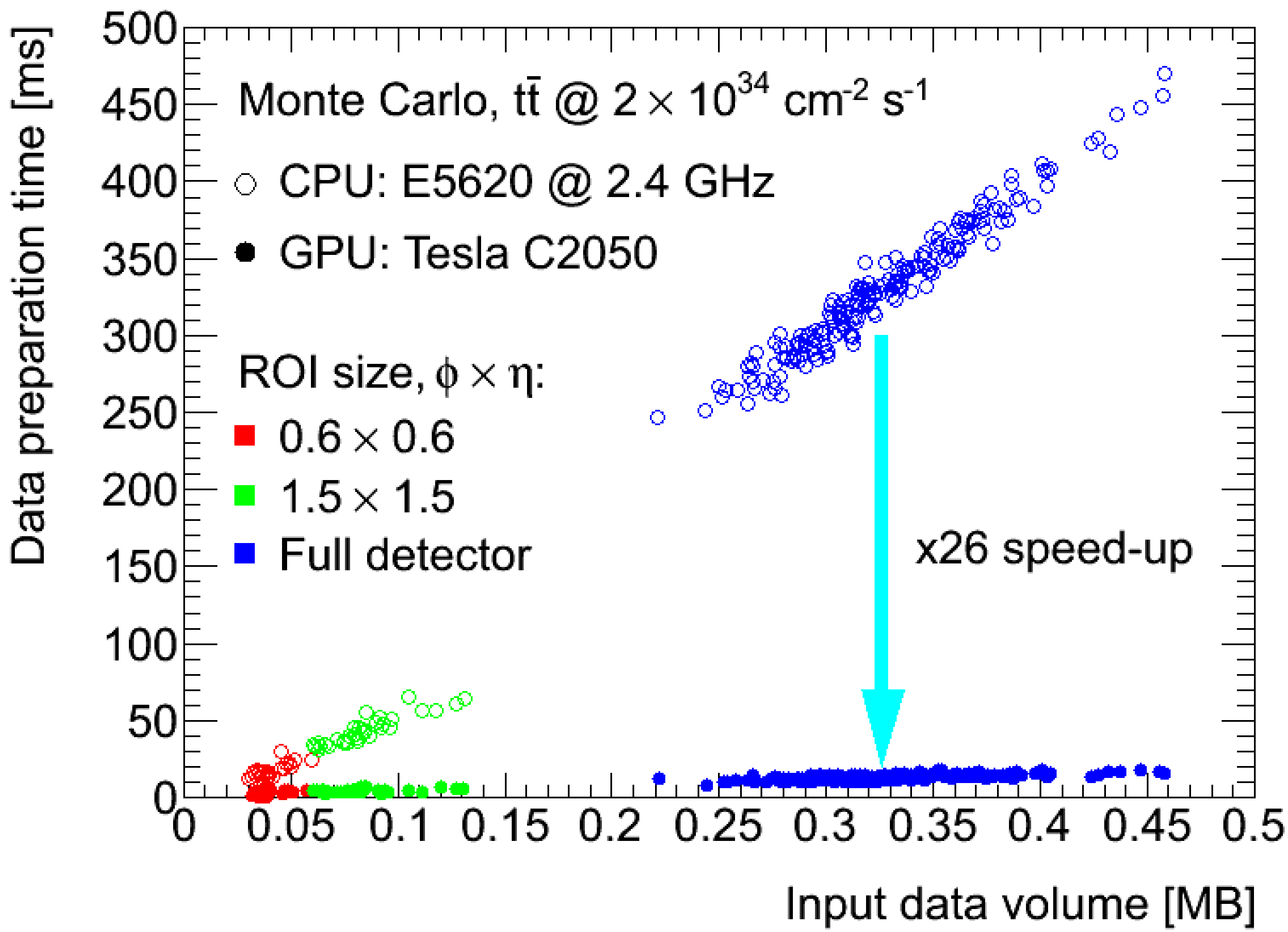
- New ideas – GPGPUs
  - Suitable for some tasks, but power hungry
  - May be particularly suitable to trigger system
  - Coding lessons can help many-cores too
- Ported HLT algorithms to GPU:
  - Zfinder
  - Track Fitter
- Improvement of offline reconstruction
  - Kalman filter



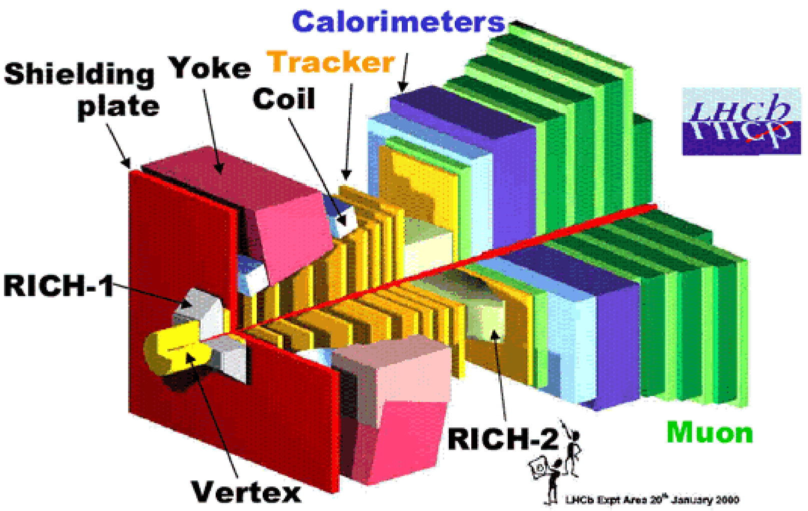


GPU-based Level 2 Data Preparation

- Full data preparation chain (bytestream->hits->spacepoints) test



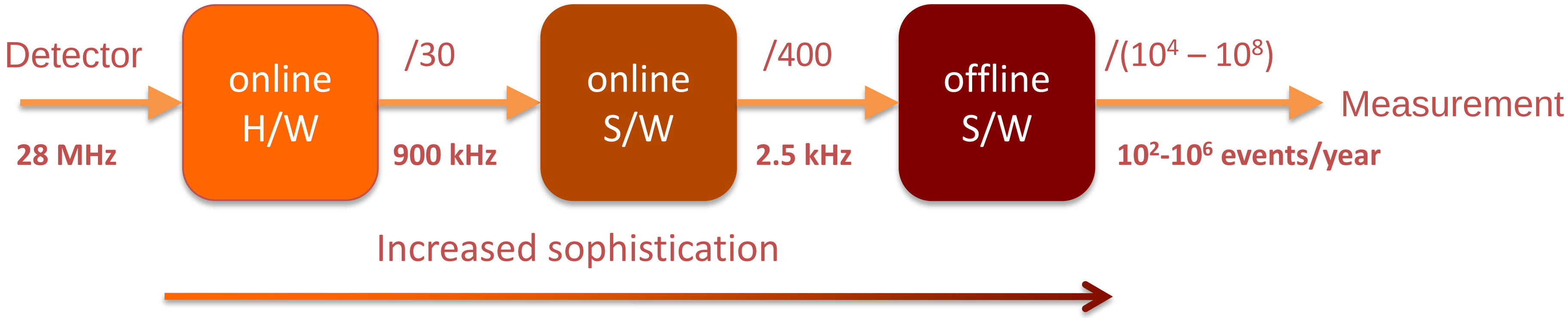
The LHCb Vertex Locator (Velo)



- Single hit resolution 4µm
- Vertex resolution:
  - $\sigma_x \sim \sigma_y = 13\mu m$; $\sigma_\mu = 70\mu m$
- Proper time resolution:
  - $\sigma_\tau \sim 50fs$

LHCb Event selection

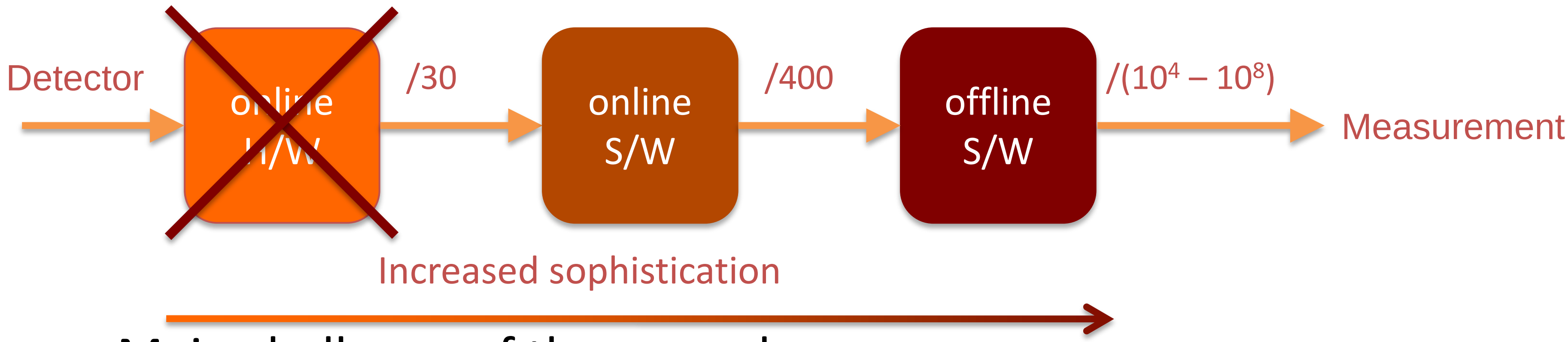
- Signal events are enhanced in several steps
  - Based on many different properties of the event



- Characteristic property of B mesons
  - ‘Long’ lifetime compared to background
  - Flies ~1 cm before decaying
- Select events with displaced decay vertices

LHCb: Changing the trigger strategy

- Not enough information to identify signal events in H/W trigger
  - Need decay vertex and momentum information
  - Remove first level hardware trigger



- Main challenge of the upgrade
  - Processing and reading out all the data
  - Require intelligent readout chips capable of zero suppression and possibly clustering
  - High-rate links ~5GB/s both over wire and optically

Summary

- LHC Upgrade will require handling high data rates at different levels of the experiment
  - Tracker: pixel sensor with high granularity for low occupancy and high resolution
    - Hybrid pixel sensors: high density readout electronics, interconnect technologies, large area, high fill factor
    - 65nm & 3D technologies for readout chips
    - HV CMOS based APS for thin intelligent sensors
  - Trigger: Hardware level, multi-GHz boards, use of latest FPGAs
  - Trigger: Software: use of GPUs for fast pattern recognition
  - Computing & software: development of new architectures
- Thanks to Lars Eklund, Dimitry Emeliyanov, Norman Gee, Roger Jones for input