Development of a technological prototype of Silicon-Tungsten electromagnetic calorimeter for ILD

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on behalf of the ILD SiW-ECAL development group

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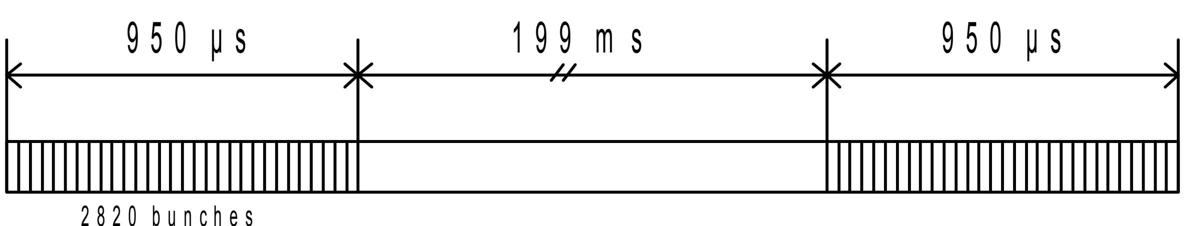
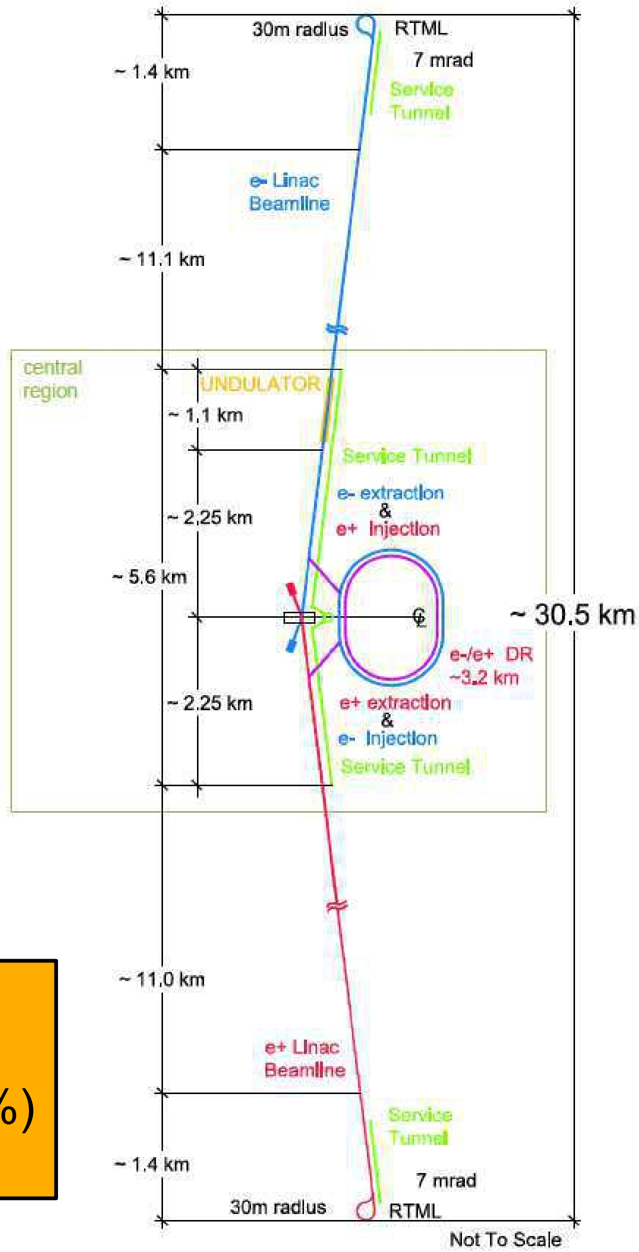
Grant ANR-2010-0429-01

ILC parameters

Max. Center-of-mass energy	250–1000 (90)	GeV
Peak Luminosity	0,8–3x10^{34}	1/cm^{2}s
Beam Current	5.8	mA
Repetition rate	5	Hz
Average accelerating gradient	31.5	MV/m
Beam pulse length	0.95	ms
Total Site Length	31	km
Total AC Power Consumption	120-300	MW





- Time between collisions : 350–700 ns
- Trains of 1300–2700 Bunches
- Low detector occupancy
- Low bgd : $e^+e^- \rightarrow qq \sim 0.1$ / BC
  $\rightarrow \gamma\gamma \rightarrow X \sim 200$ / BX

- High B field
- Trigger-less
- Power Pulsing (≤1%)
- Differed readout

Constrains on detectors:

Basis: sep of H → WW/ZZ → 4j

- $\sigma_Z/M_Z \sim= \sigma_W/M_W \sim= 2.7\% \oplus 2.75\sigma_{sep}$

⇒ σ_E/E (jets) < 3.8%

- Sign ~ S/√B ~ $(\text{resol})^{-1/2}$
  60%/√E → 30%/√E ⇔ +~40% L

Large TPC

- Precision and low X_0 budget
- Pattern recognition

High precision on Si trackers

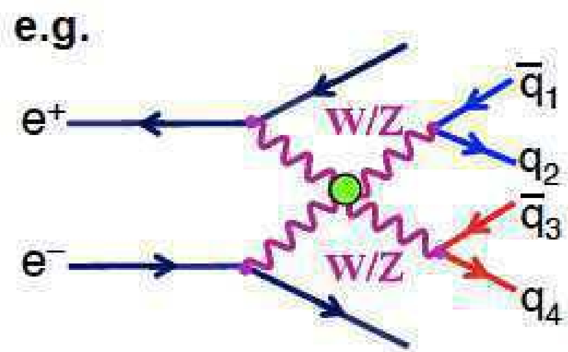
- Tagging of beauty and charm

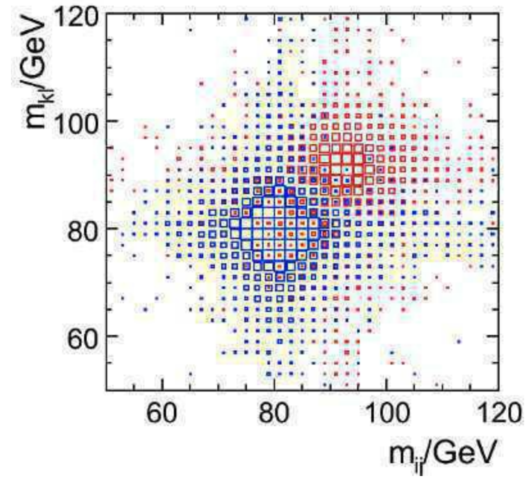
Large acceptance

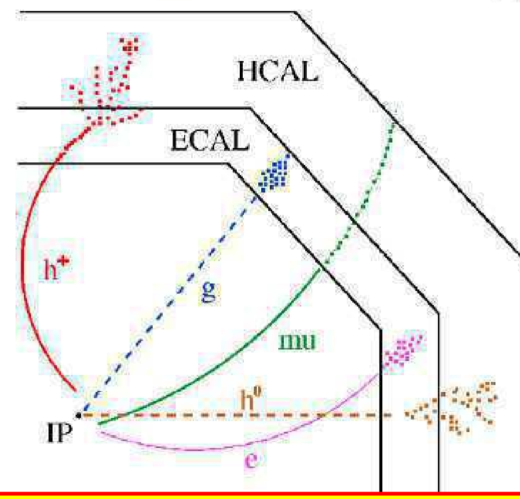
Fwd Calorimetry:

- lumi, veto, beam monitoring

Imaging Calorimetry





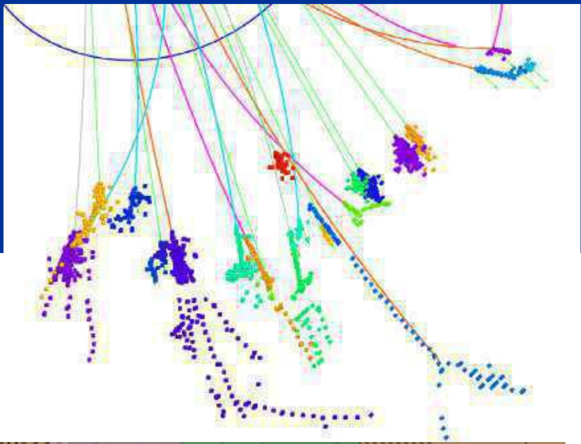


Particle Flow Algorithms :

- Jets = 65% charged + 25% γ + 10% h^0
  Tracks / ECAL / CALO's
- TPC $\delta p/p \sim 5\cdot10^{-5}$; VTX $\sigma_{x,y,z} \sim 10$ µm

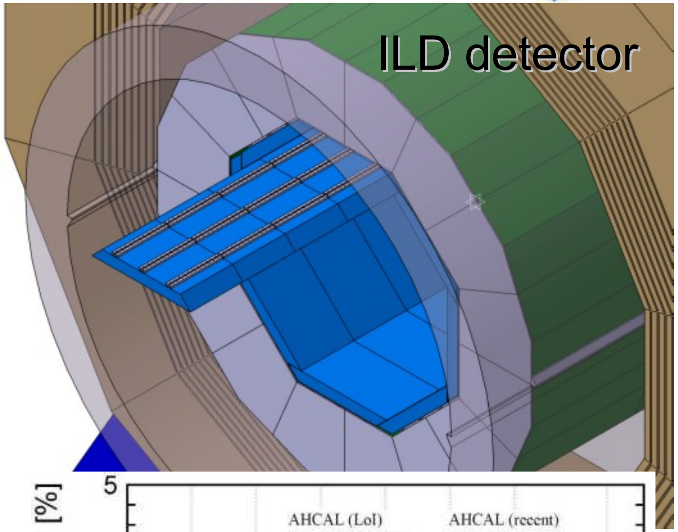
H. Videau and J. C. Brient, “Calorimetry optimised for jets,” in Proc. 10th International Conference on Calorimetry in High Energy Physics (CALOR 2002), Pasadena, California. March, 2002.

Imaging Calorimetry



Imaging Calorimeters 1000× current granularity

- wrt LHC: data rate ↘↘ but embedded electronics
- Pattern recognition **see Naomi van der Kolk Poster**

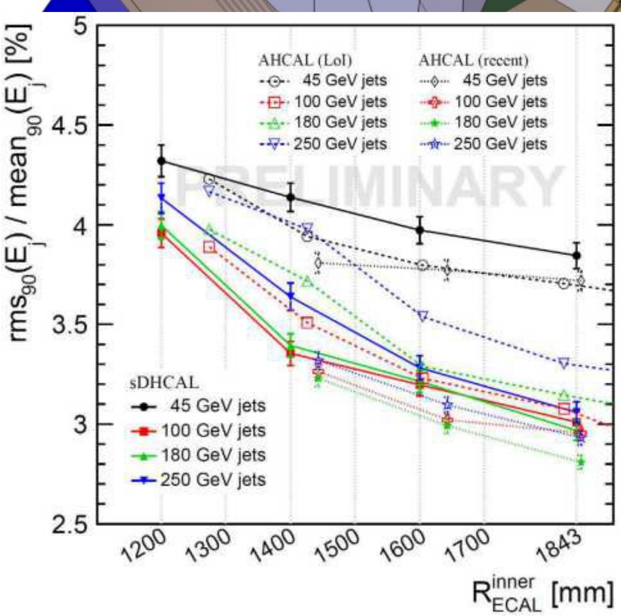


Needed R&D:

- Dimensioning, Mechanics (uniformity), Sensors, Electronics, VFE, Power Consumption, Thermal dissipation & uniformity
- Iterative construction & test of Prototypes
- Detector & Integration
  - Optimisation : Physics vs cost, services (PP, cooling)

Dedicated SW tools for PFA:

Difficulty : perf in JER = HW ⊗ SW



SiW ECAL: Physics & Technological prototype

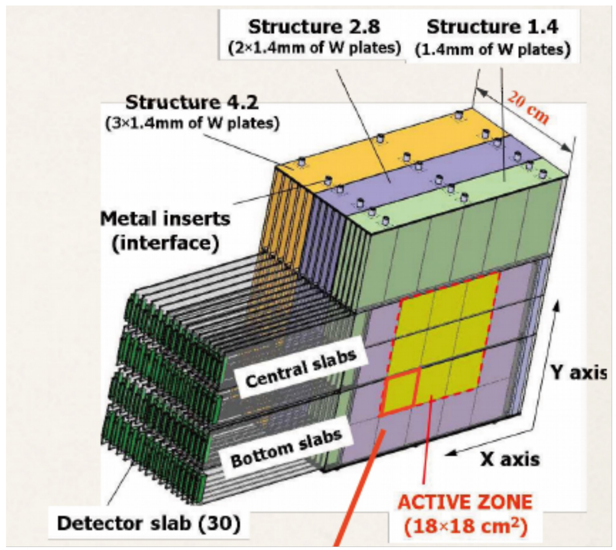
Physics prototype: 2005-2011

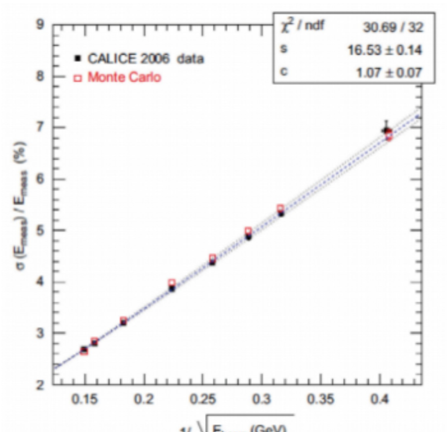
PFA proof of concept with comparison to MC (PandoraPFA etc.)

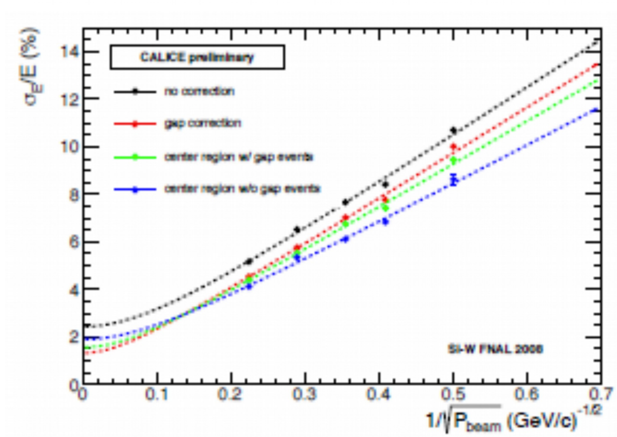
Electronics outside

- 1cm x 1cm pixels
- full 30 layers

(used for PAMELA sat.)

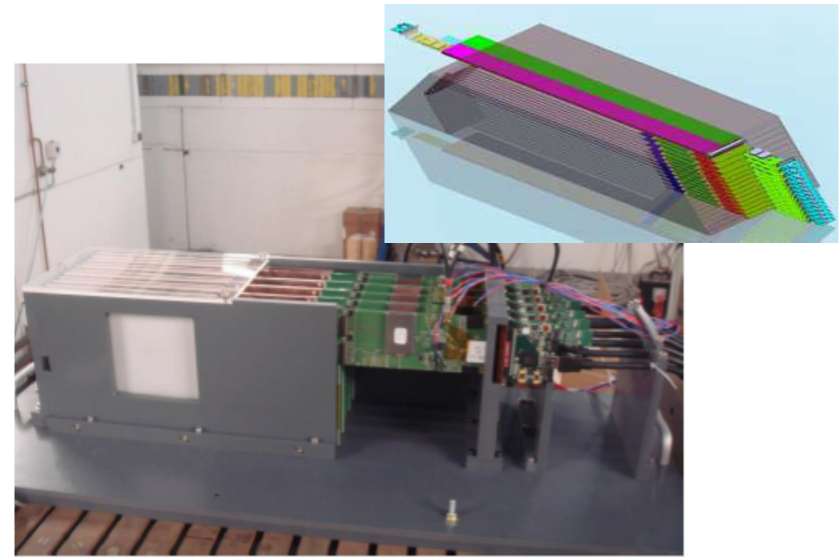






16.5%(stochastic) 1–2% (constant) obtained with 1–45 GeV e⁻/e⁺ at 2006/2008 BT

Technological prototype



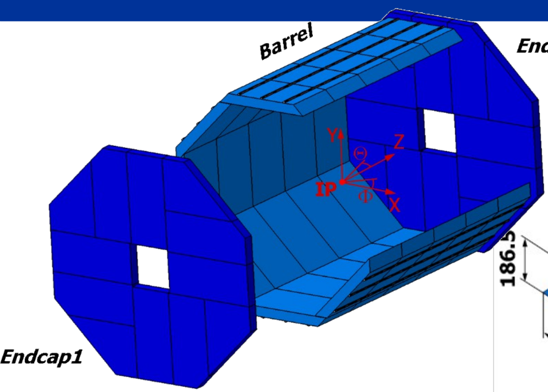
Embedded electronics

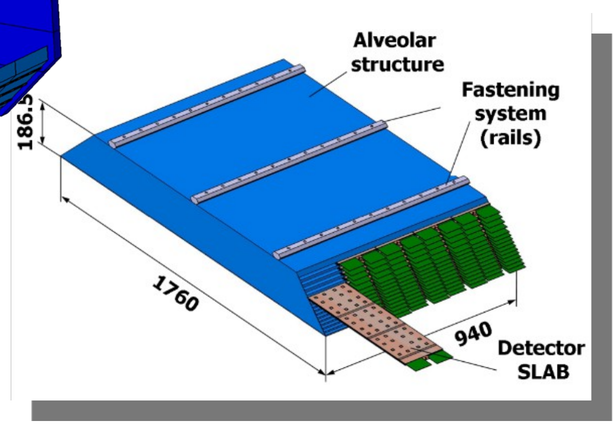
- SKIROC2 analog/digital ASICs
  - auto-triggered, zero suppr., PP
- pixels 5×5mm^2

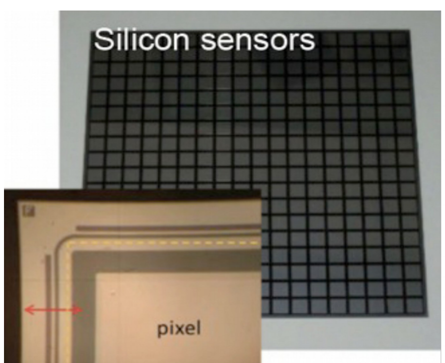
Assess the feasibility

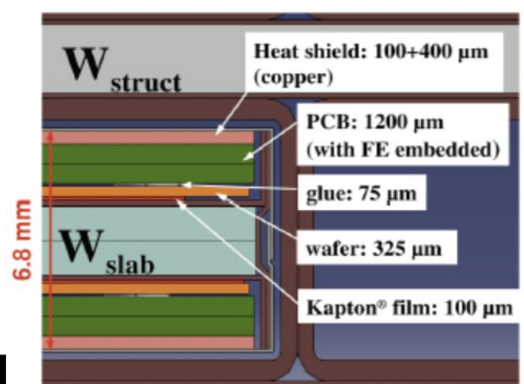
Establish procedures and develop test benches for mass production

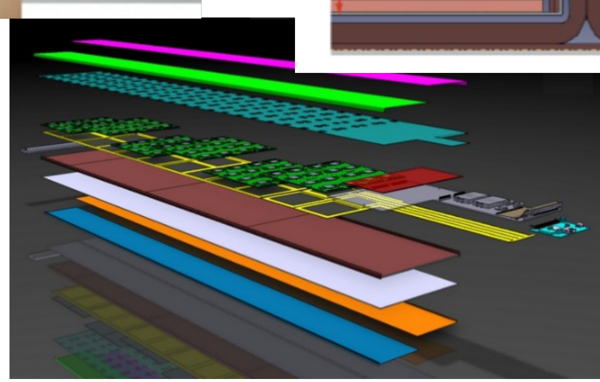
The SiW-ECAL of ILD







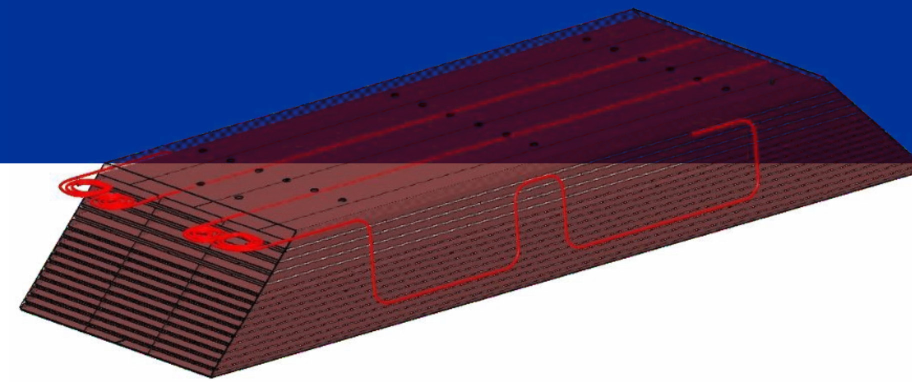




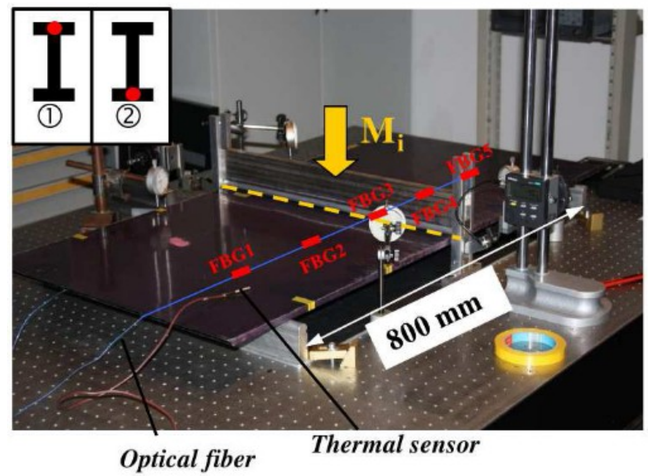
On going R&D

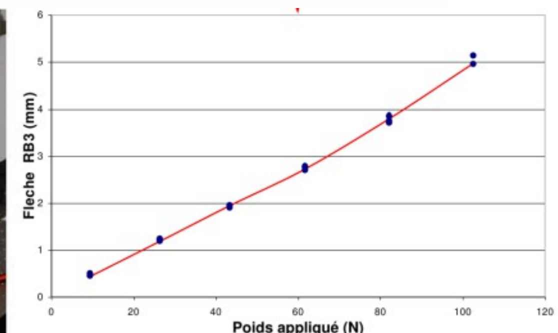
- Thermic & Mechanical studies
  - Production, Characterisation & Monitoring
  - Thermic simulation & cooling
- Assembly: Quality tests & preparation of large production
  - VFE, PCB's, ASU's
  - TB, Cosmics, Charge injection
- Wafers:
  - Guard Ring Studies → CALIIMAX program
  - Characterisation
    - Charge injection by Laser
- DAQ (see Frank Galstaldi talk's)
- Power consumption (not here)
- Optimisation: Cost → reduction of radius

ECAL : Composite Structure (barrel)

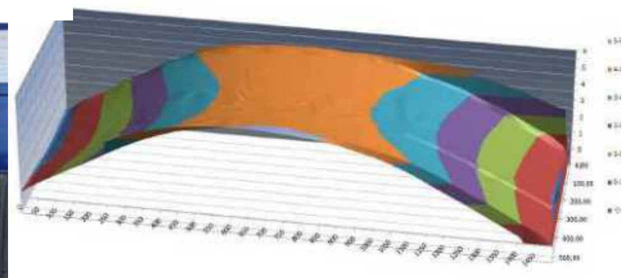


- Carbon Fiber + Tunsgten
  - Prod : dec 2011 (5 yrs of R&D)
  - 600kg, 15 layers
- 15 alveoli produced, 1 faulty
- 1 equipped with Fiber Bragg-Gratted (FBG)
  - ⇒ Comparison calculation and measurement
- Assembling mould
  - Cooking in autoclave
- Metrology
  - Minor on-side deformation



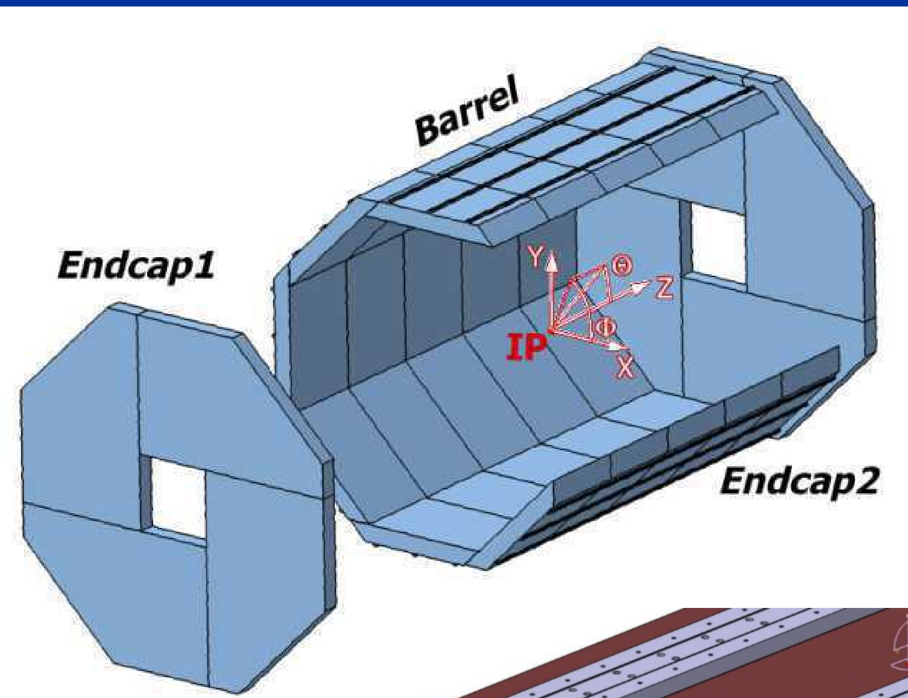


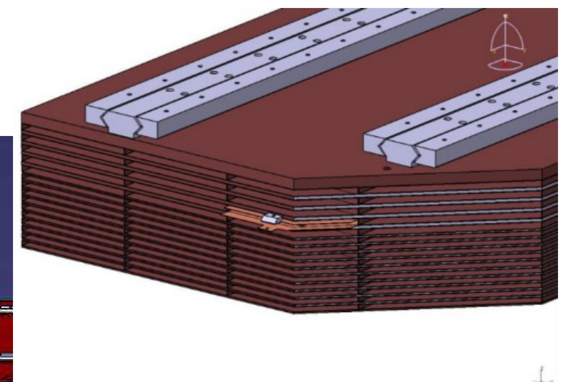
Vérification des paramètres du modèle en comparant la flèche FBG3 mesurée et simulée

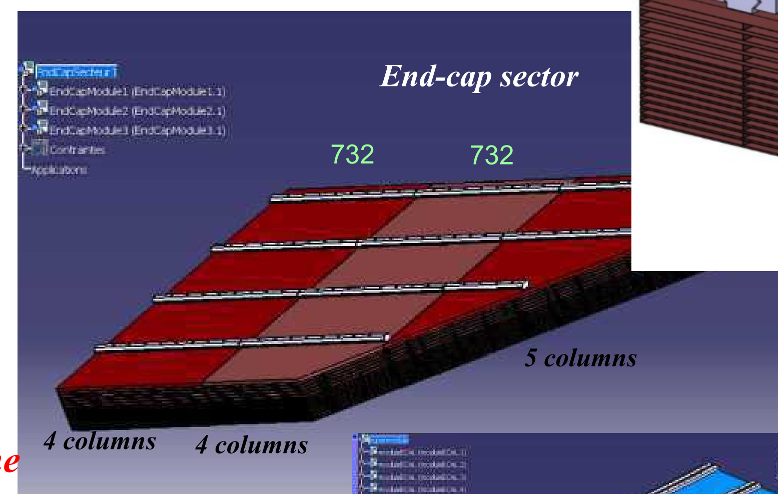


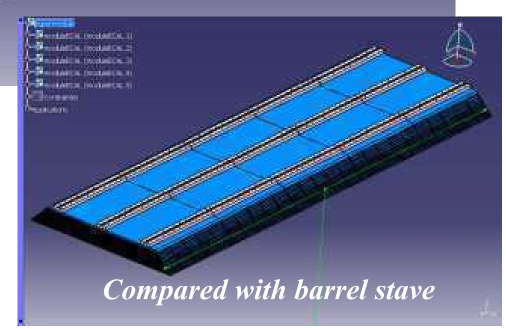
ECAL structure

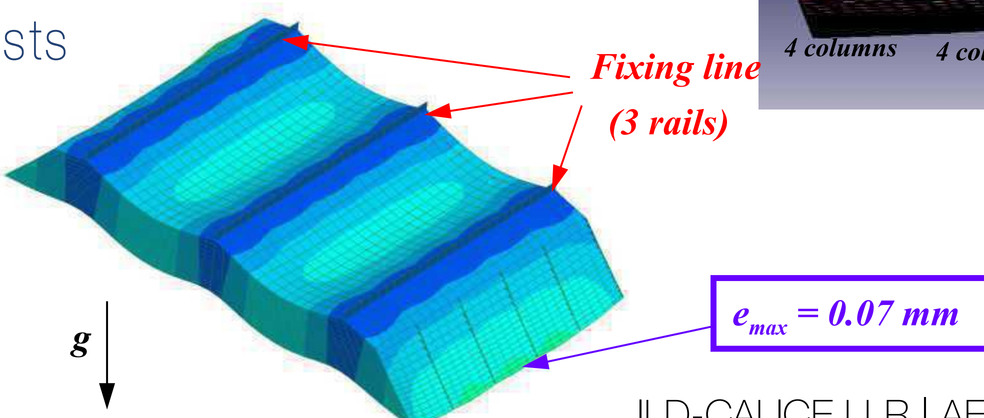
- Barrel: 5 octogonal wheels
  - R_{min} = 1808 mm; R_{max} = 2220
  - Width = 940mm
- End-caps: 4 quarters
  - $\varnothing_{min}$ = 800 mm
- Carbone / Tunsgten structure
  - filled with Si or scintillators (option MAPS/DECAL)
- Extensive mechanical simulation & tests







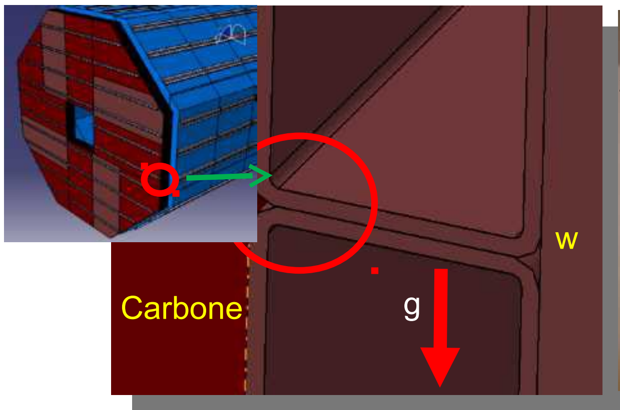


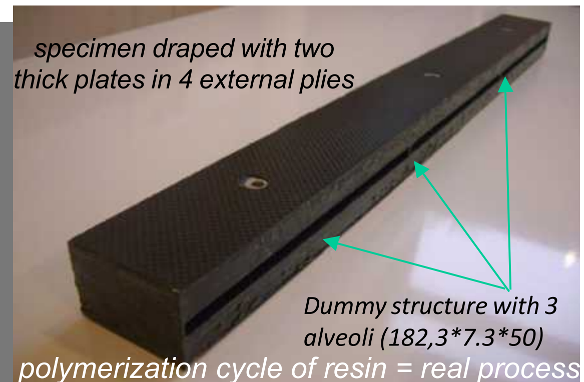


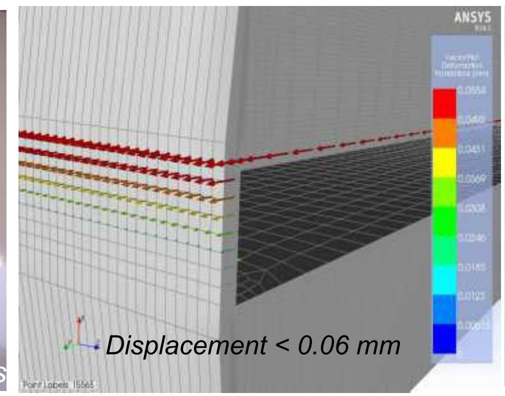
Evolution of skin thickness for Endcaps

Correlation of FEA simulations / shearing tests of representative structure

Problem of bending stress of alveoli skins / evolution of external plies







Influence of modification of external ply thickness on the first main constraint of external and internal walls

If external plies thickness increases => **Impact** on ECAL dead zone => Optimization of deflection values

Displacements	~0.1 mm vs 0.5mm for fatigue shearing tests ...
Main contraints	< 159 Mpa *both*
Shearing constraint	11.5 Mpa vs **6** (1,8/wall) Mpa for shearing tests ...

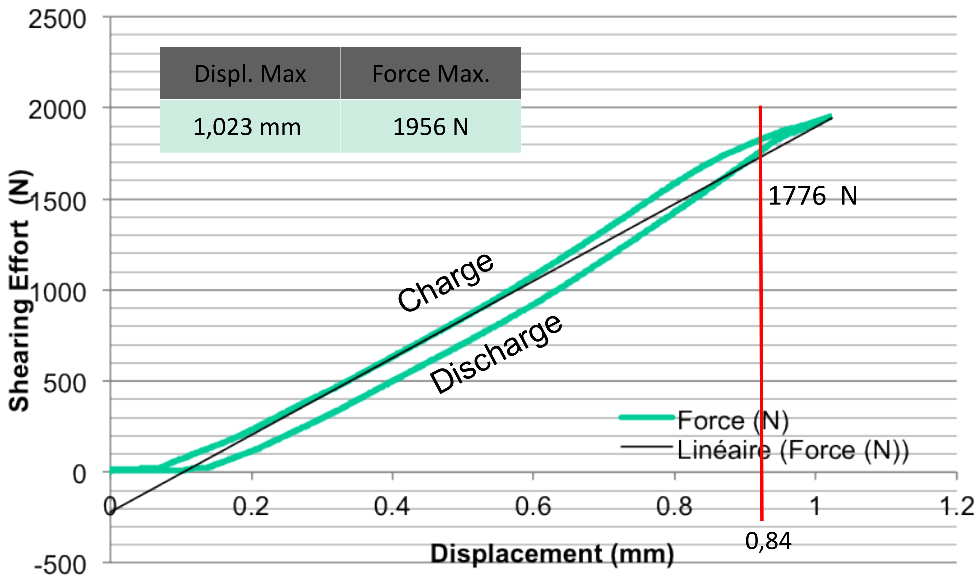
From simulations to shearing tests
(ANSYS APDL / SAMCEF / ANSYS ACP)

Tests & simulations to be performed

- Adapt FEA parameters to simulate the whole structure / shearing results
- Destructive test on a existing structure *(demonstrator -EUDET)* / verification of bonded structures
- Process: increase intercoat adhesion with structural adhesive film
- Process: obtaining reliable thicknesses of walls *(specific long moulds, tooling development)* / Draping optimization
- Reliability tests: good & uniform impregnation of parts, good compacting
- Resistance of End-Caps to earthquake
- "Mass" production conception *(ply book enhancement, tooling, process)*

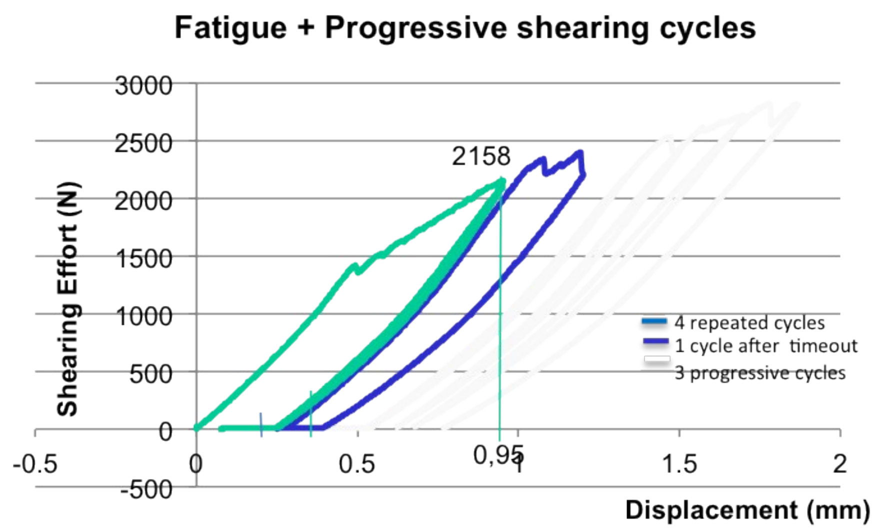
ECAL End-Caps: shearing tests

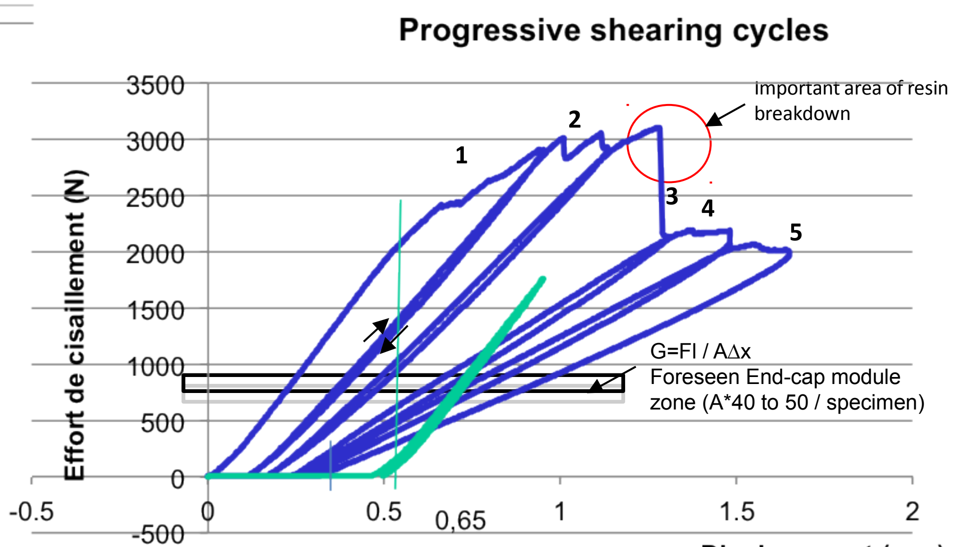
Monotonic shearing test



safety factor: s = 3.2 with respect to the stress induced / largest module (2,5m–25,5 kN) to be improved / “seismic issues” ILD’13 meeting in Cracow

Destructive tests with charge & discharge cycles / *hysteresis & weakening of the structures (resin) during repeated stresses*





Reduction in stiffness predictable during integration

(G# 85 MPa to 74 Mpa)

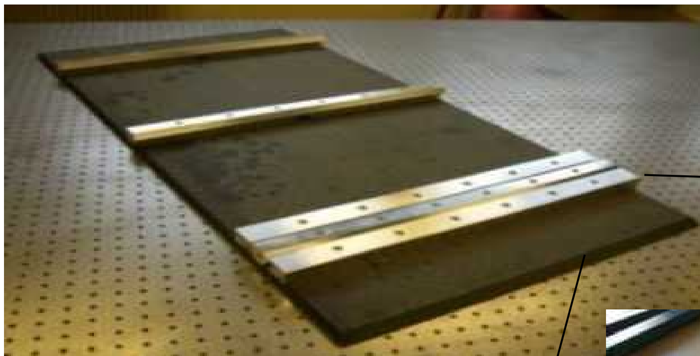
Stay < Δx = 0.35 mm (mechanical limiters) or

Increase No. of envelope folds (/ seism)

Max. admissible flexion value of slabs to be confirmed

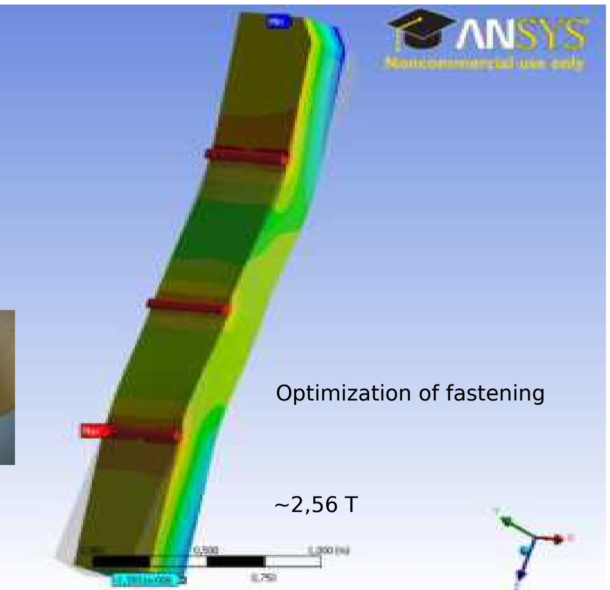
To be continued in 2014

Fasting system (on HCAL)



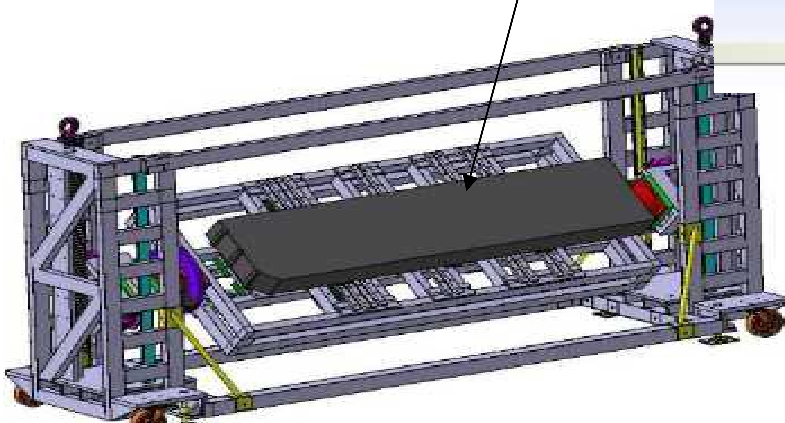
EUDET Carbon HR plate
13 mm with metallic inserts

to Carbon HR Rails



Optimization of fastening

~2,56 T



Building on going of transport and handling tools for integration & tests

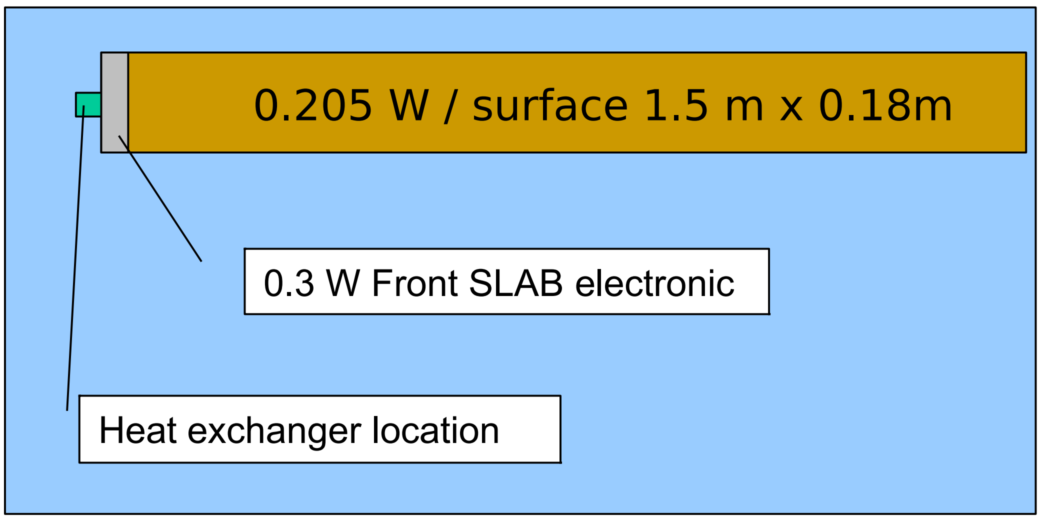
Mechanical structure of frames

Thermic Studies & Cooling

Power dissipation : Final goal with power pulsing 1/100 s

For ½ SLAB from barrel
Wafers consumption : 0.205 W
Front SLAB electronic : 0.3 W

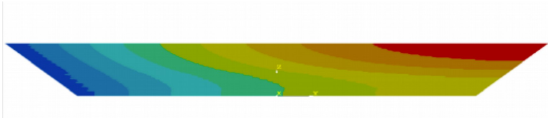
Ecal detector : 4.5 kW



Passive cooling : OK

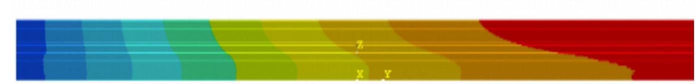
… support up to 10x bigger heat load (for details see backup)

Barrel : (1.5m)



ΔT = 2,2°C

End Cap : (2.5m)



ΔT = 6°C

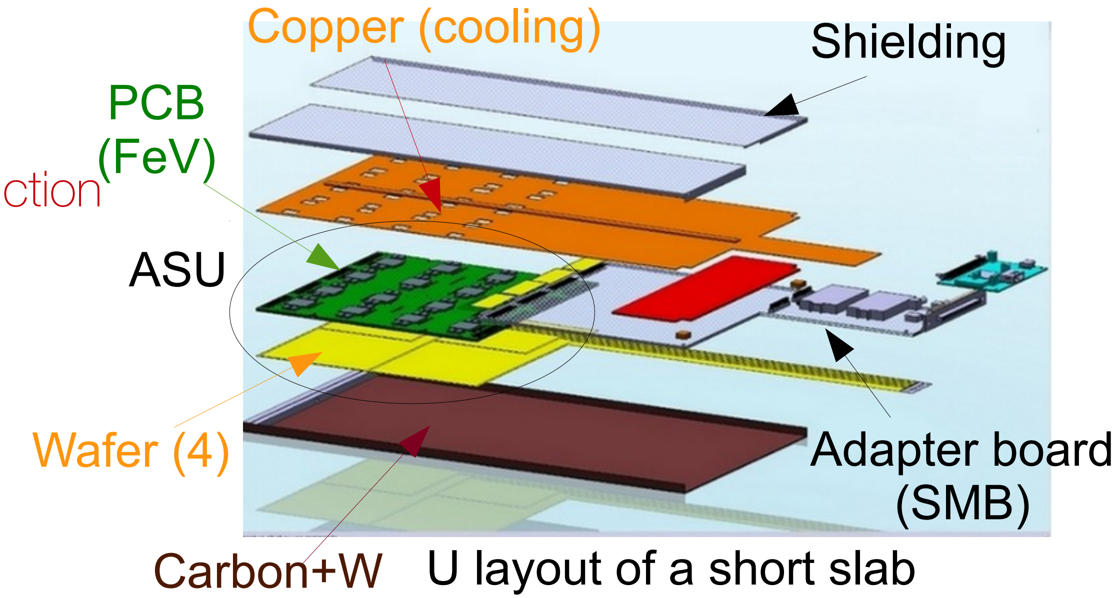
SLAB Assembly: full chain

R&D for "mass production" and QA

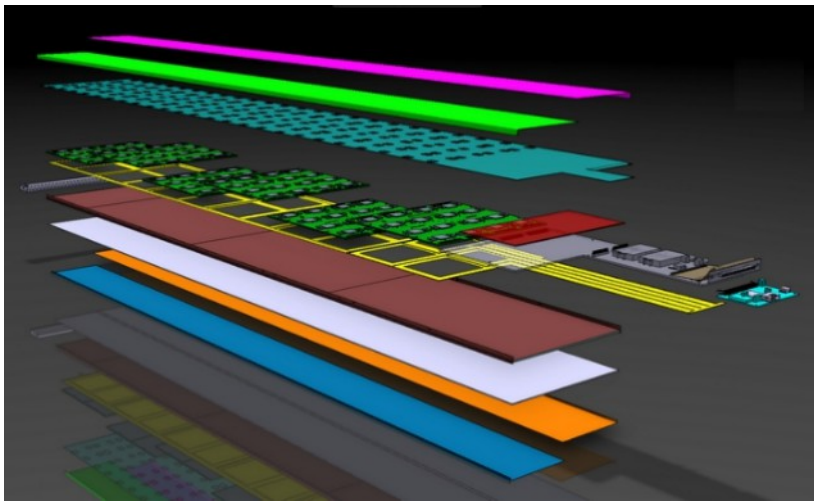
- Quality tests & preparation of large production
- Modularity → ASU & SLABs
  - Choice of square wafers (≠ from hex: SiD, CMS HGCAL)

Numbers (R_{ECAL} = 1,8 m, $|Z_{Endcaps}|$=2,35m) (likely to be reduced by 30–40%)

- Barrel modules: 40 (as of today all identical)
- Endcap Modules: 24 (3 types)
- Slabs = 6000 (B) + 3600 (EC) = 9600
  - many ≠ lengths
- ASUs = ~75,000
  - Wafers ~ 300,000 (2500 m^2)
  - VFE chips ~ 1,200,000
  - Channels: 77Mch



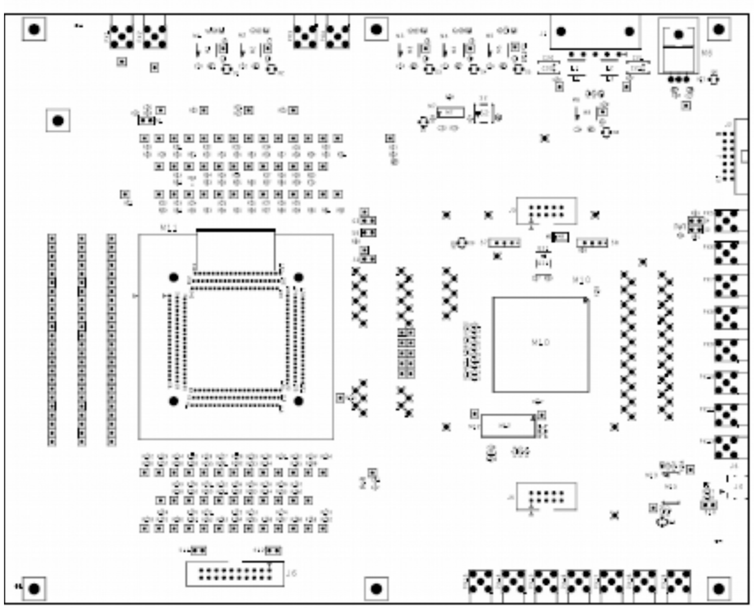
U layout of a short slab


U layout of a long slab

ASIC tests w/ testboards

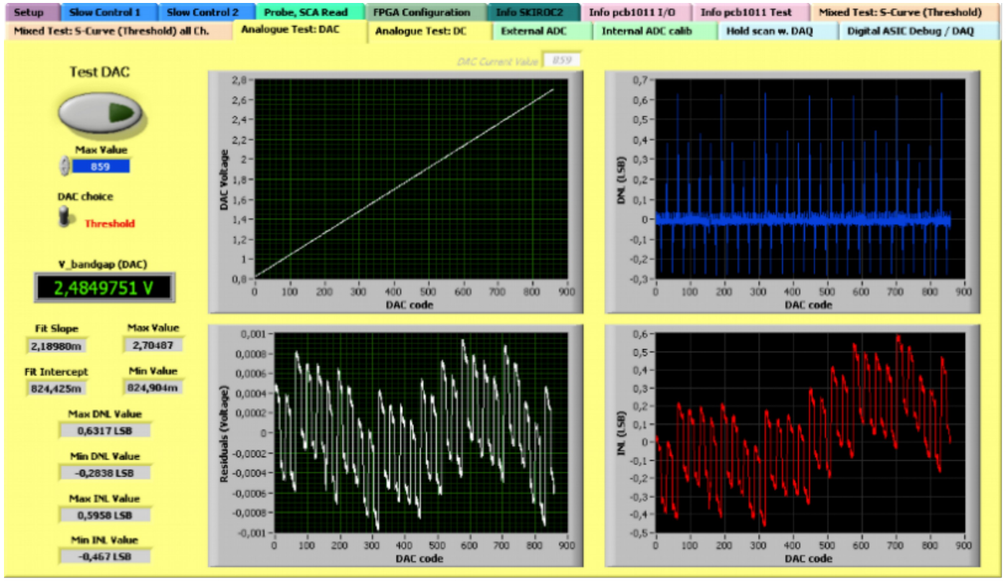
SKIROC2 VFE Chip

- 64ch readout/chip
- preamp + 2 shapers
- Auto-trigger
- 15 cell analog memory
- 14 bit ADC



SKIROC2 test board

- No detector, input holes
- Analog/digital tests
- Automated test software with Labview ⇒ caracterisation
- Small crosstalk found



See Ch. de la Taille's talk

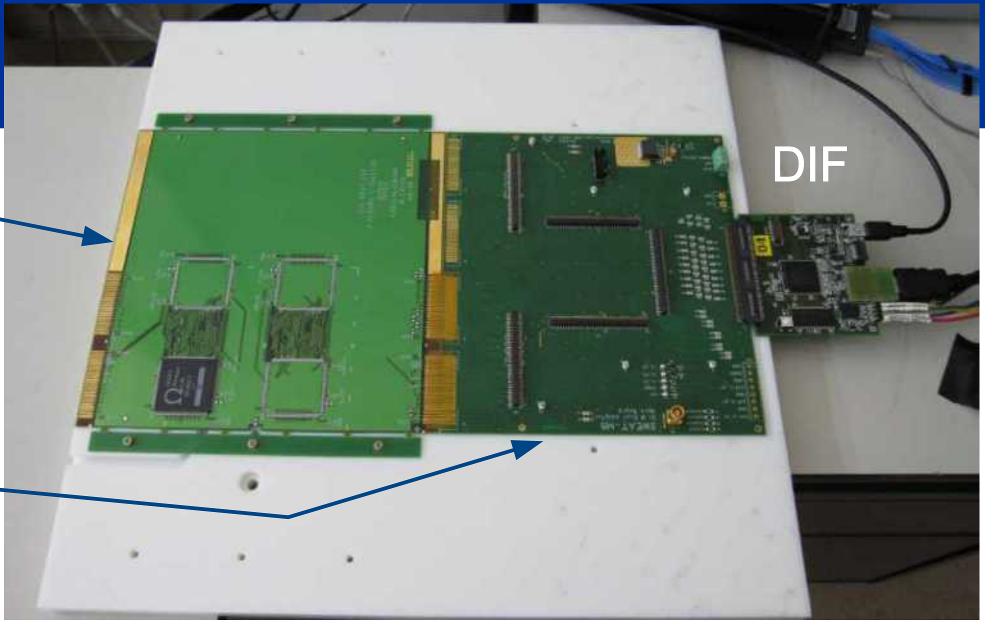
ECAL : FE Boards

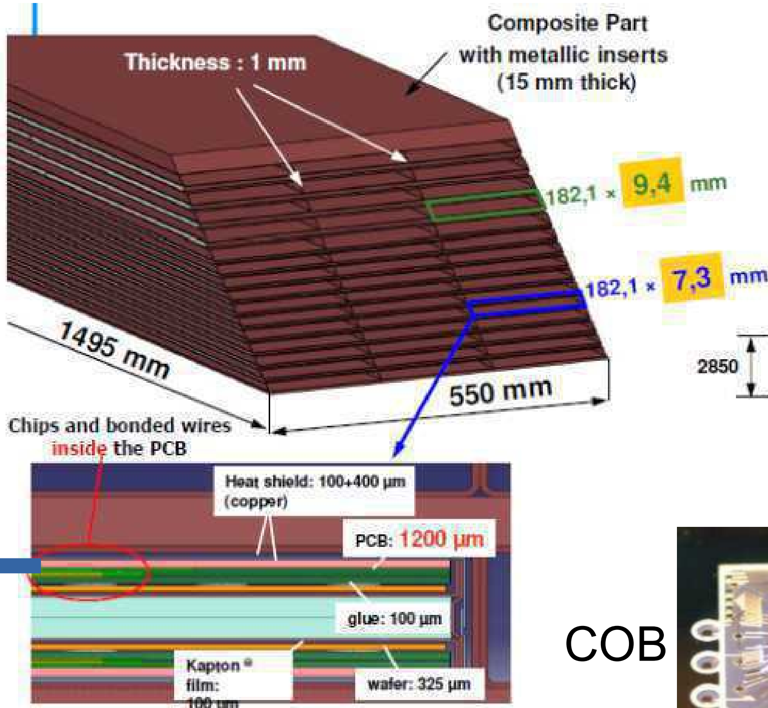
Tests of (early) FEV7 CIP et COB PCB

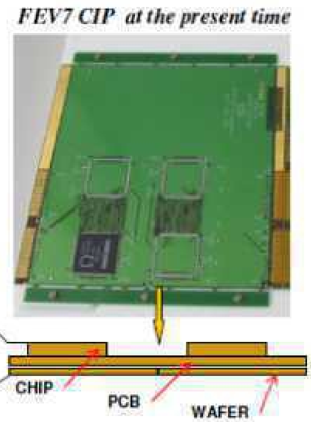
- Thin option (COB) not (yet) solved
  - ⇒ Choice of going to U shape of

"Adaptator" board

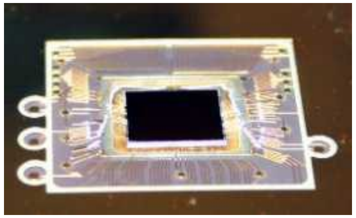
- Interface to cooling
- Buffer for power pulsing
  - with super-capacitors (super-C)
- Connexions tested in strong B field
  → DESY (02/2013): no effect



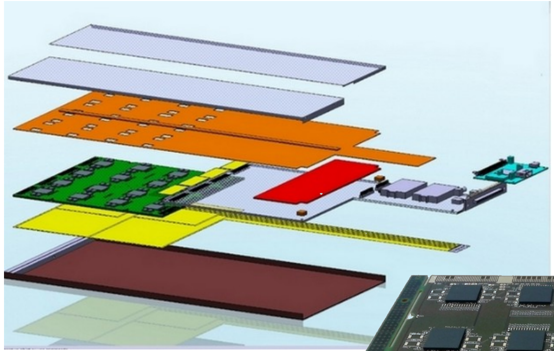




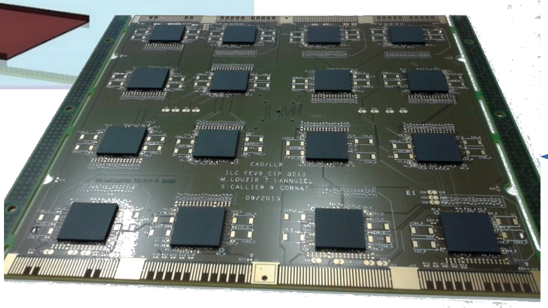
CIP



COB



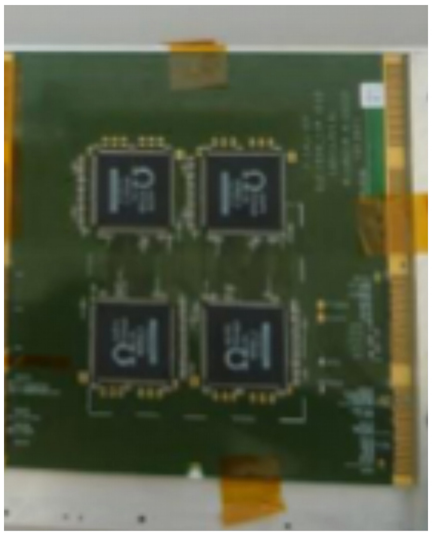
FEV9



BGA packaging

FEV 8→9→10

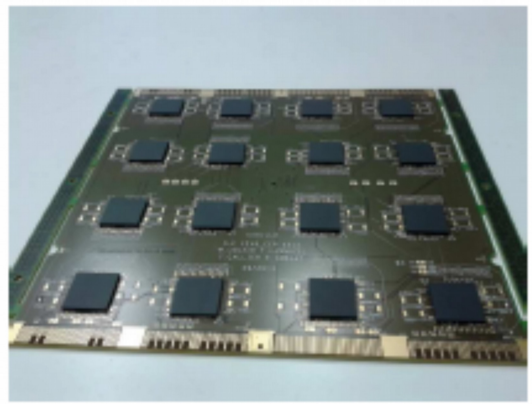
FEV8



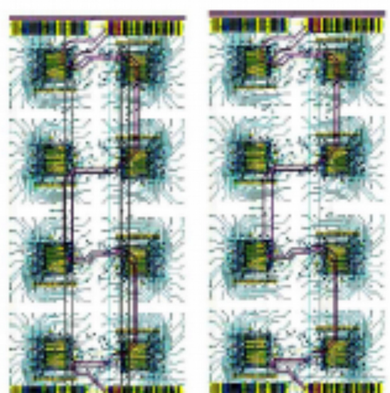
QFP SKIROC2

- 4 chips/board (256ch)
- used in 2012/13 BT
- 10 slabs exist

FEV9



Mechanical model, no chips



Straight and snake lines

16 BGA SKIROC2

- Good flatness (< 0.5 mm)

Electronics test are on-going

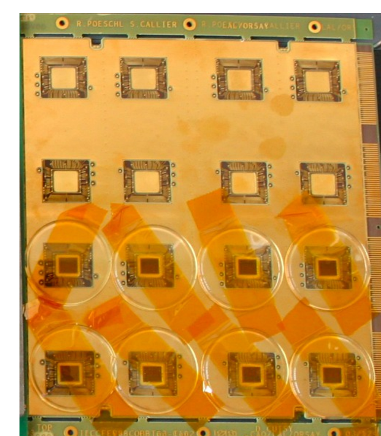
4 FEV9 will be interconnected for long slab test.

FEV10

will be used for 2015 BT

COP option:

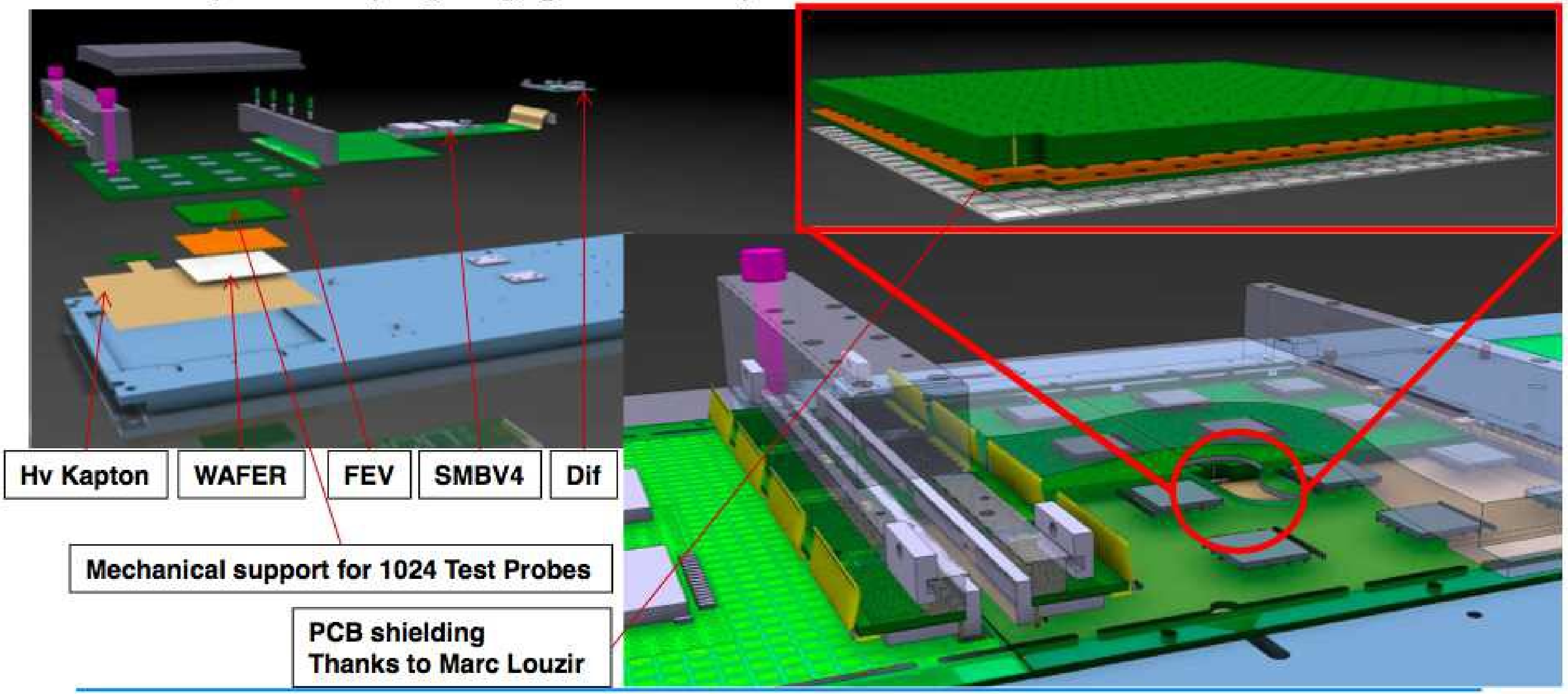
new production (in Korea) soon



Flexible FE test bench

2.0 – Setup option with support of test electric probes for connecting WAFER to FEV

- Realize an assembly with removable wafer in order to acquire cosmic data. This assembly will test the entire acquisition chain (Wafer-FEV-SMBV4-DIF-GDCC-CCC-PC-Software) before the wafer gluing operation. The first test was realized last week



Flexible benches for R&D

Qualification of PCB before assembly

Basis for later mass test

CALICE DAQ2 Acquisition System

Franck Gastaldi's talk
(DAQ Session)

Assembly 1: Gluing

Toward semi-automatic gluing of 4 wafers on every PCB:

- Constraints on the PCB geometry have been identified:
  - Flatness
  - Parallelism of the edges
  - Uniform height of the ASIC soldered on the board

9 sensors has been glued with the robot: used at 2012–13 beam tests

The leakage currents measured before and after the gluing process are similar.

Recent improvements

- Use of specific pumps for dry and clean vacuum
- Careful cleaning of PCB
- New positioning of the glue dots for the external pads, to avoid short-circuits.

Next steps

Software for automated positioning and alignment

Combine gluing and positioning robots

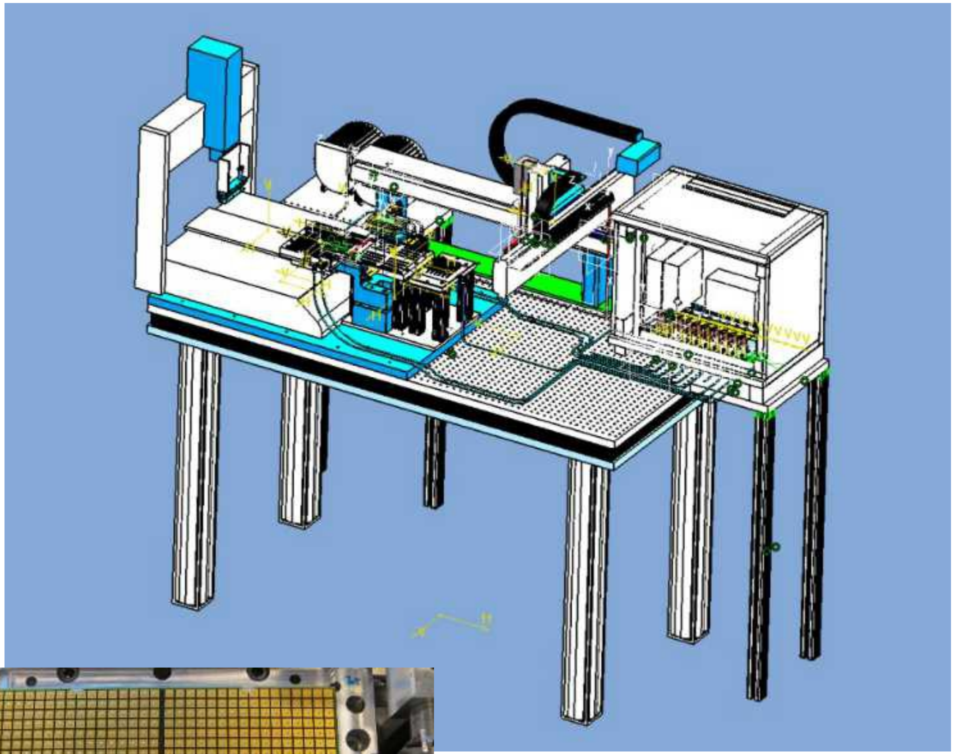
Move to clean room

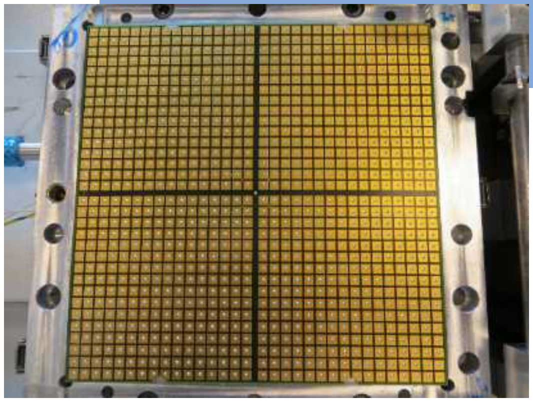
Test the gluing of 4 sensors on a single PCB

- already done with 4 glass tiles on FEV9

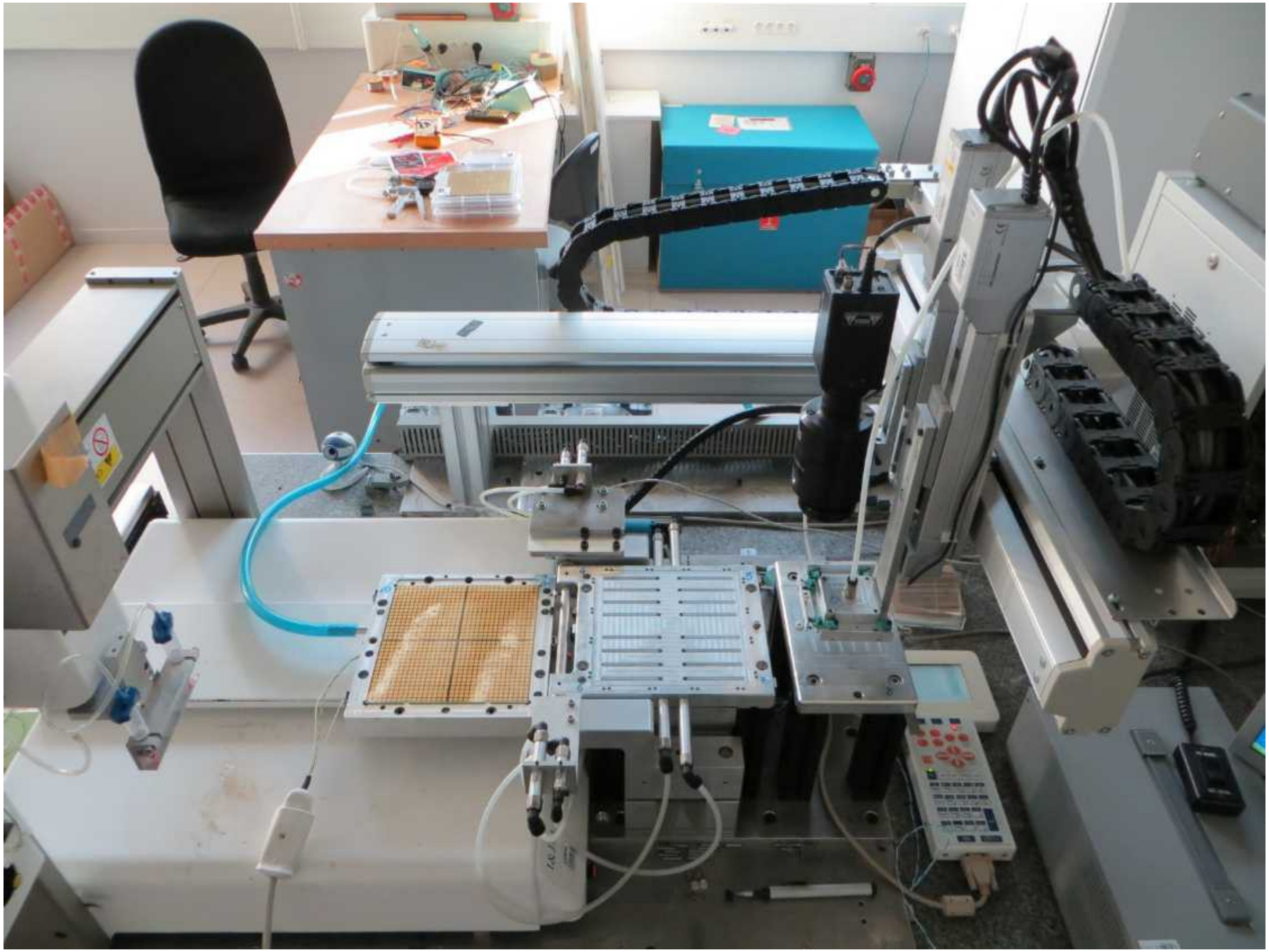
Completing the Quality Insurance

- Procedure
- Metrology of PCB
- Transportation from/to other labs





Both robots assembled



Assembly bench

Development of a set of specifications to assure proper assembly of four wafer ASUs

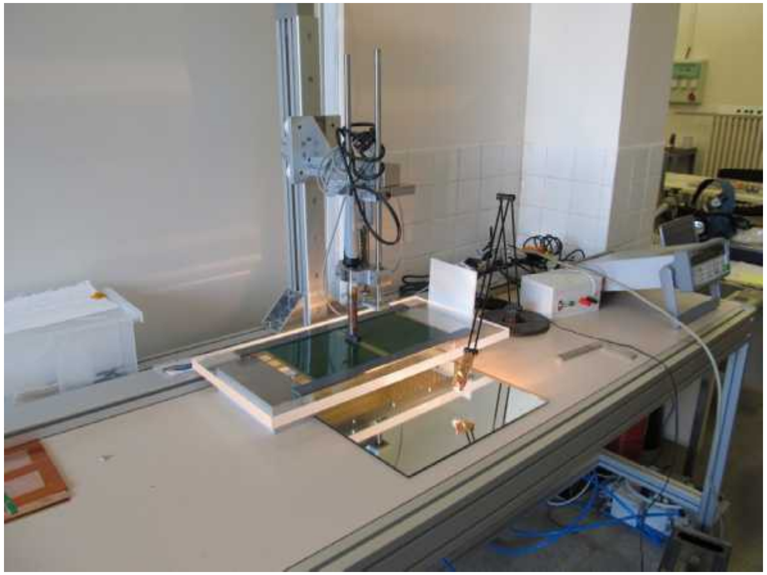
- Tolerances of PCB, H or U board
  - Example : Mechanical stress on wafers during interconnections
- First set end spring 2014

Revision/Scrutinisation of assembly tools

- Development and validation of assembly bench, 'easy' reproducibilty
- Combination of ASU positioning and interconnection

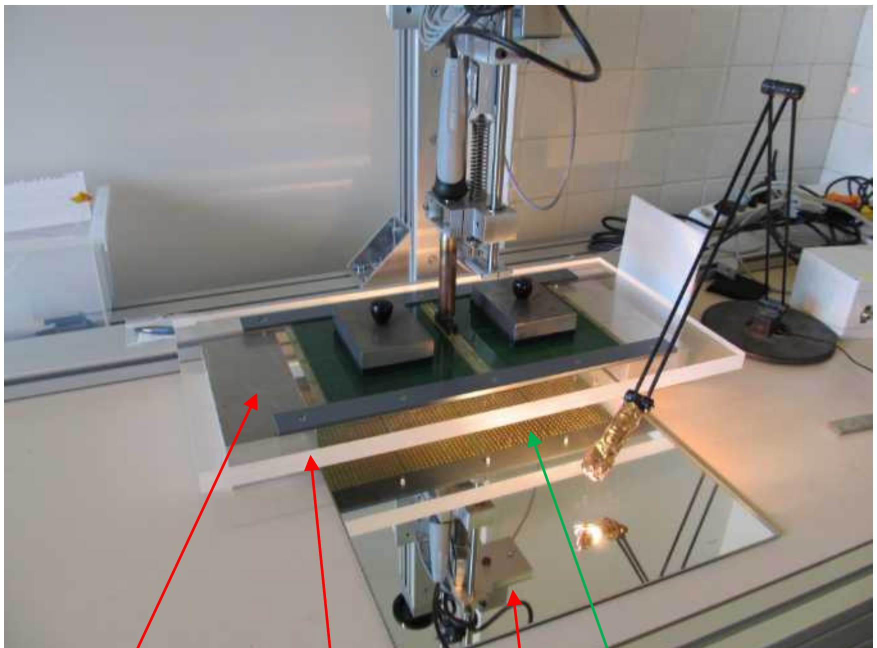
Interconnection station

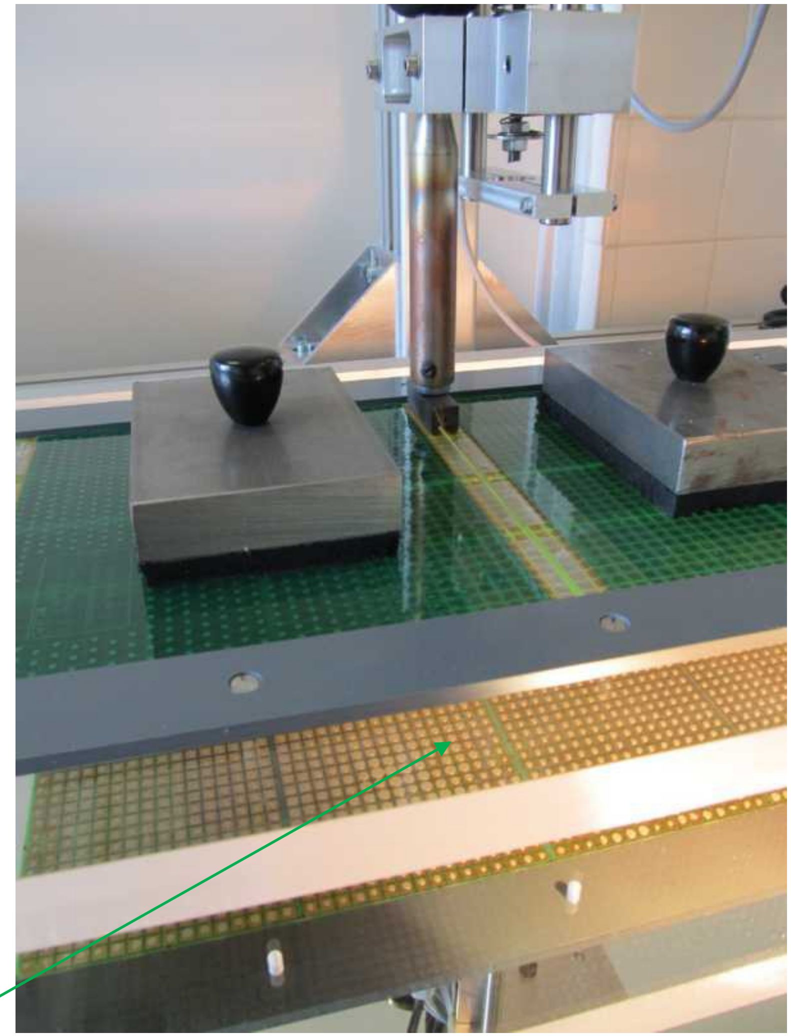
Assembly station



Assembly of slabs: example of systematic studies

Pressure test on ASU (FEV8_Glass) with soldier iron for interconnection





Support of plate

Plexiglass plate

Mirror

Mirrored image of lower ASU part

Tests will be repeated with ‘false’ wafers (contact with IEF Orsay)

Wafers:

Key elements of detector

- Basic unit for the size of the detector
- (Most expensive part too)

Guard Rings

- Alternative designs
  - segmented, "edgeless"
- Complete characterisation of sensors
  ⇒ link to & test variety of producers
- Work in CALIIMAX-HEP French ANR
  in relation with Kyushu/Hamamatsu

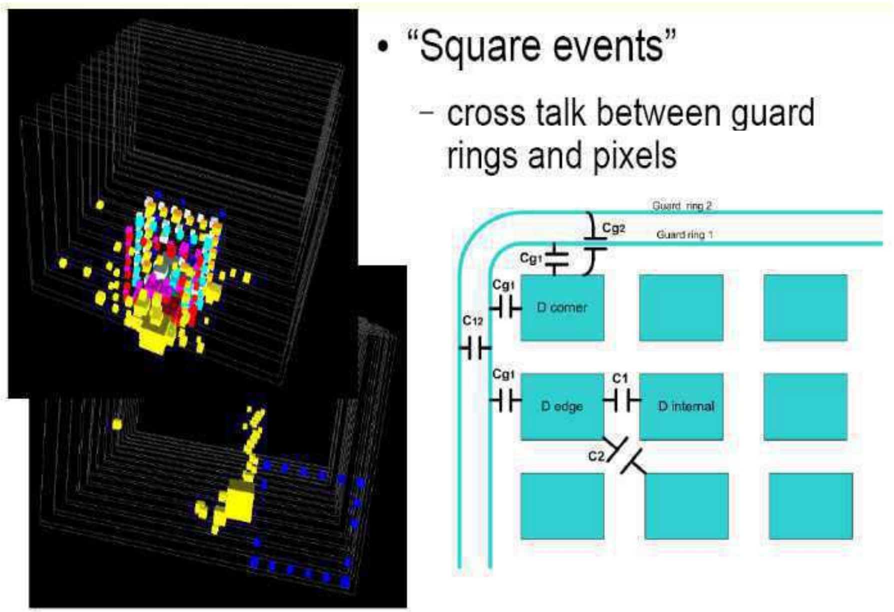
Test of Silicon sensors

- Test different HPK designs: C-V, I-V.
- Laser tests: xtalk via GR.

Plans: Irradiation tests (γ,n)

See Tatsuhiko Tomita's Poster

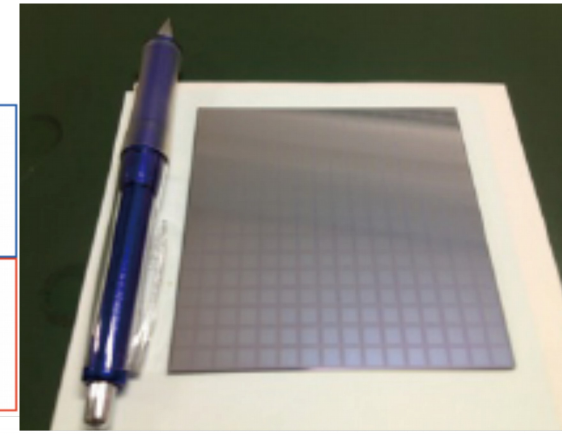
From physics prototype test beams

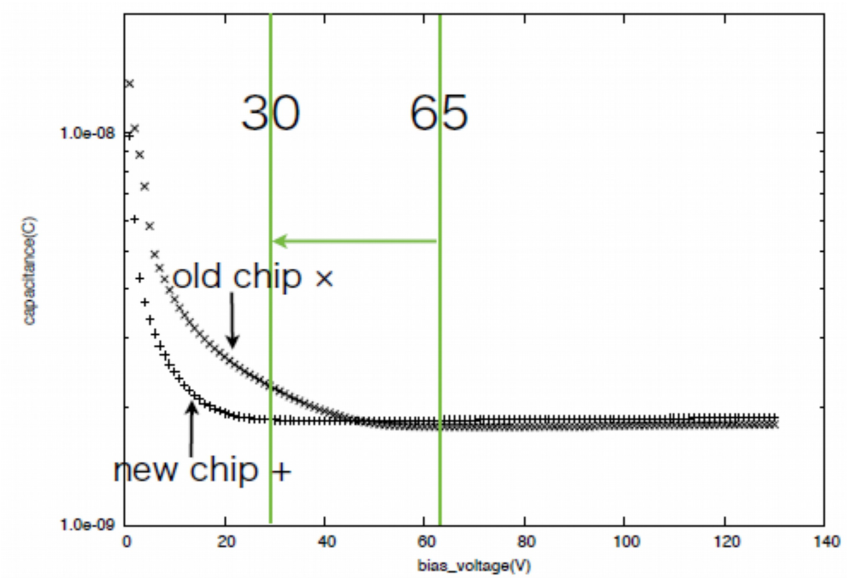


Basic sensor study

Two batches of Hamamatsu sensors

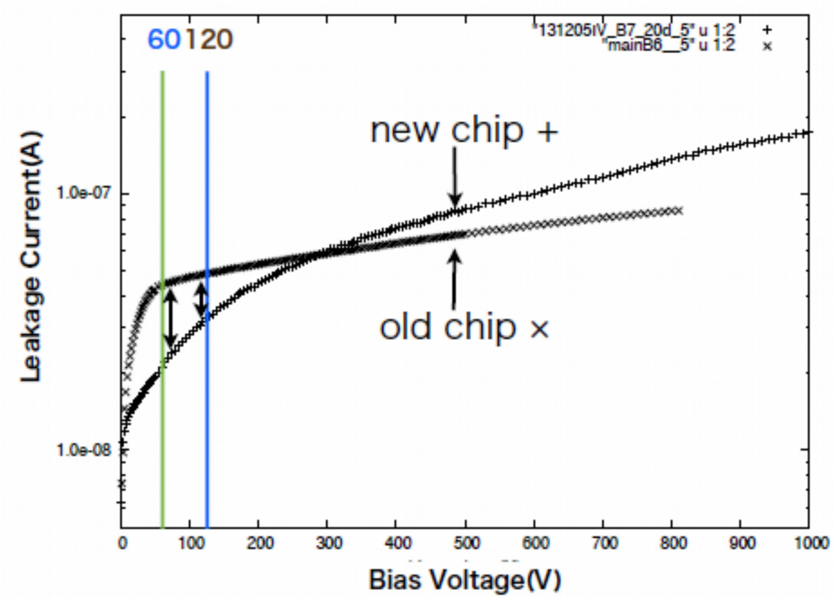
pixel size : 5.5 x 5.5 mm	same	pixel size : 5.5 x 5.5 mm
thickness : 320 μm	same	thickness : 320 μm
number of pixels : 256	same	number of pixels : 256
guard ring : 1	different	guard ring : 0
resistivity : unknown	! higher	resistivity : unknown
	as Hamamatsu said	





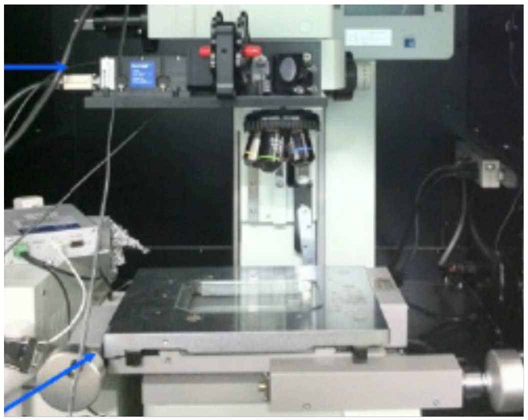
C-V curve: saturation V differs

The leakage current at 120 V is 31nA (old : 48nA),
at 60 V is 21nA.



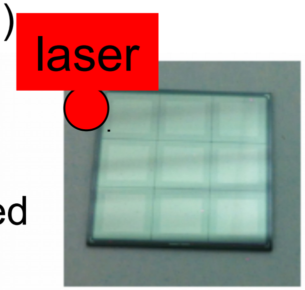
This value is twice lower than old prototype.

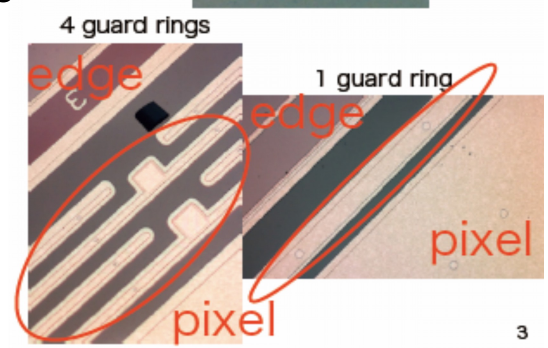
Laser study with guard rings (baby wafers)



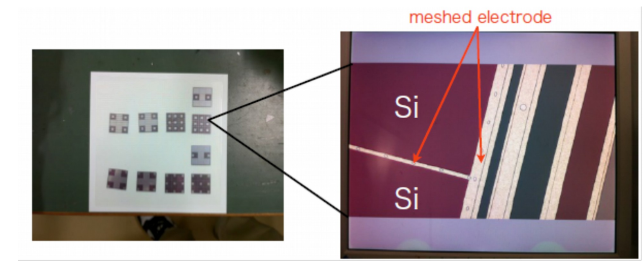
Nd:YAG laser (1064nm) focused to < 20 μm
~ 1.5 ns pulse width
~13 kW peak power
10,000 pulses measured
120V bias voltage on silicon

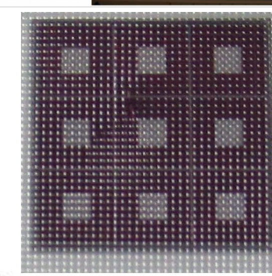
Dedicated DAQ



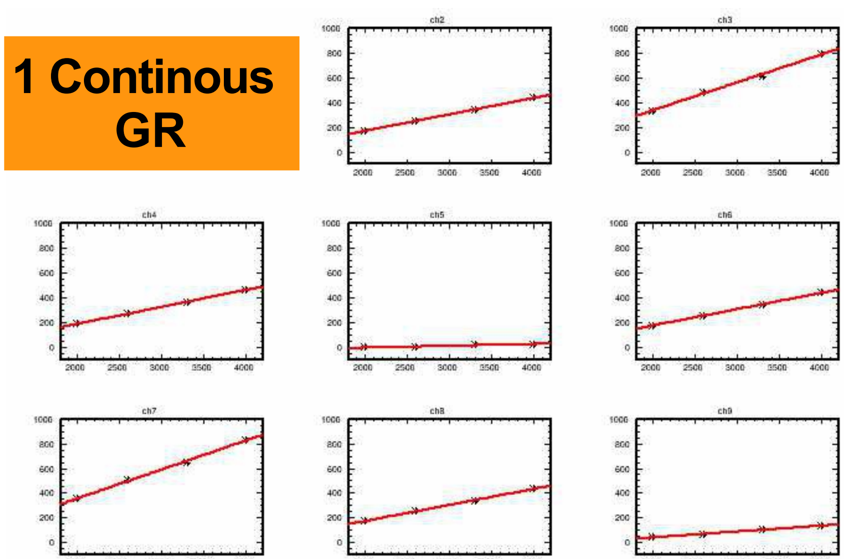


Next : Meshed electrodes
→ shoot inside pixels

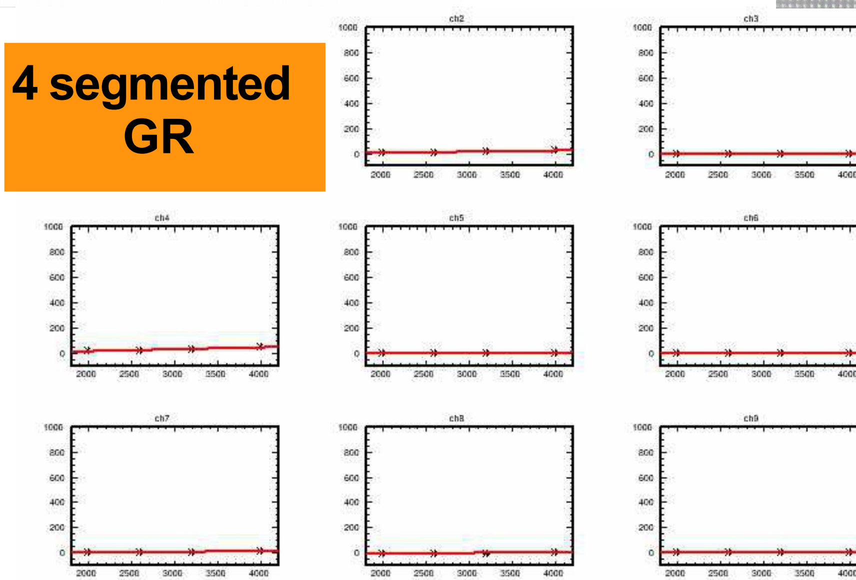




1 Continous GR

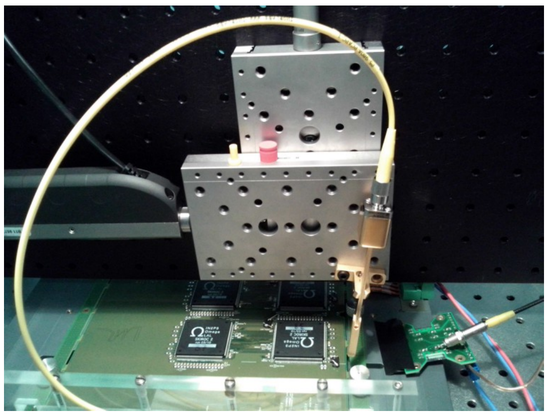


4 segmented GR



Laser study (full wafer)

. . . fires in Si detachable sensor in the gap between aluminium contacts



Laser characteristics: = 1056 ± 5 nm, 200 kHz, < 1 nsec pulse

- ~ 700 MIP signal. Intrinsic silicon absorption length at 300 K: ≈ 0.8 mm.

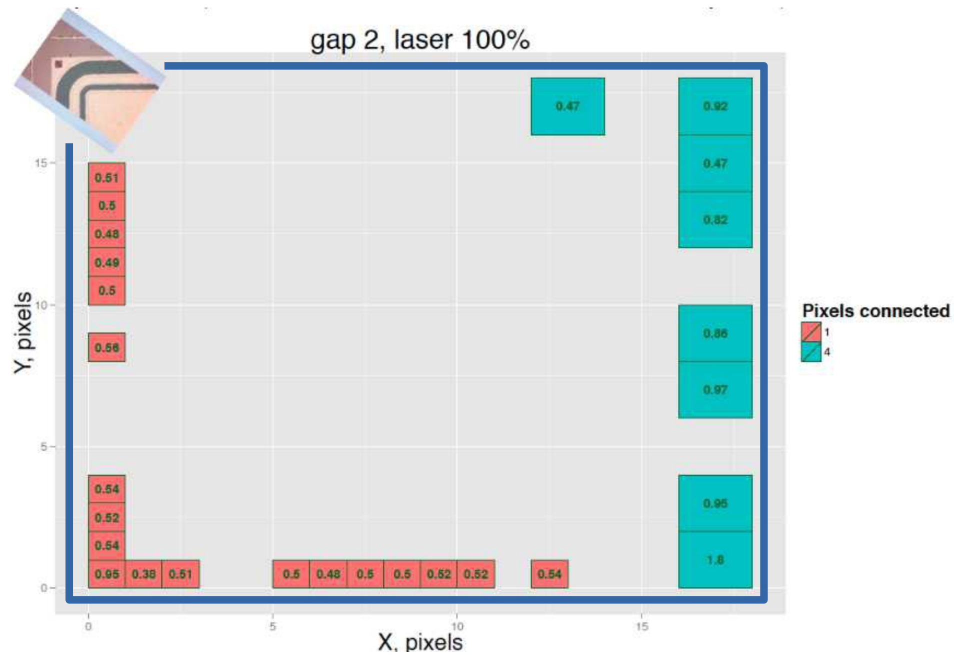
Adapted Flexible FE testbench setup

- 1024 spring contacts of 5 mm length between pixels and PCB pads.

"Standard Acquisition chain"

Hamamatsu silicon sensor:

- 16x16 pixels of 5.5×5.5 mm^2, thickness 330 μm.



Preliminary results:

- Not all springs installed and not all have contacts, about half is operational.
- Clear signals in connected pixels.
- A typical induced signal is ~0.4...0.5% per outer pixel side ×2 for corner, ×2 in case of 4 connected pixels.

To be improved: high noises (set-up), PCB bending.

Working well but “Room for improvement”

from Charge injection, cosmics, test beam

Post triggering of BX+1, BX+2 at many channels

- in ≤ 50% of events
- improved by decoupling capacitor but still exists

Noisy channel – ~10%? (PCB routing?)

External trigger not working

- Auto trigger mode only

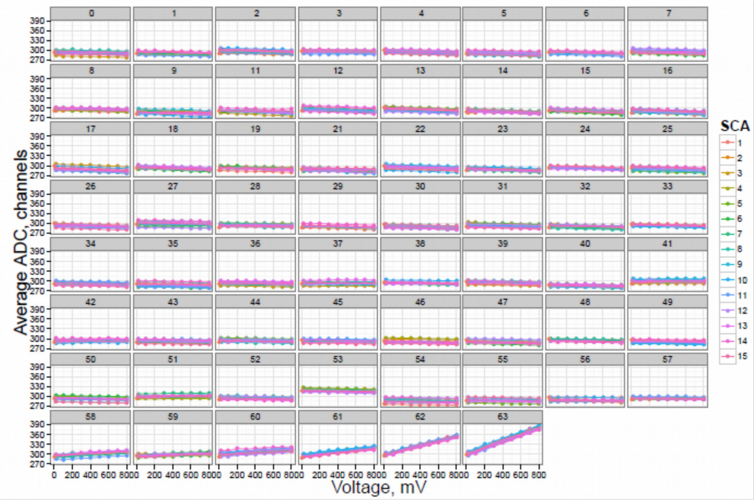
TDC (maybe too noisy)

~ 5% nonlinearity at ~1 MIP level

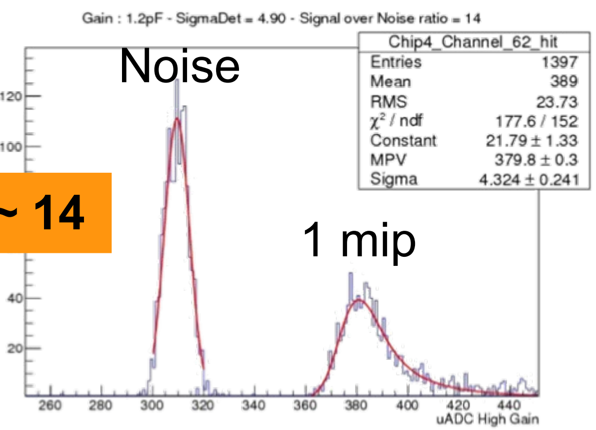
Many of them will be improved/solved in FEV9 & 10

Charge injection,

- 1 chip, ≠ memory (SCA)



Best S/N ~ 14



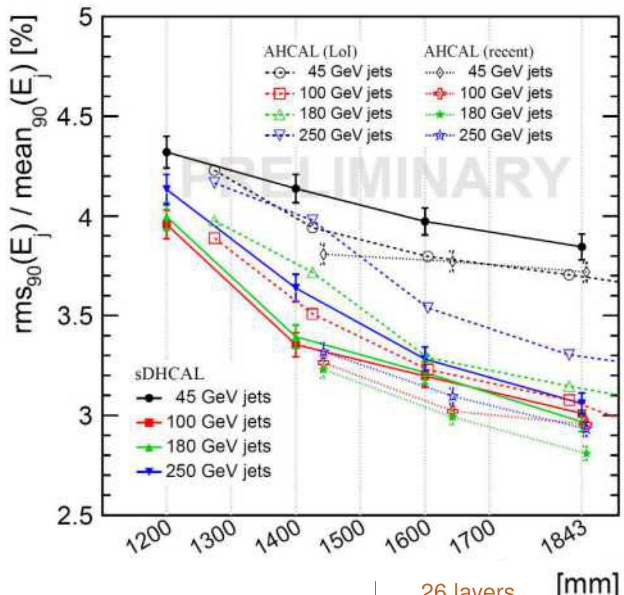
Optimisation: Cost vs performance

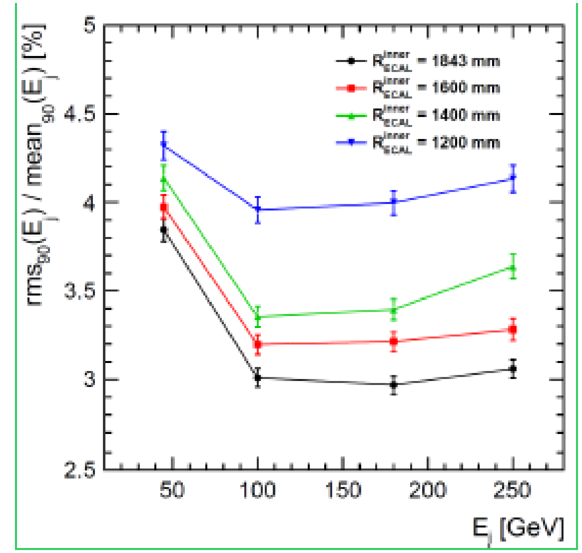
Multi-parametric optimisation

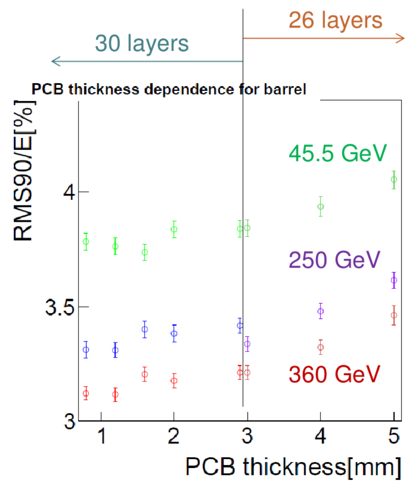
- Using full simulation & PFA rec (PandoraPFA) on
  - jets, tau's, gamma
  - over full E range
- options mix: HCAL's
- Main cost driver:
  - Radius of Tracker
  - Number of layers
  - Wafers & structural gaps,
  - Electronics thickness
  - Resilience: allowable failure rate (channel, chips)

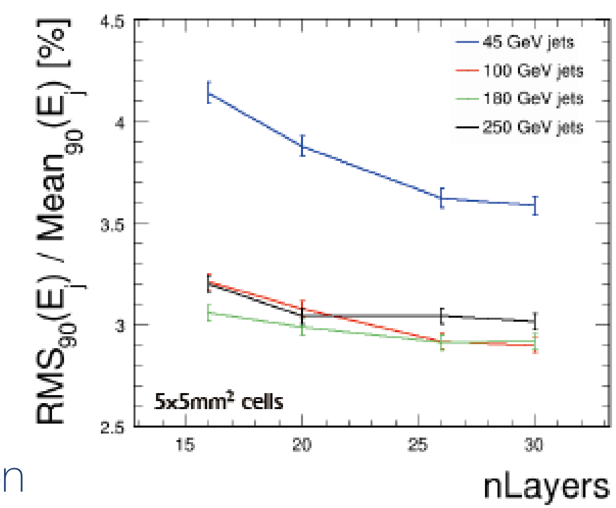
Reduction of

- Radius (1,8m➞1,4m)
- Number of layer (30➞25)









seems reasonable for minor perf. degradation for ~30-40% cost reduction

To be assessed with full simulation around new design

Conclusion & Plans

Complex task of learning & optimisation

- Every aspects intertwined:
  - Electronics performance (including power budget), Thermic, Mechanics, Compactness, reconstruction SW … within Physics performances & Cost “envelop”
  - Mass production & Quality Aspects at every stage
- Long Iterative learning procedure
- Wafer design and characterisation crucial (Cost), contact with producers (experience buildup)

2014: Solutions found for every aspects → “full” technological prototype in 2015

- Short slabs (1 ASU) in Fall
- Tower of 18×18 cm^2 + 1 Long slab (6–7 ASUs) in 2015

TB with HE electrons: stand-alone & combined (SDHCAL, AHCAL slabs): end 2015–2016

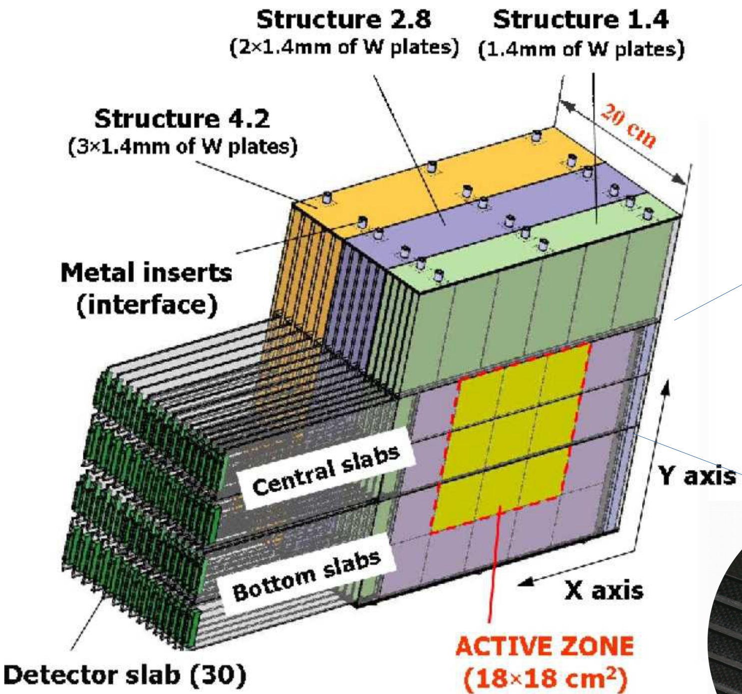
- verification of response, electronics in beam

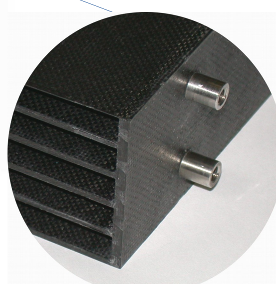
10 yrs of R&D → applications to future detectors: ILD but also

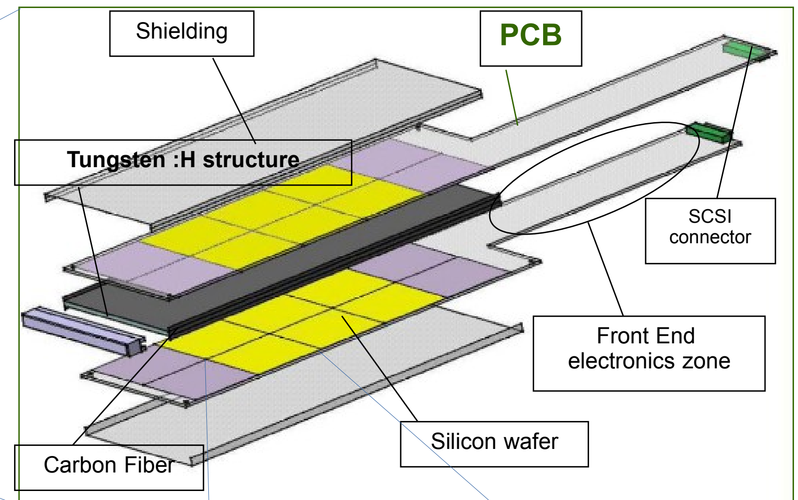
- HL upgrade of the CMS endcap phase2 (HGCAL option)
- Future circular colliders (TLEP/FCC, CEPC); heavy ions fix exp.
  - Adaptation needed (power consumption → lower granularity)
  - Si radiation resistance

Extras

Physical prototype



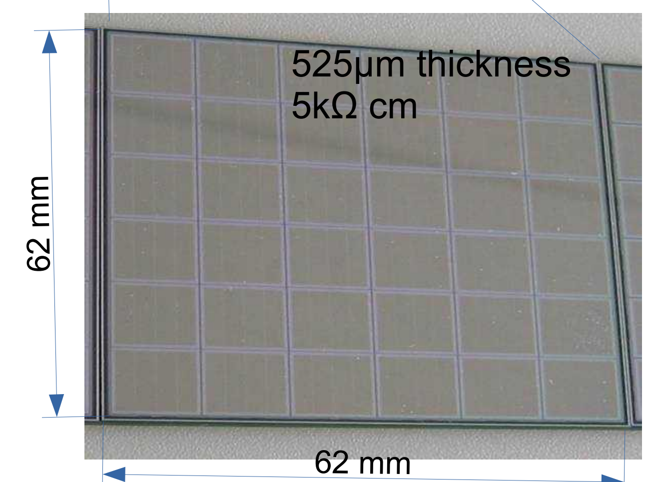




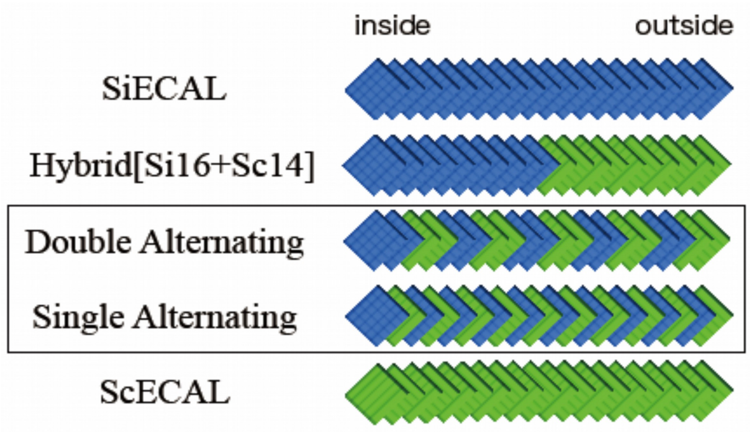
Structure

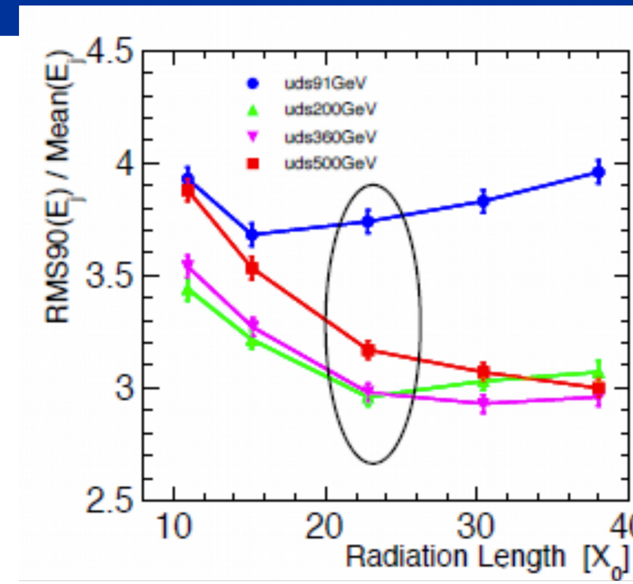
- 30 layers of Carbon Fiber /Tungsten
  $10{\times}0.4\ X_0+10{\times}0.8\ X_0+10{\times}1.2\ X_0 = 24\ X_0$
- Self supporting Structure
- Sensor Units with external analog readout chips

High resistivity Si PIN Diode divided in 10×10 mm² cells



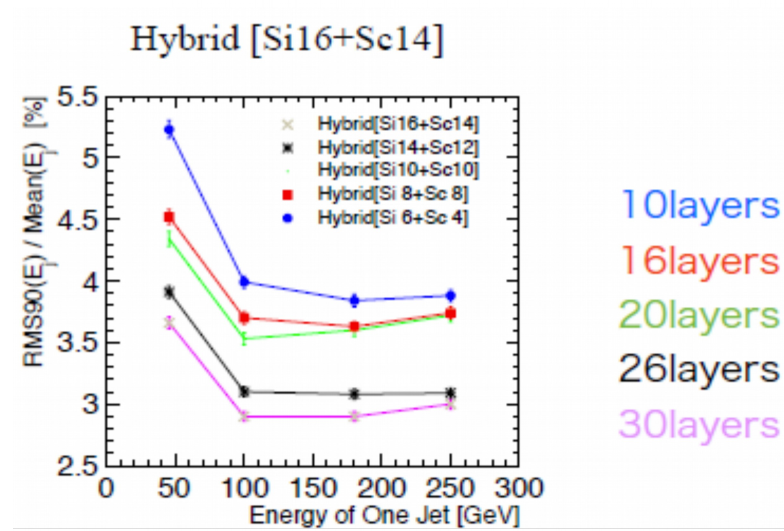
Optimization of “Hybrid”





RMS90(Ej) / Mean(Ej) [%]

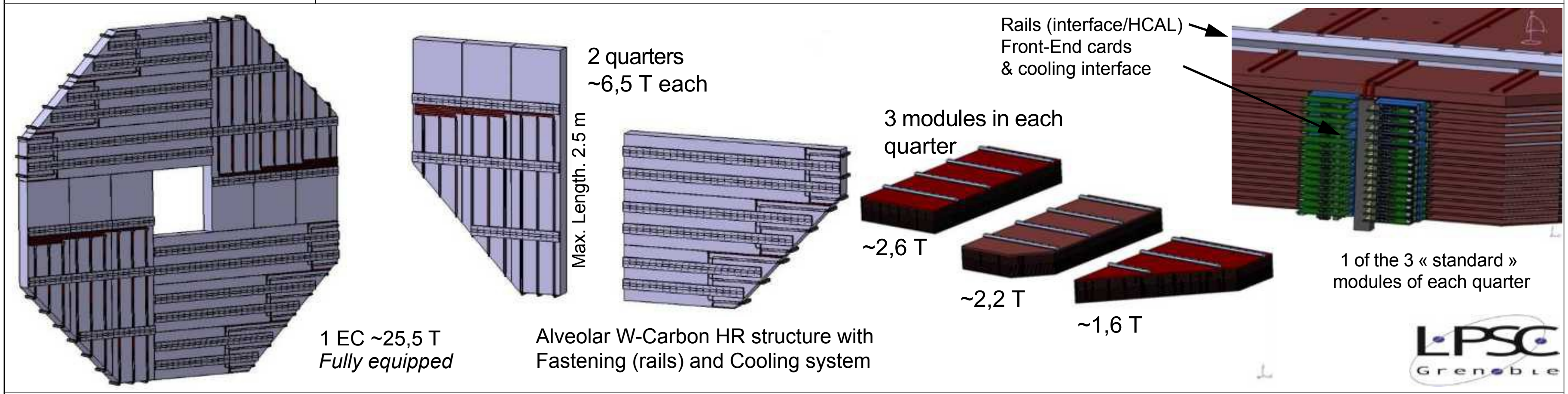
	45GeV	100GeV	180GeV	250GeV
SiECAL	3.70	2.86	2.88	2.96
Hybrid [Si16+Sc14]	**3.66**	**2.90**	**2.90**	**3.00**
Double	**3.69**	**2.92**	**2.91**	**3.02**
Single	**3.73**	**2.90**	**2.87**	**3.00**
ScECAL	3.70	2.97	3.05	3.18



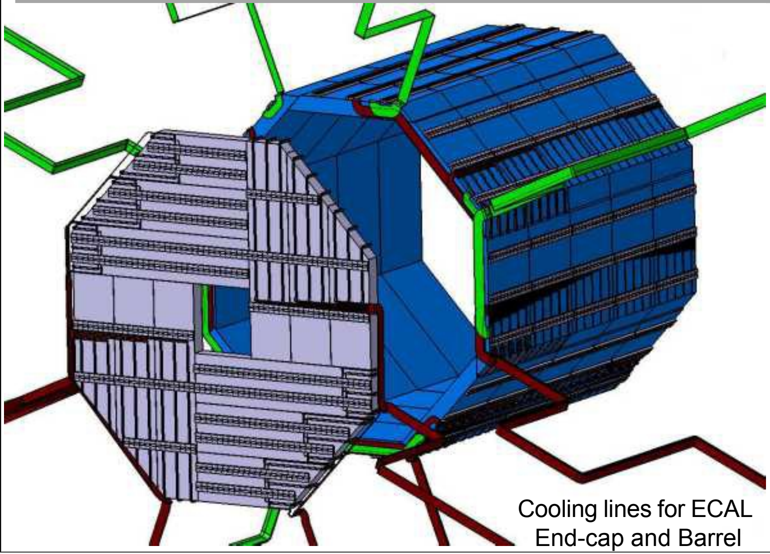
We will move to more strategic way...

Current structure of end caps

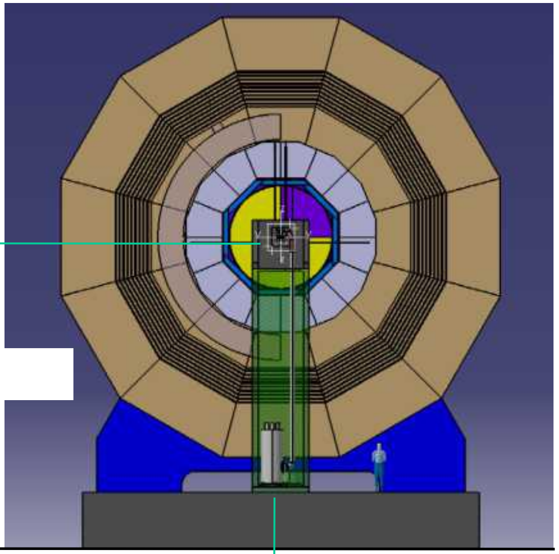
Modular structure	2 End-Caps Total of 2x12 modules = 2 x [4 quarters each]

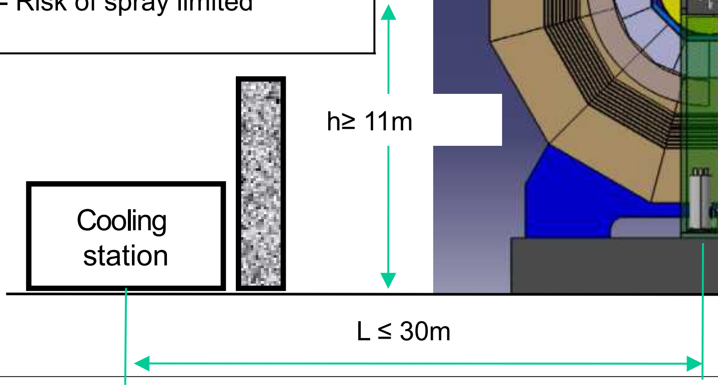


ECAL Cooling Integration - Leakless system

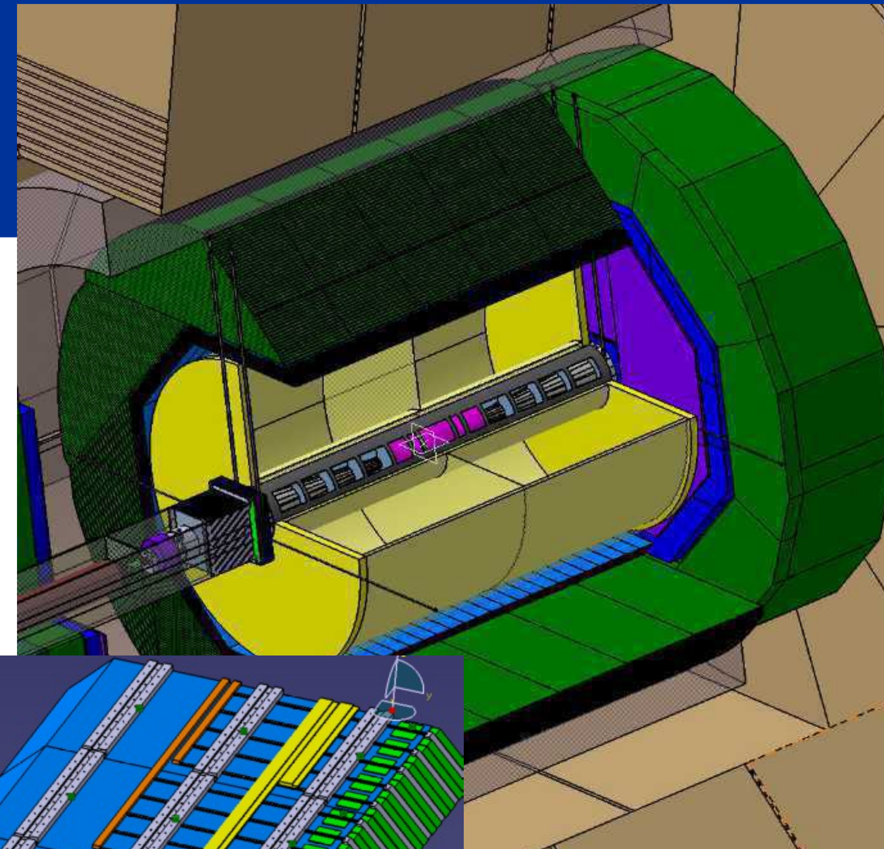


Leakless system :
- Cooling front–end
- Low water speed
- low temperature gradient
- Risk of spray limited





ILD : intégration



Intégration → DBD (fin 2012)

- Développement d'outils de CAO
- EDMS – aussi utilisé coté machine
- ↔ LAL, DESY

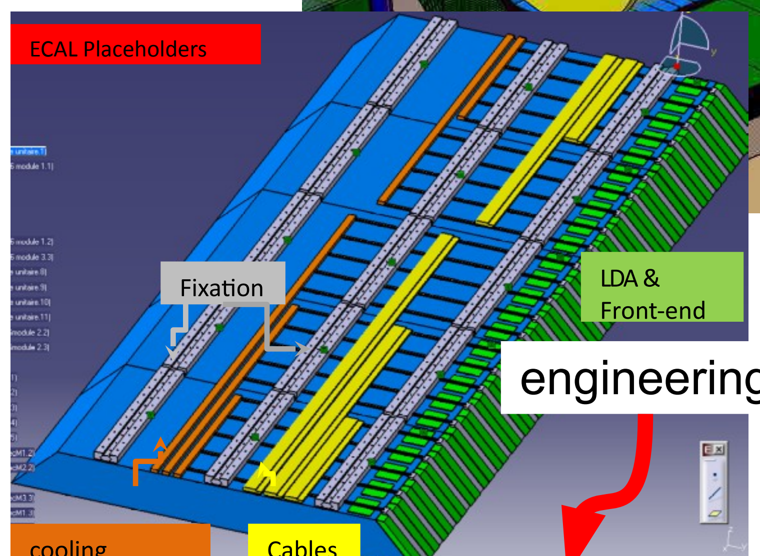
Calorimètres

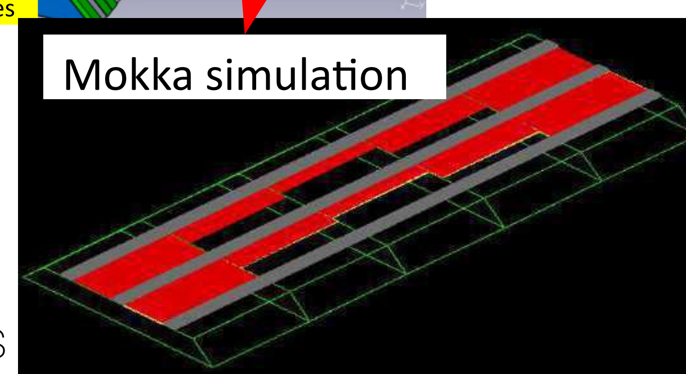
- ECAL (↔ LPSC, LAL)
- DHCAL (↔ IPNL, CIEMAT)

Cohérence ↔ simulation

Développement d'un modèle réaliste

- Zones mortes
- services (cooling, power)
- Supports

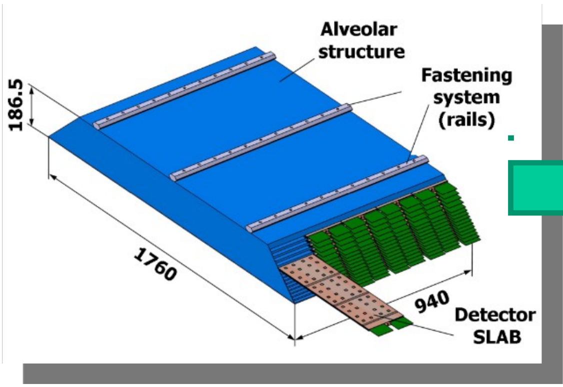




Critique pour le DBD
(très visible au meeting IWLC'2010)

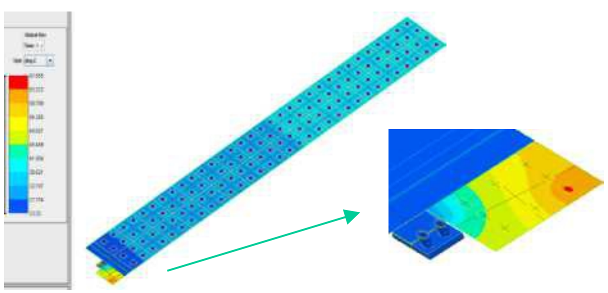
1ère version de ILD ~ complète
→ production MC de masse

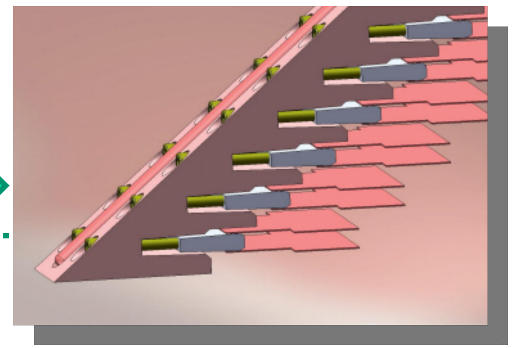
Study from the power source to the global cooling



SLAB

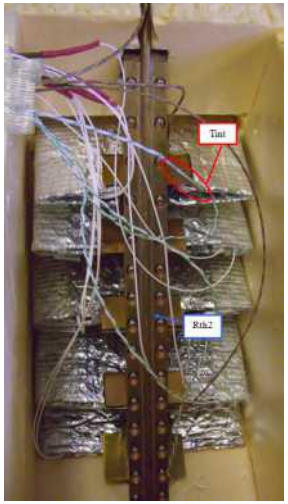
Thermal simulation and test on Slab

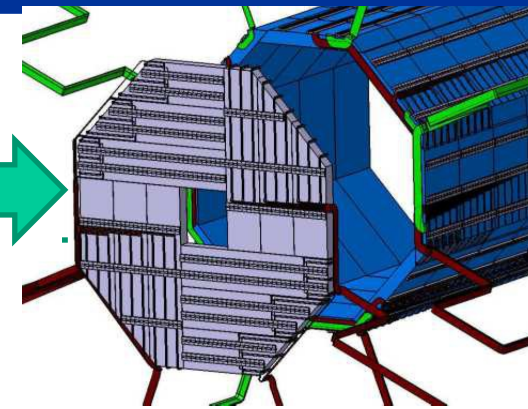




Heat exchanger

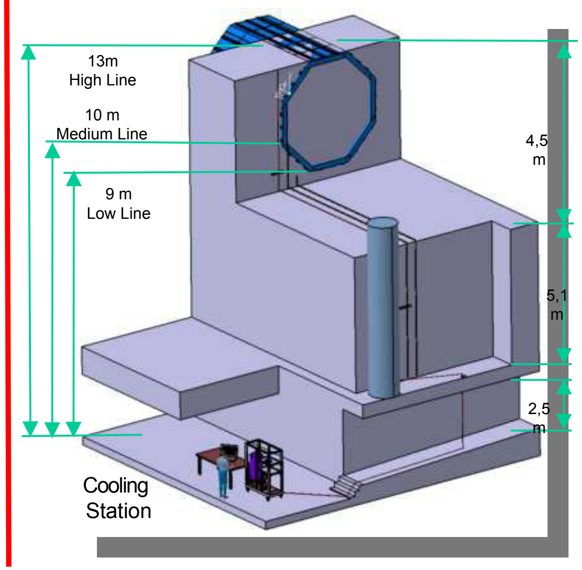
Simulation and test on different type of heat exchangers



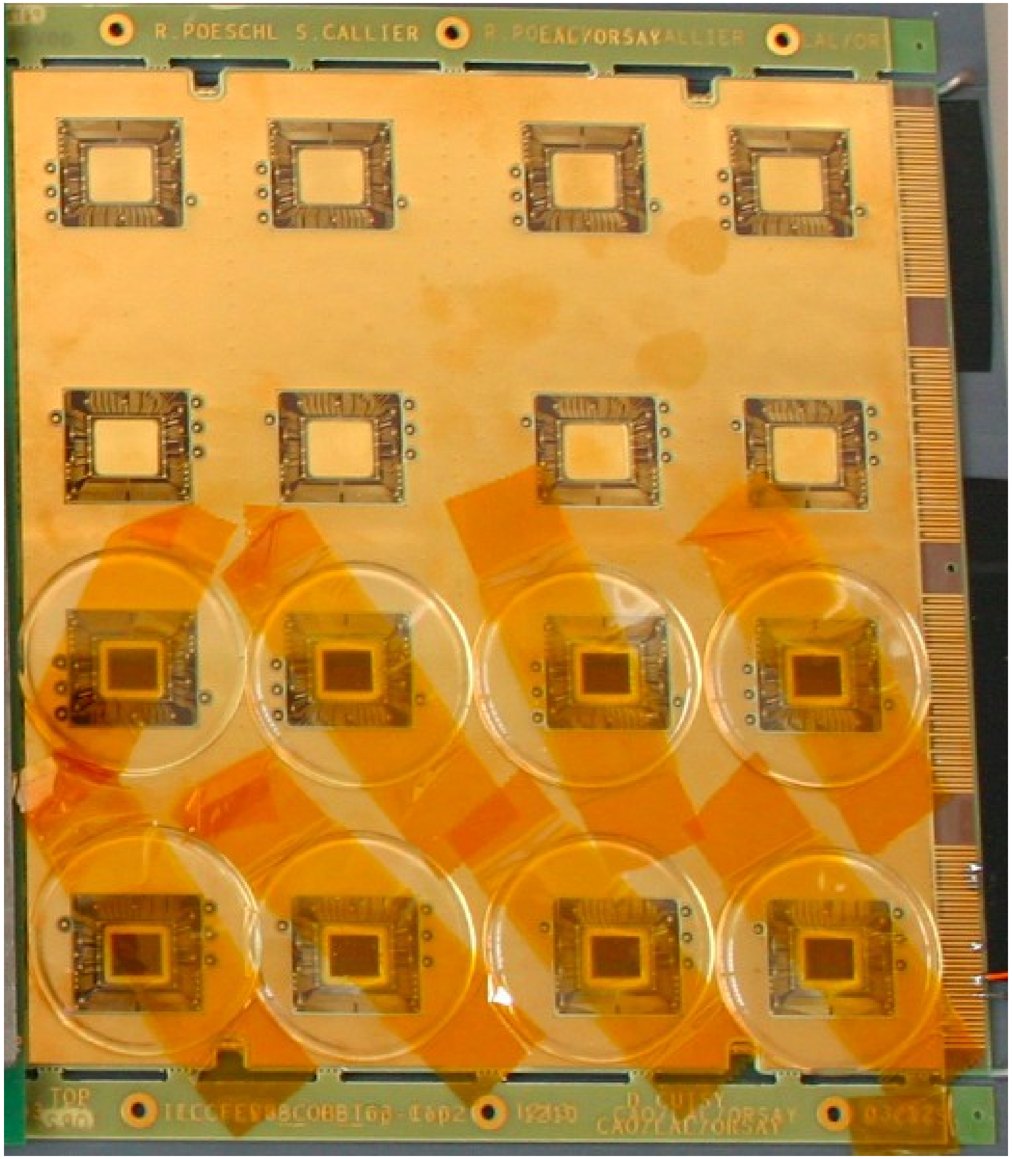


Global cooling

True scale leak less loop



Reminder FEV_COB



- Interface board with Chip On Board
  - Assures compact calorimeter

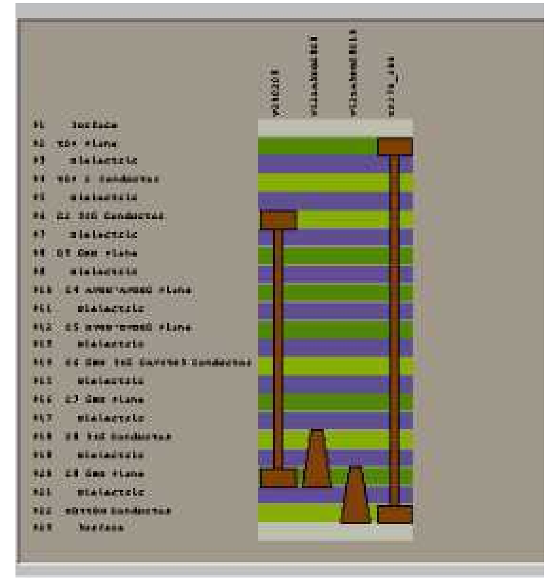
- Not trivial specs
  Ultrathin : 9 layers with thickness of about 1.2mm
  Deviation of total planarity of about 0.5 mm (3mm is industrial standard)

However it's now there in a first version

- Design and routing OMEGA/LAL
- Fabrication end of 2012
- Metrology at LAL
- Chips mounted beginning of 2013 by CERN bonding lab

- First tests in summer 2013 at LAL

Cooperation with EOS



- Korean company EOS has declared to be ready to produce the PCB
  -> Relaxed constraints on the thickness 1.2mm -> 1.5mm

- Technical discussion ongoing via mail but production is imminent

- Plans to assure entire PCB assembly in Korea
  - PCB production
  - ASIC bonding
  - Encapsulation