



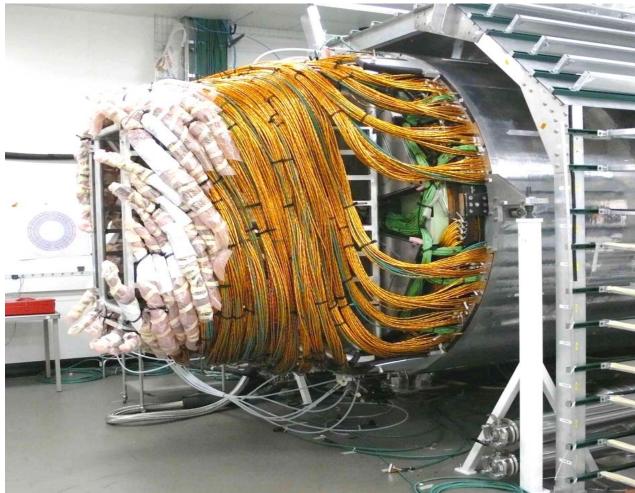


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- Broad ranging discussion
 - First, Explore alternative ideas and approaches
 - Then, Focus on most promising ones
 - 19 July Tracker-Trigger Joint meeting
 - 2 Aug Sensor WG meeting
 - 11 Sep Simulations WG
 - 12 Sep Readout WG
 - 13 Sep Material, cooling, engineering WG (1/2 day)
 - 13 Sep Steering Group
 - Expect follow ups in monthly Tracker meetings (Thursday)
 - 8 Nov Readout WG (tbc)
 - 6 Dec Simulations Sensors (tbc)

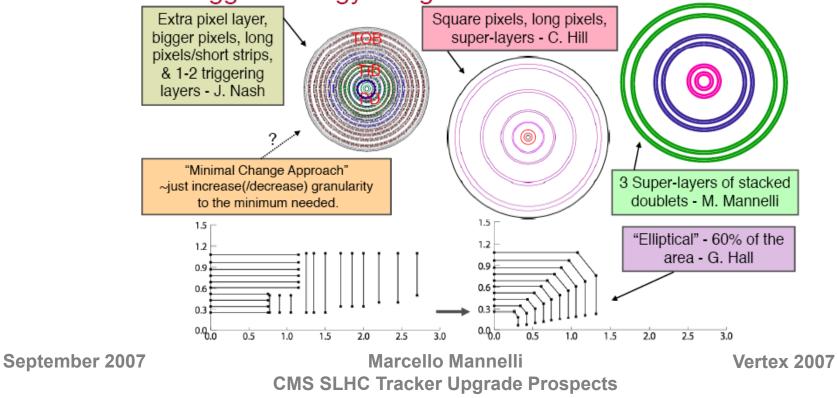
+ Simulations video meeting every two weeks

	Geoff Hall	2 CM	S week Sep 2007 SLHC SG
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- Broad ranging discussion
 - First, Explore alternative ideas and approaches
 - Then, Focus on most promising ones
 - No single strawman tracking system or tracking trigger strategy/design







- Broad ranging discussion
 - First, Explore alternative ideas and approaches
 - Then, Focus on most promising ones
- This presentation will NOT be and Over-view
- Highlight Two sets of Thoughts concerning:

Local Occupancy Reduction / Hit Discrimination

Granularity vs Power Consumption

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SLHC CMS Tracker Upgrade Required Functionality



- Fast, Robust, Efficient, High Resolution Tracking
- HLT Capability:
 - The present CMS Tracker will be used in the HLT, immediately after the hardware Level-1 Trigger, to select Physics Objects and Event Topology with much better Resolution, Efficiency & Background Rejection
 - High Pt muons, electrons, b-jets, tau-jets, Missing ET, etc.
- Level 1 Trigger Capability:
 - Must keep ~ same L1 Trigger rate, despite 10 time higher event rate, 10 ~ 20 times higher occupancy, without sacrificing Efficiency and Background Rejection
 - Just raising thresholds will not work AND is NOT desirable: scale is set by Physics

At SLHC need to transfer use of the Tracker from HLT to Level-1 Trigger

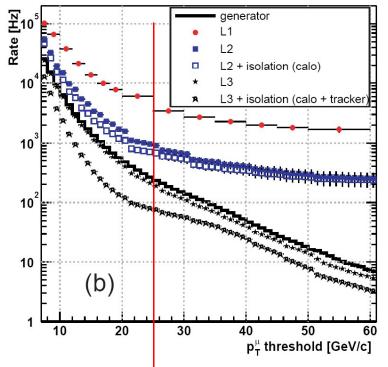
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Tracker: From HLT to L1



- Confirmation of Isolated High-pt μ Candidates
 - Fast, Efficient & Clean Tracking
 - Excellent Pt resolution
- Increased Rejection of fake e/γ Candidates
 - Match with Track at Vertex
- Rejection of Uncorrelated Combinations, from different primary vertex
 - Match with Tracks at Vertex



Factor ~ 100 reduction For same Pt threshold

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Tracker: From HLT to L1



- The CMS Tracker produces vast amounts of information for each L1 Triggered event
 - For the Strip Tracker, the Analogue Information for each Strip is read-out at ~ 100kHz
 - For the Pixel Detector, the Analogue Information for each Cluster is readout at ~ 100kHz
 - Local Zero Suppression
 - All hits in a given Region of Interest are taken into consideration in the HLT
- It is implausible to access this information at 10³⁵ Luminosity & 20(40)MHz crossing rate, as input to the L1 Trigger Decision
- Local Zero-Suppression will be required for the full Tracker. In addition consider

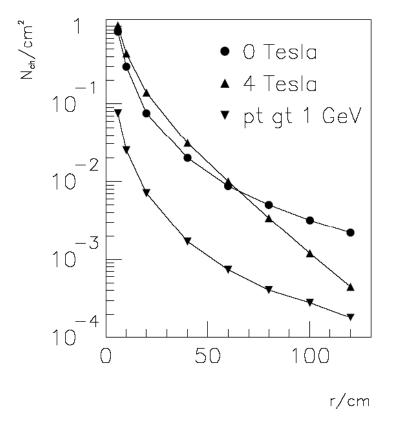
Local Occupancy Reduction / Hit Discrimination

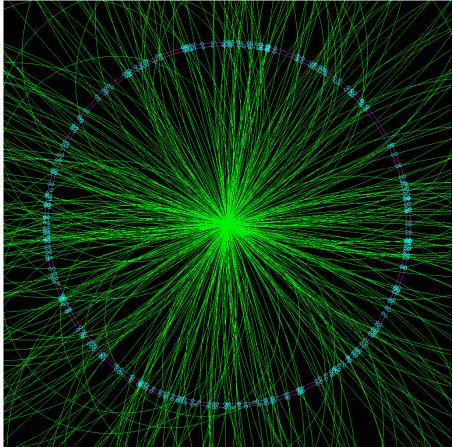
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SLHC CMS Tracker Upgrade Local Occupancy Reduction







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SLHC CMS Tracker Upgrade Possible Local Occupancy Reduction Scheme



Possible Strategy: Local Pt Discrimination

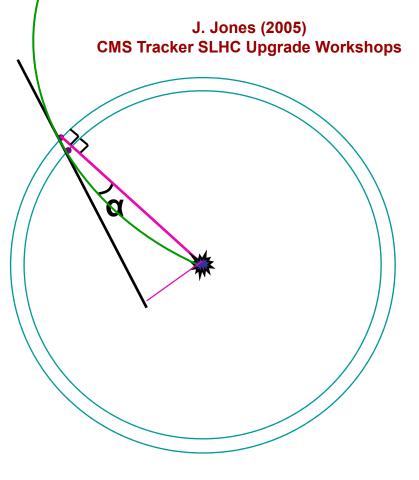
- Only read-out hits from tracks above a certain Pt threshold
 - 1 GeV Pt threshold would reduce read-out hits by ~ factor 10
 - Tracks below 1 GeV Pt are usually not very interesting, especially in the early phases of event selection
- For Level 1 Triggering purposes, need also to identity (muon) tracks above 10 ~ 20 GeV
- Consider a hierarchical scheme for Local Pt Discrimination



SLHC CMS Tracker Upgrade Possible Local Occupancy Reduction Scheme

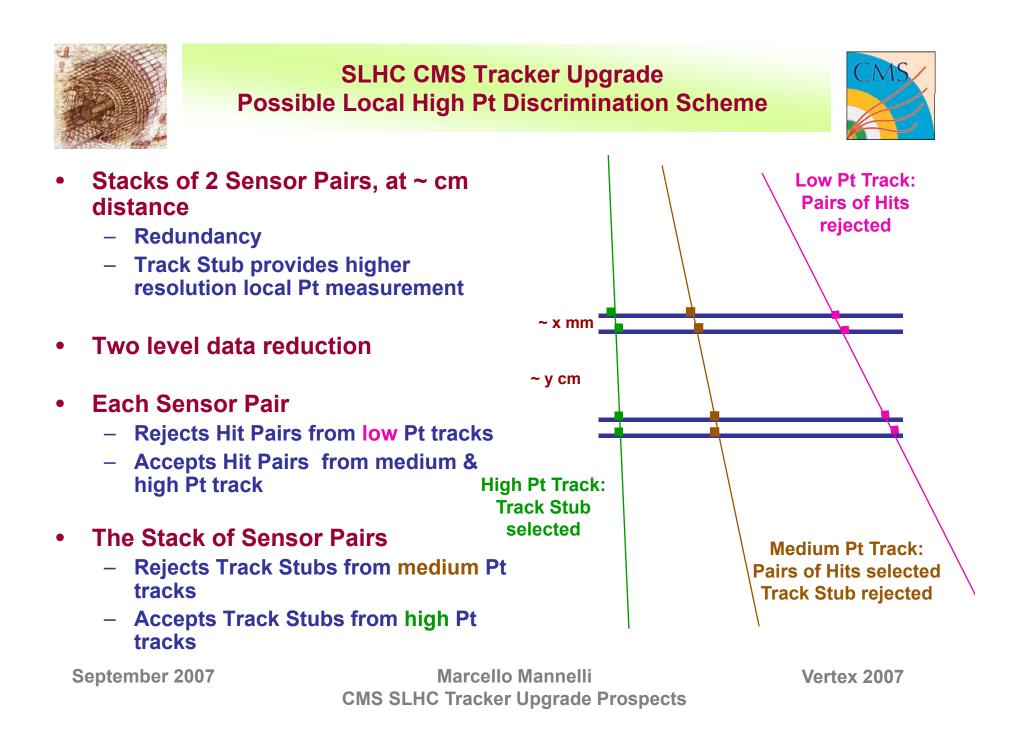


- Pairs of Sensor Planes, for local Pt measurement
- High Pt tracks point towards the origin, low Pt tracks point away from the origin
- Use a Pair of Sensor Planes, at ~ mm distance
 - Pairs of Hits provide Vector, that measure angle of track with respect to the origin
 - Note: angle proportional to hit pair radius
- Keep only Vectors corresponding to high Pt Tracks



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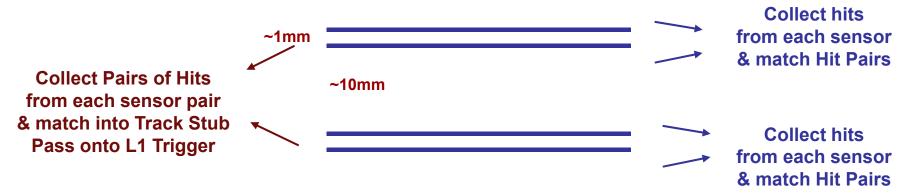




SLHC CMS Tracker Upgrade Possible Local High Pt Discrimination Scheme



Local Information Gathering, and Processing Hierarchy



- Collect hits from each Sensor in a Pair
 - Match into Hit Pairs
 - Retain Hit Pairs from medium & high Pt Tracks
- Collect Hit Pairs from each Sensor Pair in a Stack
 - Match into Track Stubs
 - Retain Track Stubs from high Pt Tracks
 - Pass onto L2 Trigger

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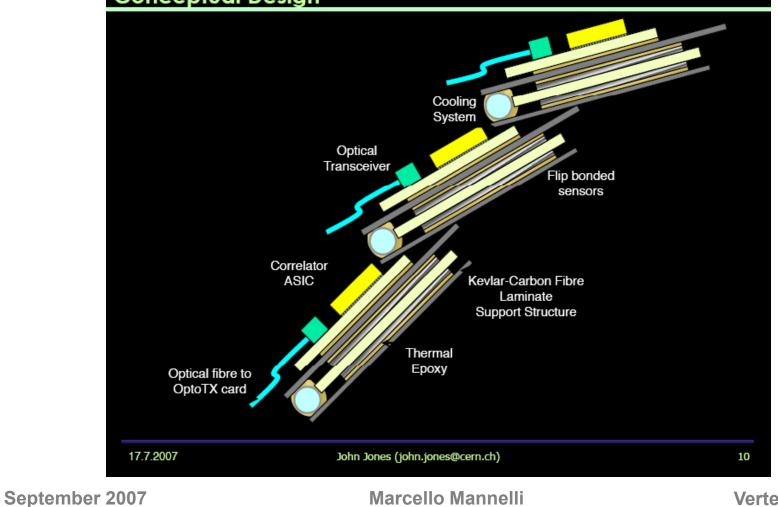
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SLHC CMS Tracker Upgrade Possible Local High Pt Discrimination Scheme



Conceptual Design



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Straw-man Layout Example

12 Measurement Layers

Organized in 3 Super-Layers

Each Super-Layer consists of a Stack of 2 Sensor Pairs (4 measurement layers / Super-Layer)

•Inner Super-Layer ~ 20~40cm (Geometry of Inner Vtx layers?)

•Middle Super-Layer ~ 60cm

•Outer Super-Layer ~ 100cm

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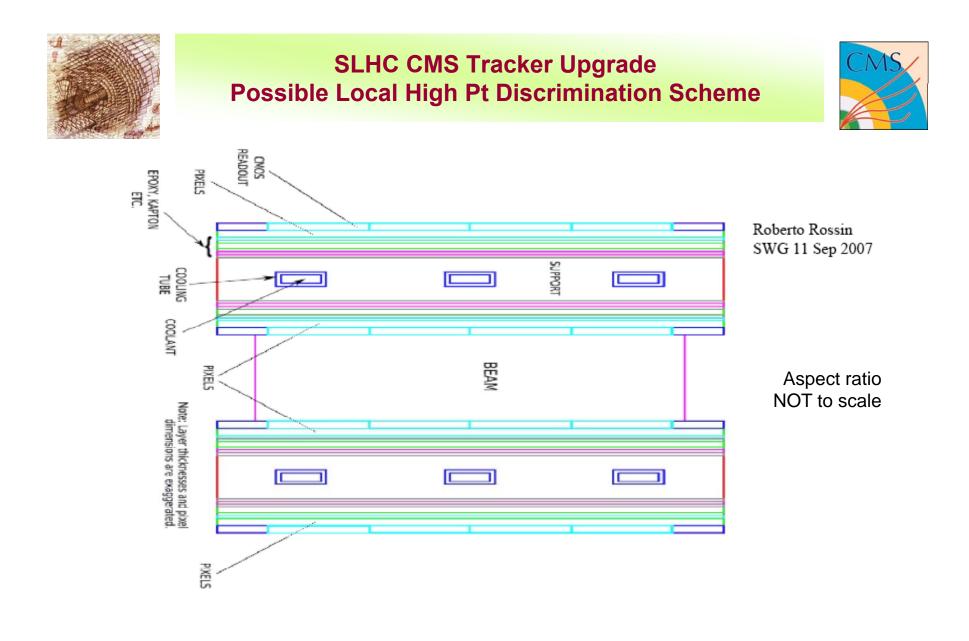
Comments:

Stack of Sensor Pairs provide opportunity for shared mechanics and services

=> May be useful approach for reducing Material Budget, independent of Local Occupancy Reduction scheme

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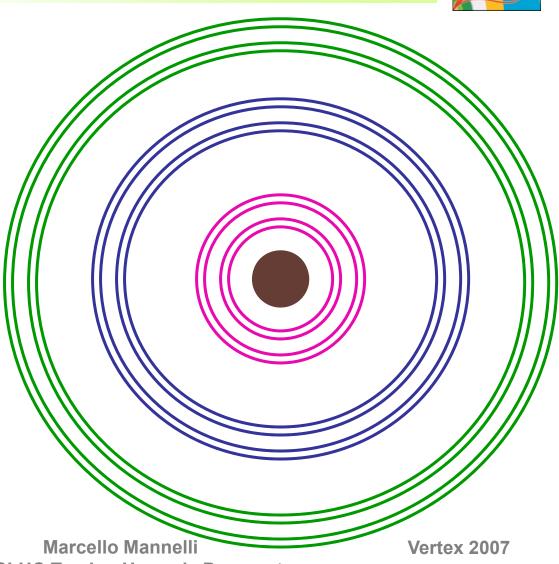
Comments:

Stack of Sensor Pairs provide opportunity for shared mechanics and services

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Drawbacks if used throughout?

Optimal arrangement & Layout?



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Basic Parameters to Vary

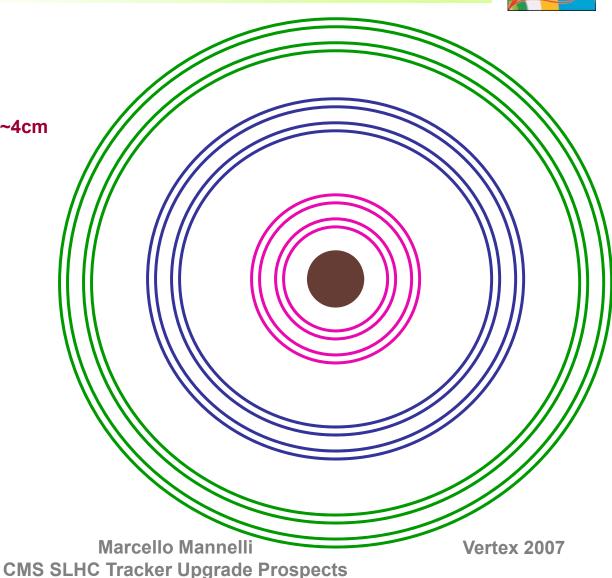
•Cell Geometry: Pitch 60~120um, Length 1~2mm/2~4cm Sensor Thickness 60~200um

•Single Hit Efficiency: 95%~99.5%

•Sensor Pair Geometry D ~ 1~4mm, Align Transverse 20~200um, Align Radial 50~200um

•Stack of Sensor Pairs: D ~ 10~100mm, Align Transverse 100~400um, Align Radial 100~1000um

•Radial Positions (10?) 20~40cm, 60~80cm, ~100cm September 2007







Basic Things to Check

•Track Quality

•Hit Pair Pt Resolution, Data Volume & Efficiency vs Pt cut

•Track Stub Pt Resolution, Fake Rate & Efficiency vs Pt cut

•Min radius at which scheme works effectively

•Fake Rate & Efficiency if require

•3/4 vs 4/4 hits in a Track Stub •1/3 vs 2/3 Track Stubs

•All the above varying the design parameters over the plausible range

•Eg. Effect of cell geometry on occupancy and resulting effect on fake rate & efficiency

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SLHC CMS Tracker Upgrade Granularity vs Power Consumption (Mass)



- The CMS Silicon Strip Tracker is extremely effective because:
 - Fine strip pitch, from 80um to 200um
 - each hit has high resolution and track parameters are rapidly constrained
 - Strip length, from 10cm to 20cm results in cell size ~ 0.5mm²
 - occupancy ~ 2% or less at 10³⁴
 - Pattern recognition converges ~ unambiguously with first few hits => fast
- At SLHC occupancy 10~20 times higher
 - Strip length in range 1 ~ 2cm to maintain low occupancy
 - Short Strips
 - Pixel length in range 1~2mm => reduce occupancy, 3D info
 - Long Pixels

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SLHC CMS Tracker Upgrade Granularity vs Power Consumption (Mass)



The present CMS Silicon Strip Tracker is extremely effective

- The performance limiting factor is NOT intrinsic precision, and most likely will NOT be our ability to align etc.
- The performance limiting factor is the Material Budget of the Tracker
- This also limits the performance of the CMS ECAL
- There is much to gained if we can lower the material budget, AS WELL AS achieving the performance requirements just mentioned

Low(wer) Mass!

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SLHC CMS Tracker Upgrade Granularity vs Power Consumption (Mass)



- The Tracker Material Budget is strongly driven by
 - Large Power Dissipation, and need for Efficient Cooling (~33kA)
 - Large Current requirements (~20kA)

Lower Power Dissipation and Current Consumption



Granularity: Short Strips vs Long Pixels



- Cost and Manufacturability are a Key Input
- Implications on System, Read-Out Architecture etc.
- Comparative Performance Studies are Important Guidance
- Reliable projections of Power Dissipation/cm² are a Fundamental Input
- Short Strips vs Long Pixels
 - Extrapolate from Strip Tracker APV25 to reduced capacitance short strips
 - Extrapolate from Pixel ROC to larger capacitance long pixel
 - Compare: Power, Material, Cost, Feasibility, Performance
- Pursue both approaches until these points are sufficiently well understood to draw some conclusions



Power Consumption of CMS Strip Tracker



- Power Dissipation of Strip FE chip (APV25) ~ 350mW (128 channels)
- Total Number of APV25 chips in CMS LHC Strip Tracker ~ 73'000
- Total Power Dissipation of CMS LHC Strip Tracker ~ 26kW
 - This is Nominal FE Chip Power dissipation
 - Actual Power dissipation is estimated at 33KW
- Note:
 - 210m² / 73'000 chips ~ 28cm² / chip
 - 350mW / 28cm² ~ 12mW/cm² (120W/m²)

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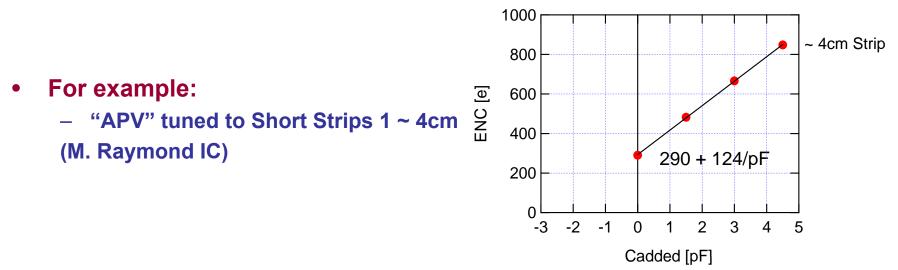
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Power Consumption for Short Strip Tracker



- Analogue Current Consumption of APV25 driven Strip Capacitance
 - $C_{strip} \sim 1.2 pF/cm$; Strip Length 10 ~ 20cm => C_{strip} 12 ~ 24pF
- For Short Strips can accept higher Noise vs C slope => reduce power



 Preamp/Shaper Power/Channel for "APV13", tuned to short strips implemented in 0.13um, may be reduced from 1mW to 0.12mW ~ 1/8



Power Consumption for Short Strip Tracker



- Assume Preamp/Shaper Power/Channel can reduced by a factor ~ 1/10
 - Is it realistic to expect overall FE chip Power Dissipation to decrease by such a factor?
- Within this architecture, likely Lower Limit for Short Strip length 1 ~ 4cm to maintain current Power Dissipation/cm²
- Are there different approaches to a Short Strip FE Chip which would allow to go to ~1cm strip length AND significantly reduce Power Dissipation/cm² ?



Power Consumption for Long Pixel Tracker



- Power Dissipation of Present CMS Pixel FE Chip ~ 30uW/channel
 - 30uW / 15'000um² ~ 200mW/cm² for current LHC Pixel
 - Compare to ~ 12mW/cm² for present LHC Strip Tracker (factor ~ 16)
- Assume SLHC Pixel size ~ 120um * 2.0mm ~ 0.24mm²
 - This implies ~ 4M Channels / m²
- Which results in ~ 12.5mW/cm² (125W/m²) ~ present Strip Tracker
- Assume Total Sensitive Area is ~ 210m²
- This results in Total FE Chip Power Dissipation ~ 26kW vs 26kW now
 - And 850M Channels...

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Power Consumption for Long Pixel Tracker



- Plausible SLHC 0.13um Long Pixel FE Chip Power Dissipation ~ 20uW/channel
 - Private communication Roland Horisberger
- IF True, this would:
 - result in Total FE Chip Power Dissipation ~ 17kW (vs 26kW)
 - leave head room for additional power dissipation (L1 Trigger, etc)
 - open possibility for reduction of overall Power Budget
- The Power consumption extrapolations shown here are speculative
 - But Interesting, and worth pursuing until reliable conclusions can be drawn

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Conclusions



- The present CMS Tracker will be a powerful tool for LHC Physics
- "Novel" approach:
 - Tracking with "few" high quality hits, in high occupancy environment
- Technology extrapolation, at "large" radii:
 - Very Large Scale Deployment of Radiation Hard Strip Sensors, with Low Power Density, Low Mass, and Low Cost
 - when proposed, the Strip Tracker represented ~ 2 Order of magnitude extrapolation from existing devices
- Technology extrapolation, at "small" radii:
 - Large Scale Deployment of Very Radiation Hard Pixels, with Low Power, and acceptable cost



Conclusions



- The CMS SLHC Tracker will be based on the present experience
 - but is required to provide Tracking and L1 Trigger capability in 10~20 times higher occupancy & radiation environment, and should be lighter
- "Novel" approach:
 - Explore schemes for local Occupancy Reduction & Pt Discrimination
- Technology extrapolation, at "large" radii:
 - Explore possibility of Very Large Scale deployment of Very Radiation Hard Long Pixels (Short Strips), with Lower Power Density, Lower Mass, and Low Cost
- Technology extrapolation, at "small" radii:
 - Large Scale Deployment of Extremely Radiation Hard Pixels, with Lower Power Density, and acceptable cost



Back-up Material



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Straw-man Layout Example

•Sensor Pair: D ~ 1mm, Cut ~ 200um

•Stack of Sensor Pairs: D ~ 10mm, Cut ~ 400um

Pt Thresholds (back-of-envelope)

•Inner Super-Layer ~ 20(40)cm Pair ~ 1(3)GeV, Stack ~ 7(13)GeV

•Middle Super-Layer ~ 60cm

Pair ~ 4GeV, Stack ~ 20GeV

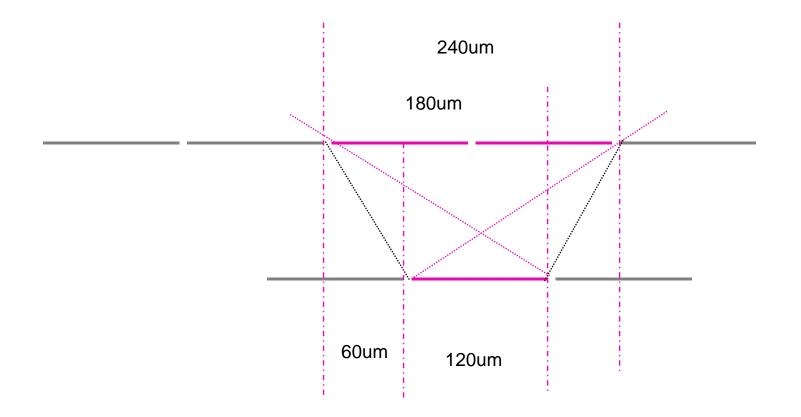
•Outer Super-Layer ~ 100cm Pair ~ 7GeV, Stack ~ 30GeV

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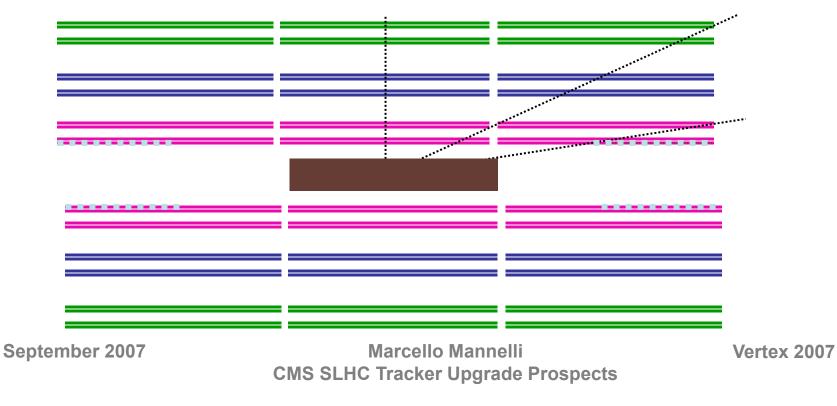


- Extend Local Pt discrimination & Triggering Capability to End-Caps
- Provide homogeneous response, until loss of lever arm due to Tracker Acceptance
- Keep it "Simple": Minimize number of variants





- Consider a Central Barrel of 3 Stacks of Sensor Pairs ~ 170cm long
- Equip Forward and Backward End-Caps with identical Barrels - 3 ~ identical Barrels, ~ 170cm long, covering the full acceptance
- Back of envelope calculation: ~ 240m²







Pros:

- "Simple" (!)
- ~ Homogenous Performance up to η ~ 1.6, in the r-phi projection
 - Constant number, Radius and Information content of hits
 - Local Pt discrimination, Pattern recognition, Track Parameters

Cons:

- Abrupt transition from 3 (2) to 2 (1) Super Layers at η ~ 1.6 (2.0)
- ~ Inefficient use of sensor active area at large η
 - Material & Costs
 - Large Cluster length variation with η
 - From ~ few um at low η -> ~ 1mm at high η (if ~ 100um thick sensors)

Is there scope for mitigating the Cons, while retaining the Pros?

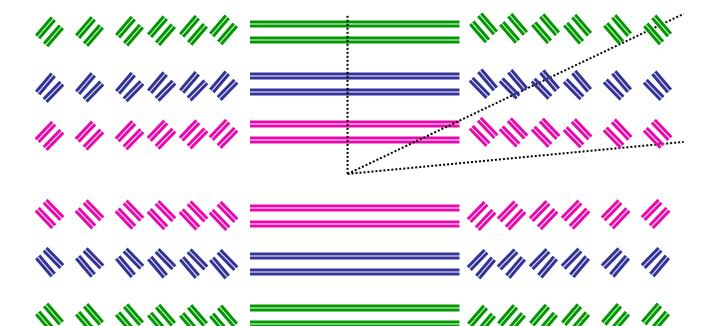
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- Consider a Central Barrel of 3 Stacks of Sensor Pairs ~ 170cm long
- Equip Forward and Backward End-Caps Barrels with Inclined Modules – 3 "similar"Barrels, ~170cm long, covering the full acceptance
- Back of envelope calculation: 160 ~ 190m²



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Pros:

- Efficient use of sensor active area at large eta
 - Significant reduction in active surface
 - Reduced Cluster length variation with eta
- May also mitigate abrupt hit coverage transitions at large eta

Cons:

- Much less "Simple"!
- Less Homogenous Performance

To be Understood

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Straw-man Layout a Word of Caution



- The Straw-man Layout shown here is Deliberately Extreme
- It is intended to highlight the Performance Potential AND the Pitfalls of new ideas, to allow informed decisions down the line



Power Consumption for Long Pixel Tracker



- Current LHC Pixel FE Chip Power Dissipation ~ 30uW/channel
- SLHC Pixel Analogue current consumption ~ same as LHC Pixel Chip
 - * 2 due to higher pixel capacitance (0.3 ~ 0.4pf vs 0.1pf current pixel)
 - * 0.5 if go from 25ns to 50ns peaking time
 - Independent of technology
- SLHC Pixel Digital current consumption ~ same as LHC Pixel Chip
 - Driven by data rates
 - SLHC data rates at 20cm ~ 1/2 of LHC High Lumi data rates at 4cm
- Analogue & Digital current consumption for SLHC Pixel ~ LHC Pixel
- Expected effect of moving from 0.25um to 0.13um
 - Overall Current Budget ~ same as present Pixel chip
 - Overall Power Budget reduced by a factor ~ 1.5
 - Mainly affecting the Digital part of the chip
- Plausible SLHC Pixel FE Chip Power Dissipation ~ 20uW/channel