Thinned Silicon Detectors

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- Motivation
- Technologies
- MPI SOI Technology
- Results
- Plans

Vertex07
Lake Placid, NY
9/25/2007

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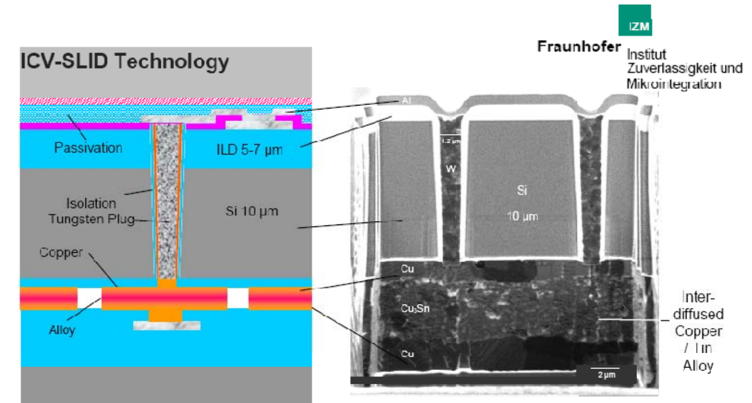
Motivation for Thinning

In Industry:

- Flexible electronics (smart cards)
- Reduced power consumption
- Vertical (3D) integration



Particle Physics:

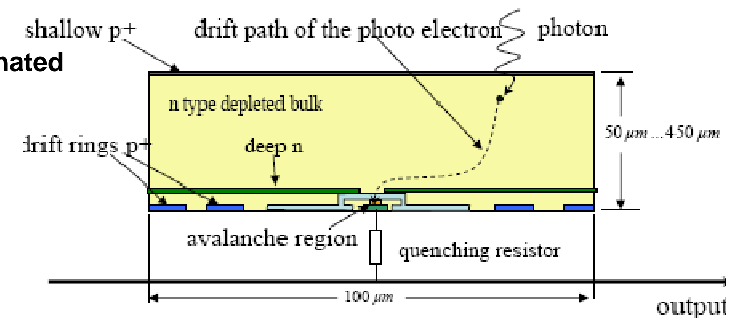
Material Reduction:

- High precision vertexing (& tracking) detectors demand low material budget
- ILC aims for 0.1% X_0 per layer
- X_0 for Si: 9.26 cm => 0.1% corresponds to 100 µm Si!
- Need mechanical carrier, readout & control ASIC, interconnection material
- Sensitive area has to be ~50 µm thick!

Lower leakage currents and operation voltage for back illuminated devices

- $V_{dep} \sim d^2$
- $I_{leak} \sim d$

Example: Back-illuminated SiPM



Detectors measuring dE/dx

Improve radiation tolerance: sLHC: 10^{16} n/cm^2

Trapping in highly irradiated detectors

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Highly irradiated detectors ($\phi > 10^{15}$ n/cm²)

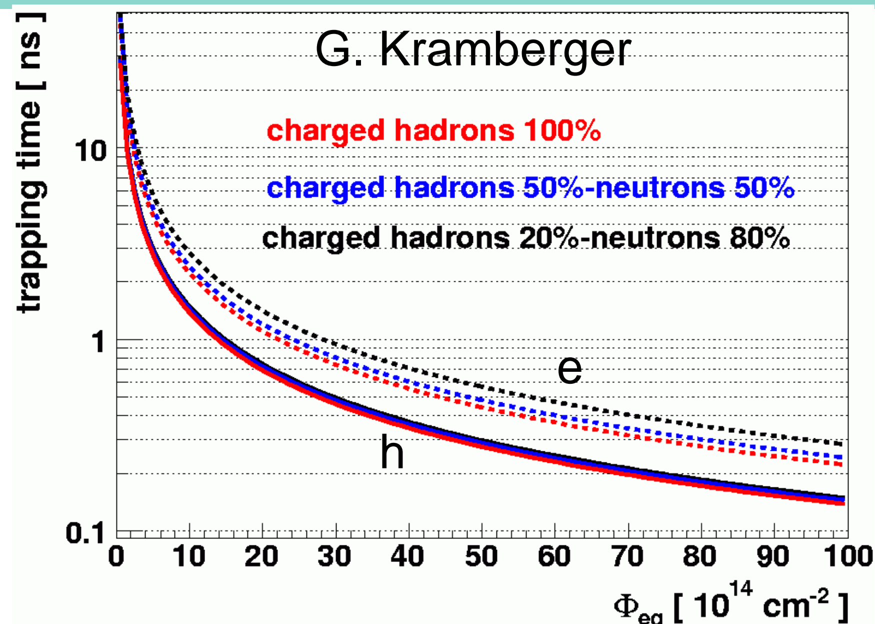
- **Large leakage currents**
- **Large depletion voltage**
- **Low CCE due to trapping**

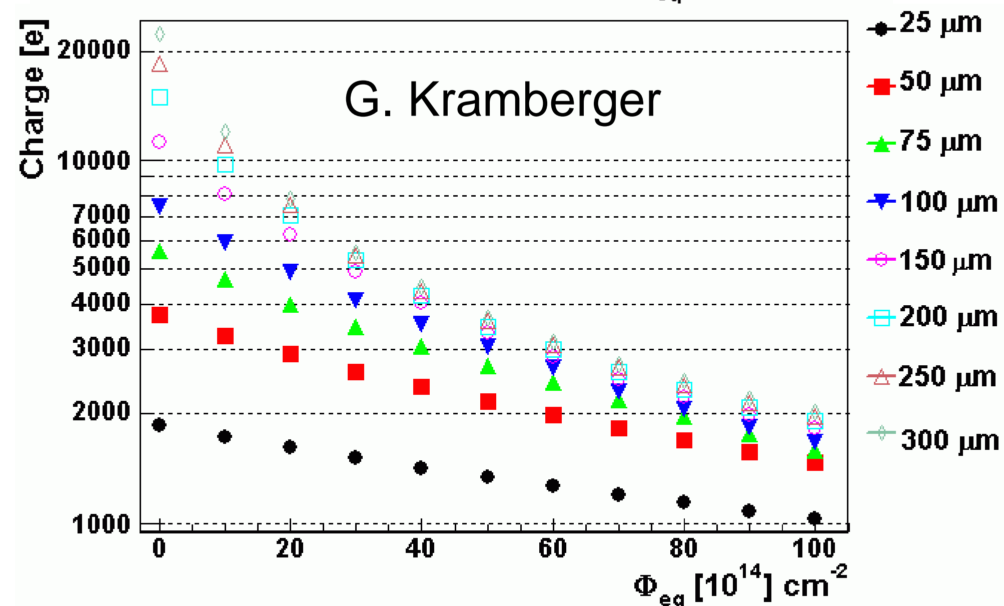
$l_{drift} < d_{det}$

Thin detectors can give the same signal!

However: thin detectors have always a small signal, even before irradiation!

Low noise electronics necessary!





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Electric field and drift velocity

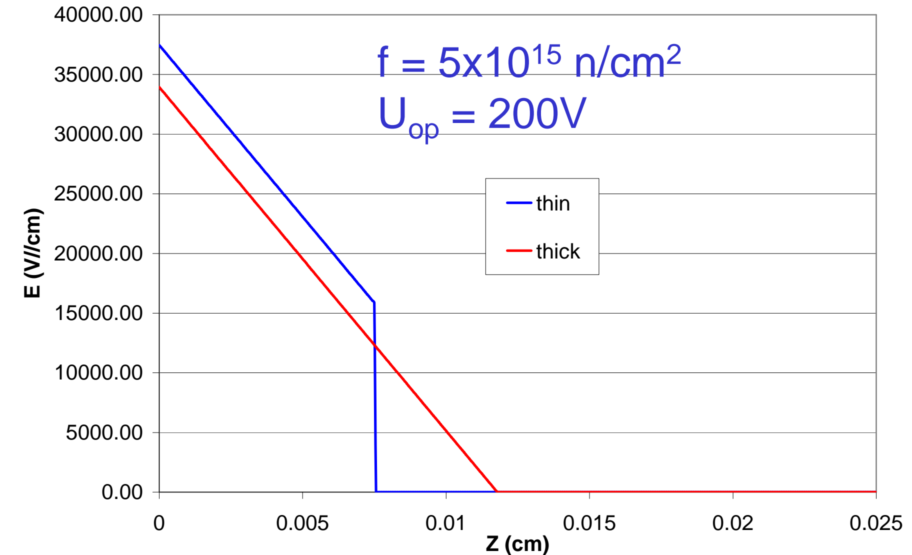
Is there an advantage of thin detectors?

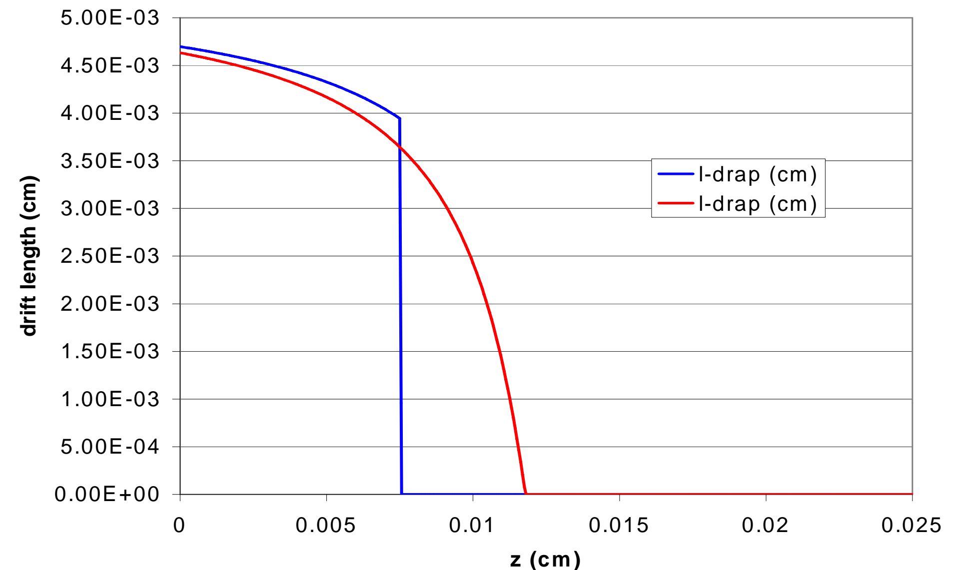
At the same voltage thin (=over depleted) detectors have a higher electric field than thick (= partially depleted) detectors

⇒Higher drift velocity
⇒Better CCE

(unless $v_{drift} \sim v_{sat}$)

In addition the depleted volume of thick detectors is larger
⇒Larger leakage currents (shot noise, heat)
⇒Additional volume does not give a signal ($l_{drift} < z_{dep}$)





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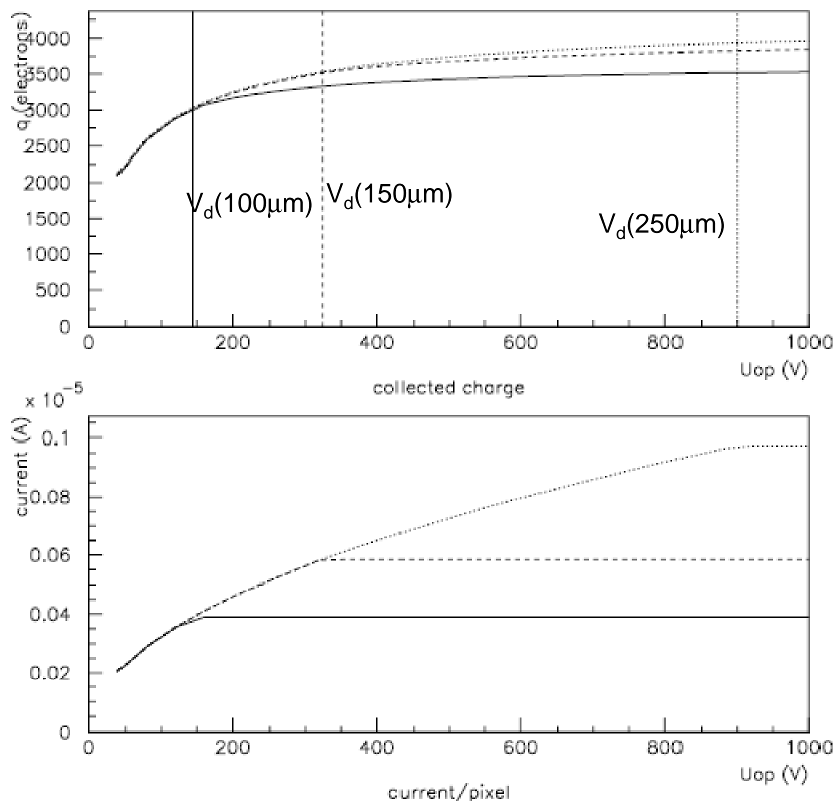
Charge Collection

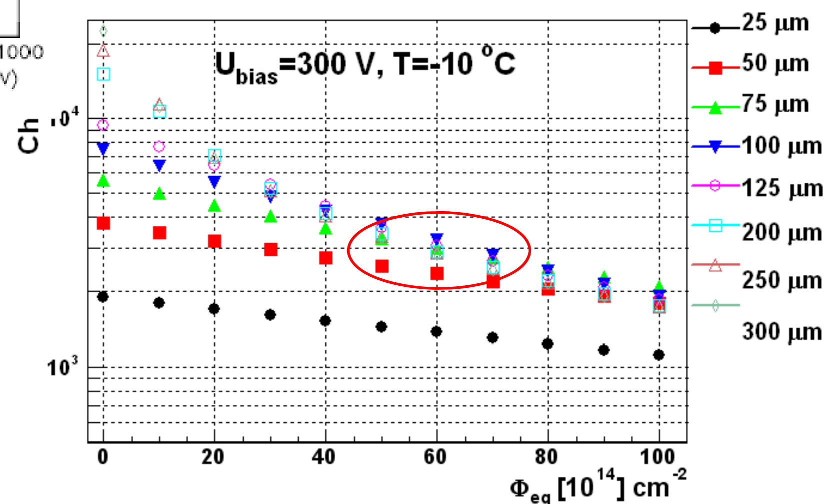


Irradiation to 5×10^{15} n/cm^2

Thicknesses: 100 µm V_d=150V
150 µm V_d=325V
250 µm V_d=900V

At 350 V the 100 µm detector collects 95% of the charge of the thicker detectors but at much less leakage current!

The example above assumes a planar diode.
For segmented detectors CCE is affected by the weighting field.
Signal (thin) > signal (thick) possible!
(G. Kramberger)



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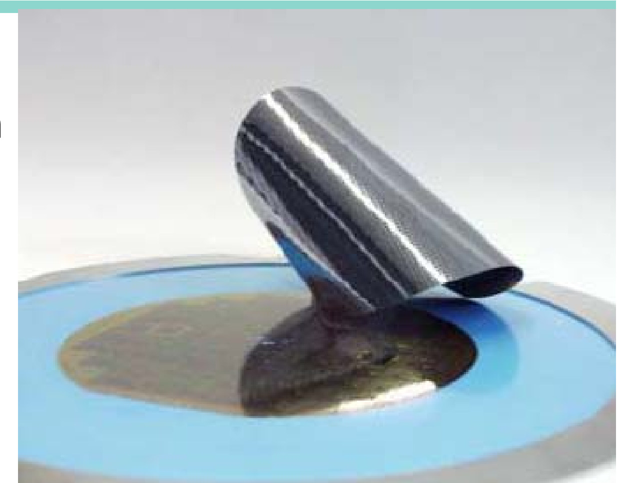
Methods



Processing thin wafers

In principle: wafers can be thinned to ~ 10 μm

Standard thickness:

~ 300 μm (4”) -> 250 μm

~ 500 μm (6”) -> 300 μm

Wafers below this thickness become fragile.

Reduced yield, non standard processing.

Problems in automated batch processing lines.

Not recommended and many manufactures will refuse to do it.

(140 μm detectors on 4” wafers made by Micron Semiconductor: see G. Casse)

Back thinning of processed wafers/chips

“standard procedure for CMOS wafers/chips”

Wafer/chip need to be glued on a carrier

No back side processing possible

(except: laser annealing,

e.g. for back thinned CCDs)

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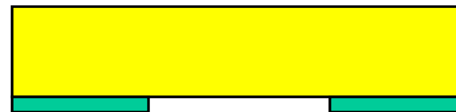
Methods

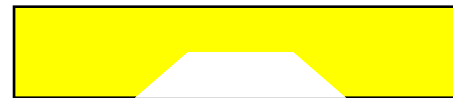
Backside processing:

High temperature steps (diffusion or annealing after ion implantation) incompatible with already processed front side (e.g. aluminium)

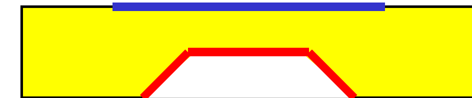
Etching of thin, small windows, process after etching



Mask windows



Thinning by etching



Process both sides

Without etch stop: difficult to control thickness and uniformity
use etch stops:
a) highly doped epi-layers: ok, but perhaps this is not the material you want for detectors
b) buried oxide layer in SOI wafers

Processing after thinning: limits the size of the thinned devices!
Difficult for large area devices (> ~ cm^2)

Is it possible to do all high temperature steps before etching?

Thinning Technology at MPI Semiconductor Laboratory

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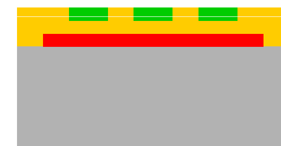
1) Process backside of thick detector wafer (structured) implant.

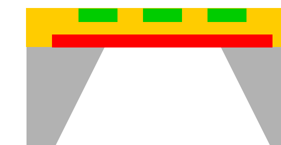
2) Bond detector wafer on handle wafer.

3) Thin detector wafer to desired thickness (grinding & etching).

4) Process front side of the detector wafer in a standard (single sided) process line.



5) Etch handle wafer.
If necessary: add Al-contacts
Leave frame for stiffening and handling, if wanted



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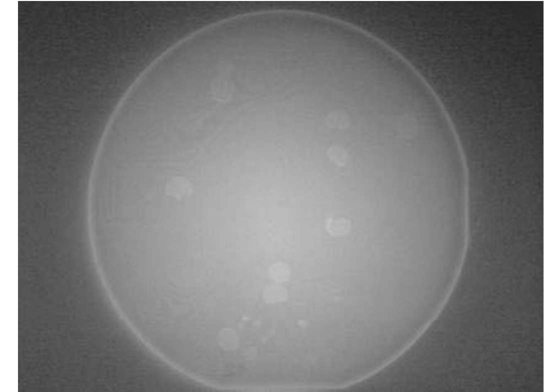
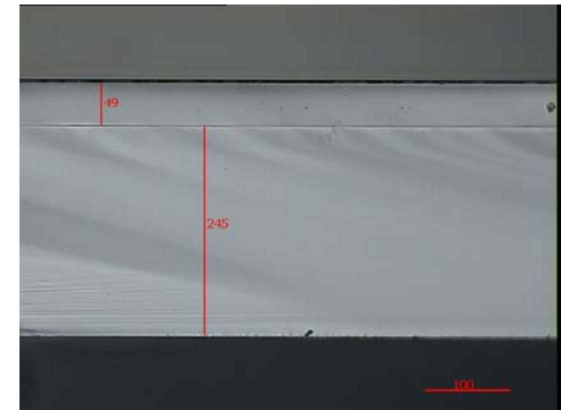
SOI Wafer Bonding

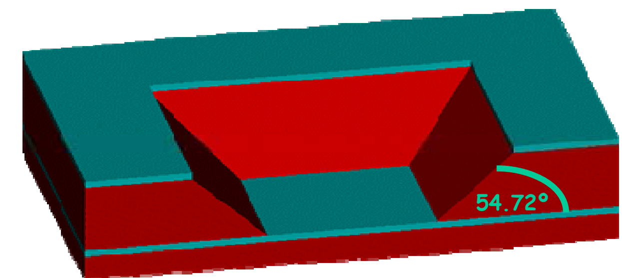
SOI wafer bonding: done in industry (TRACIT, France)
Good quality, almost now voids



Thinning of handle wafer to (almost) any thickness. Stack can be handled like a normal wafer
Handle wafer is a perfect protection of the detector backside!
Single sided processing even for n-in-n detectors



Selective anisotropic etching by TMAH
Tetramethyl Ammonium Hydroxide



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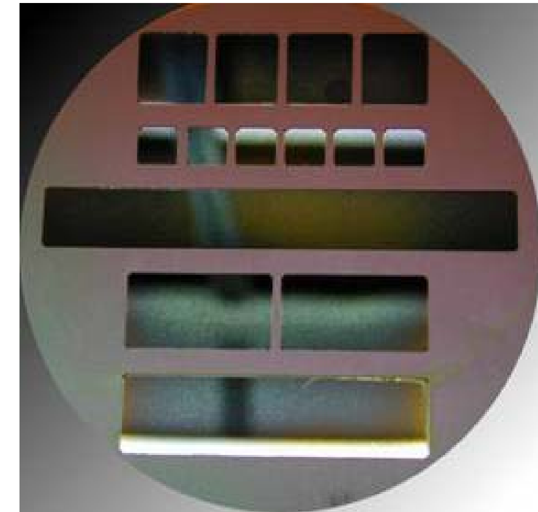
How thin can we get?

Tests made with 4 inch wafers
Mechanical dummies, no processing

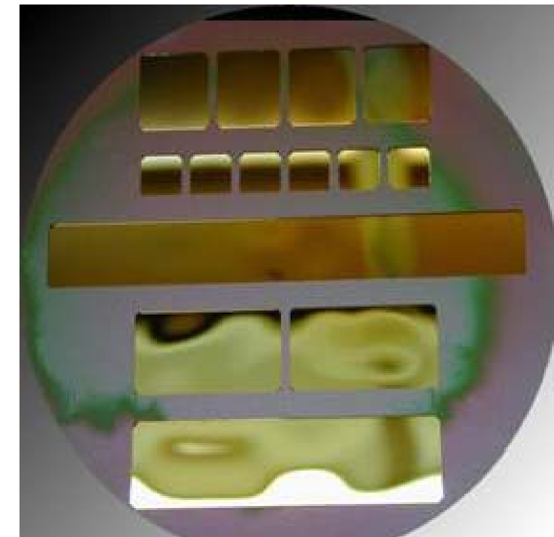
50 μm: no problems

< 50 μm: Si becomes “fexible” and
surface gets distorted
Depends on window size
Probably worse for processed wafers
(CTE mismatch of SiO and Al layers

However: no damage!



51 μm



26 μm

Thinning : mechanical samples

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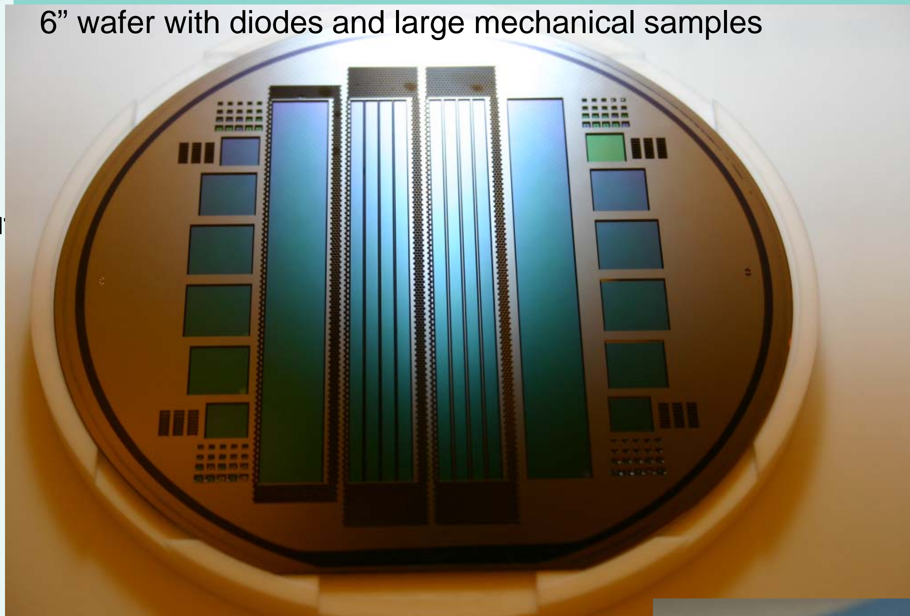
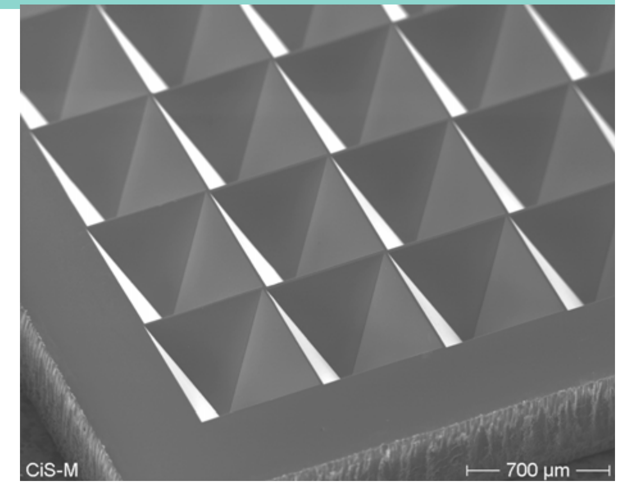
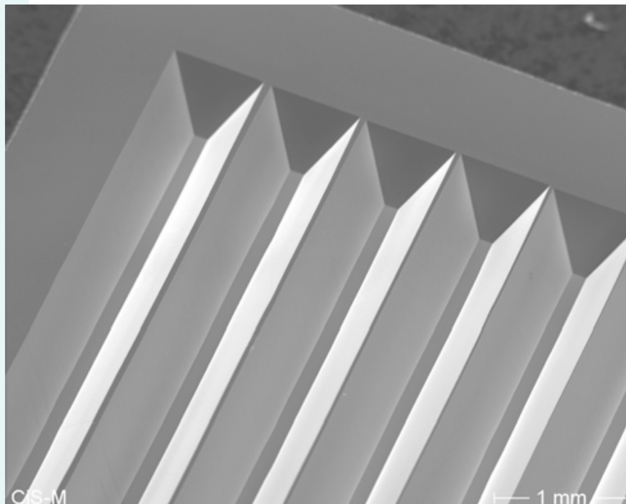
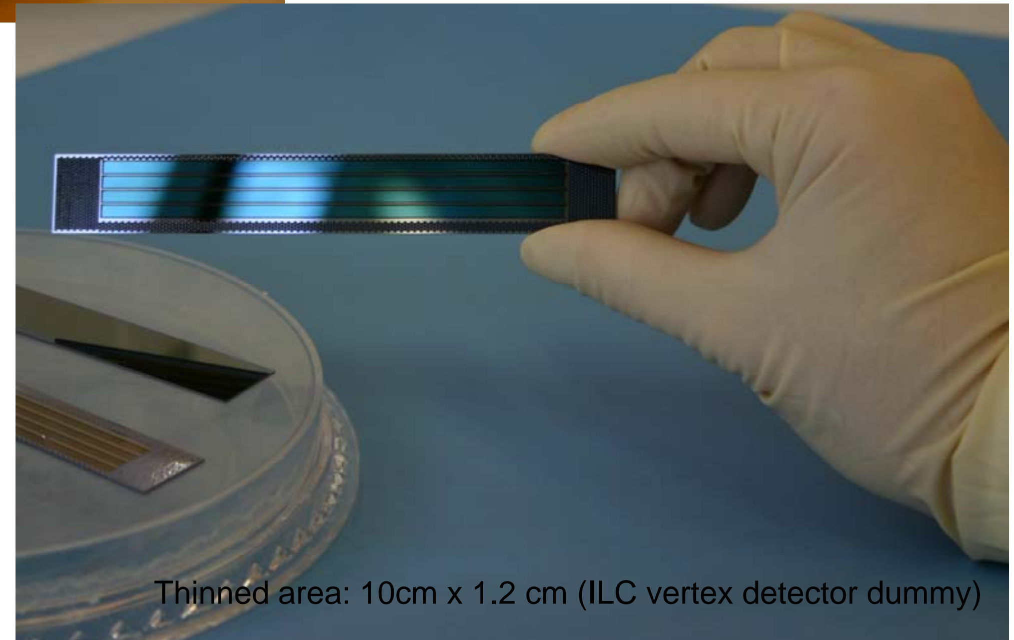
6” wafer with diodes and large mechanical samples





Possibility to structure handling frame
(reduce material, keep stiffness)





Thinned area: 10cm x 1.2 cm (ILC vertex detector dummy)

Mechanical Properties

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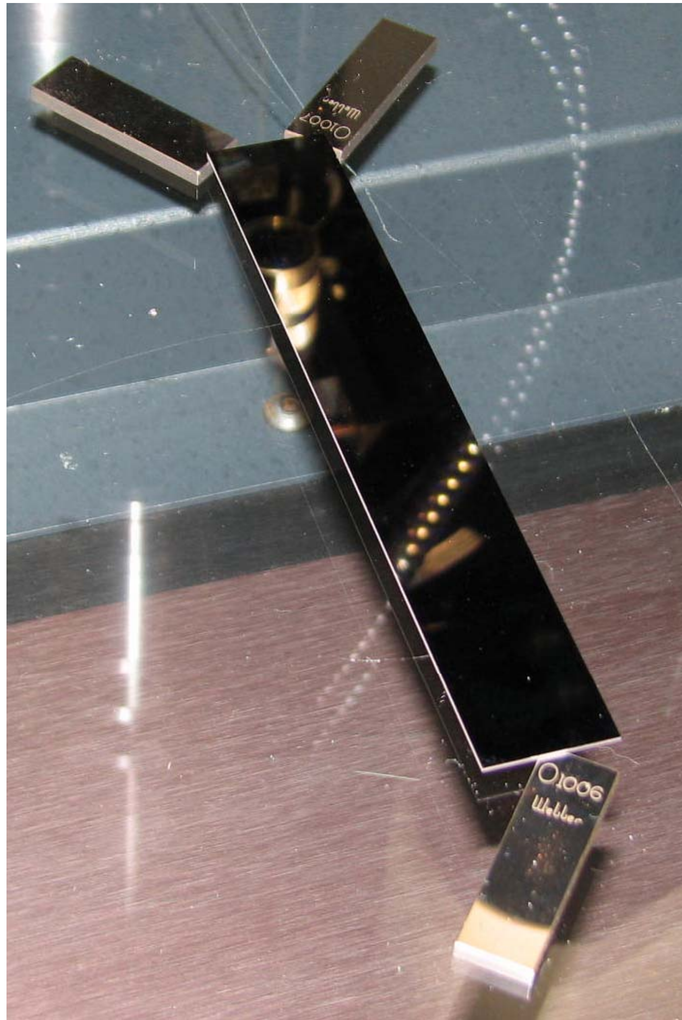
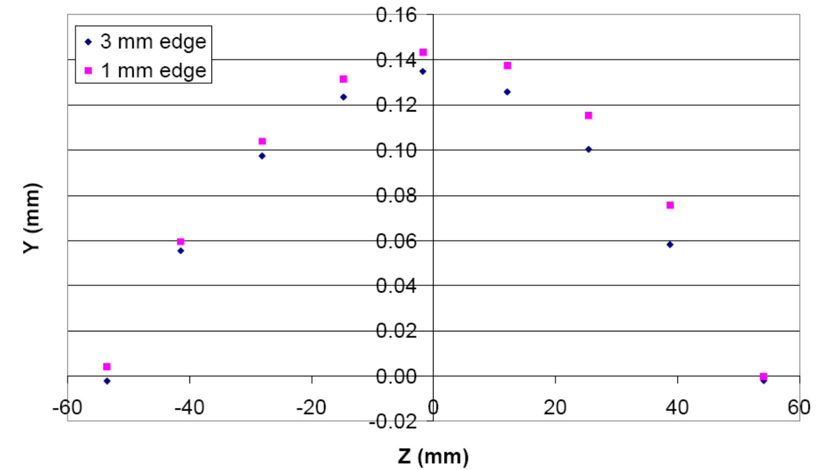
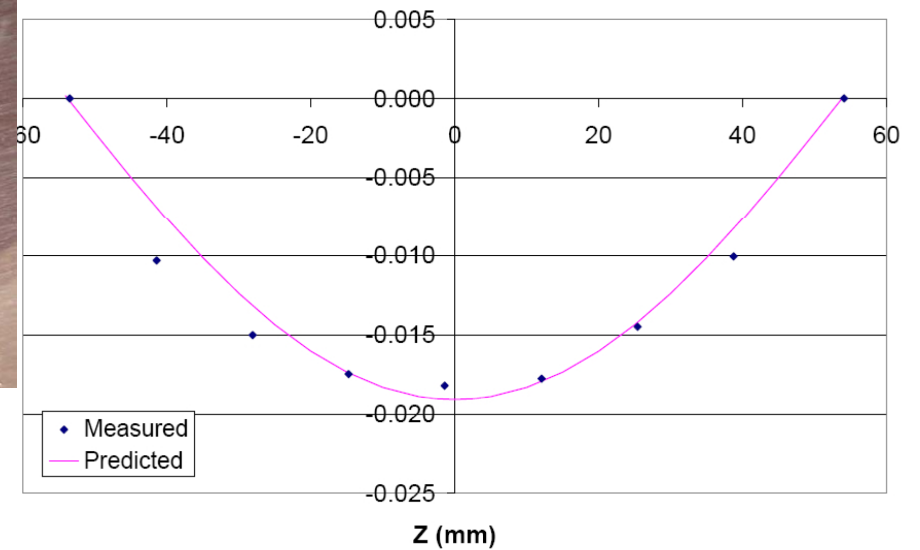


Bill Cooper, Fermilab





PiN Diodes on thin Silicon

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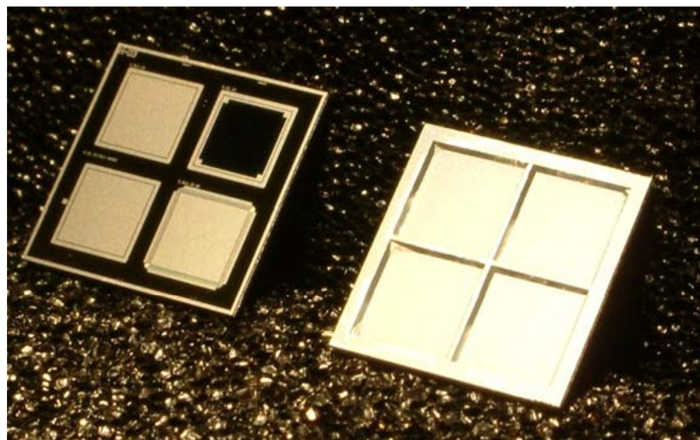

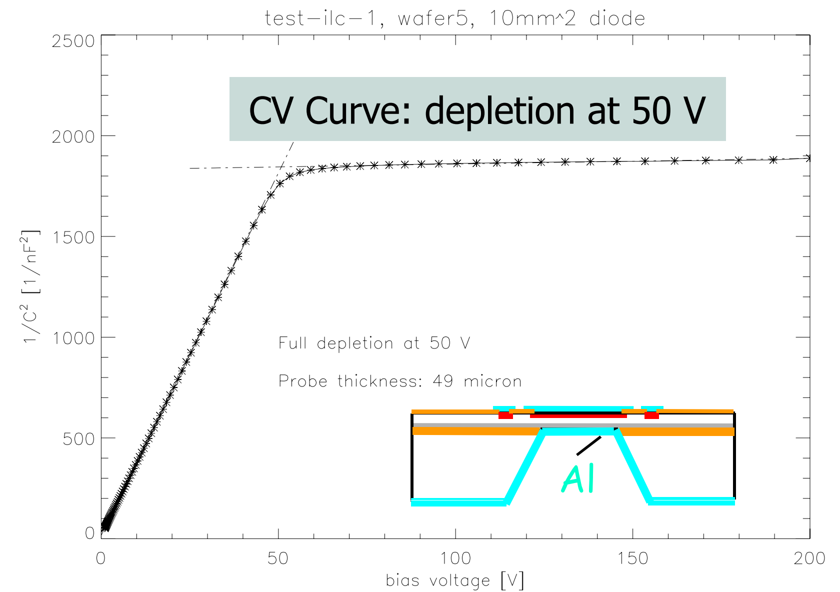

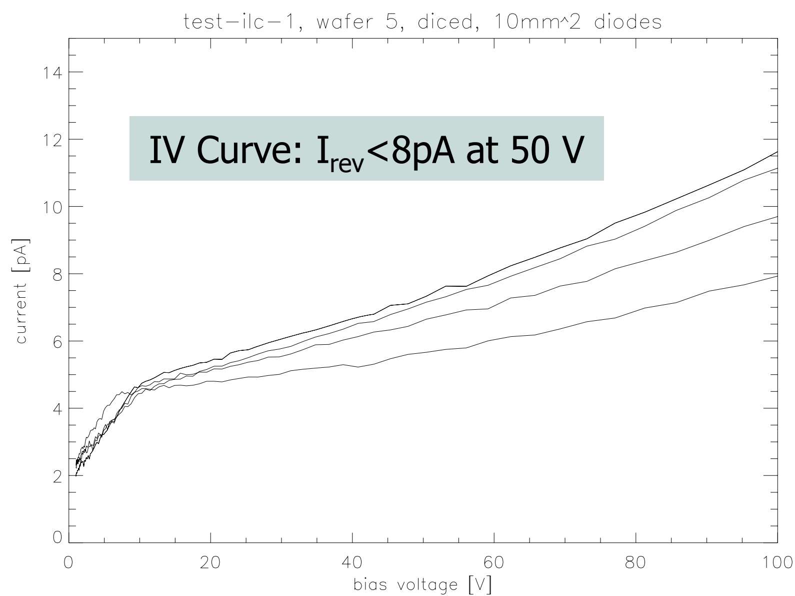

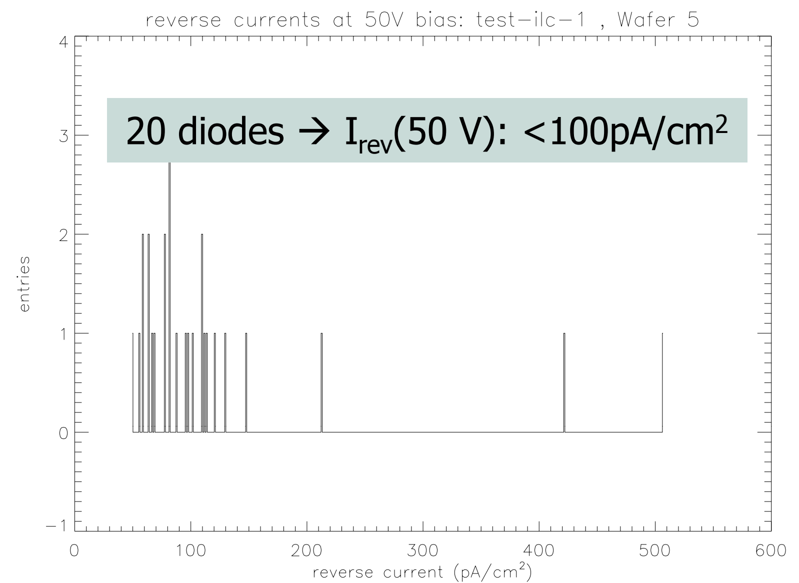

Irradiations

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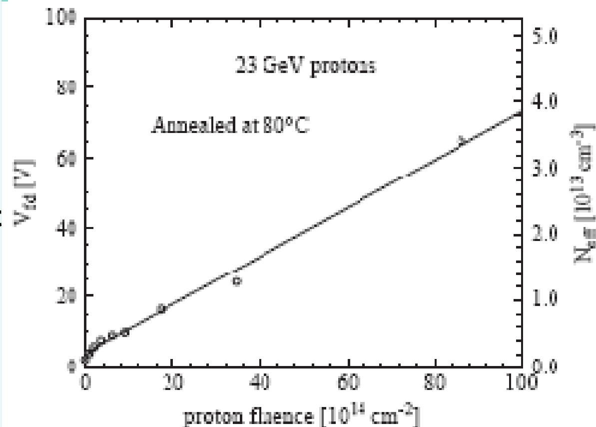

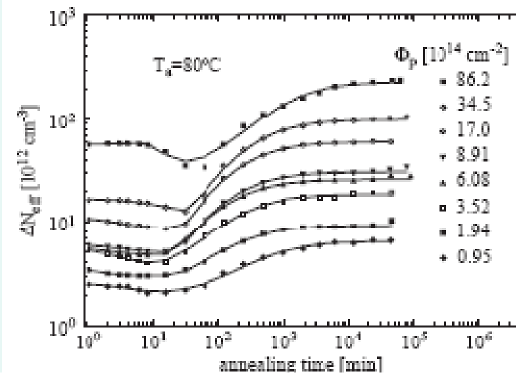

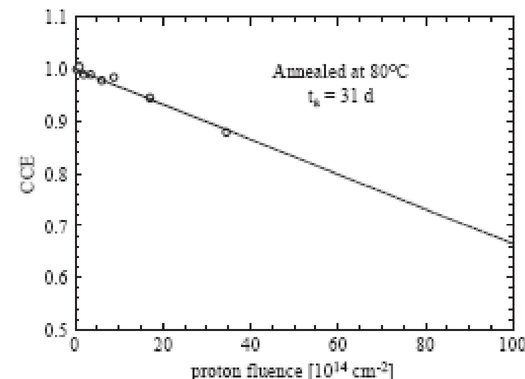

Proton irradiations of PIN diodes (50 µm, n-type)

Fretwurst et al. NIM A 552 (2005)

After short term annealing:
Leakage currents:
a(80°C, 8min) = 2.4 x 10^{-17} A/cm

V_{dep} < 100V at 10^{16} p/cm^2

However, detectors need to be kept cold (avoid reverse annealing!)

With $N_{eff}= |N_0 exp(-c^*\phi) - \beta\phi|$
β= 3.6 x 10^{-3} 1/cm
(like oxygen enriched material)

50 µm: CCE ~ 66% @ 10^{16} p/cm^2
2600 el (extrapolated)

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Actual Projects: Large ILC type structures

Large (10cm x 1.2 cm) ILC module like structures, 50 μm thick

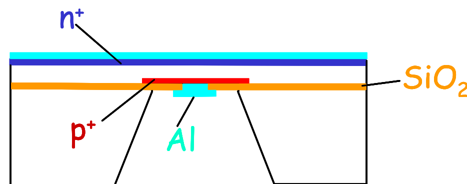
Instrumented with MOS diodes and strip-like patterns
Smaller test diodes and MOS structures

Backside implant like needed for DEPFETs (structured p-implant)

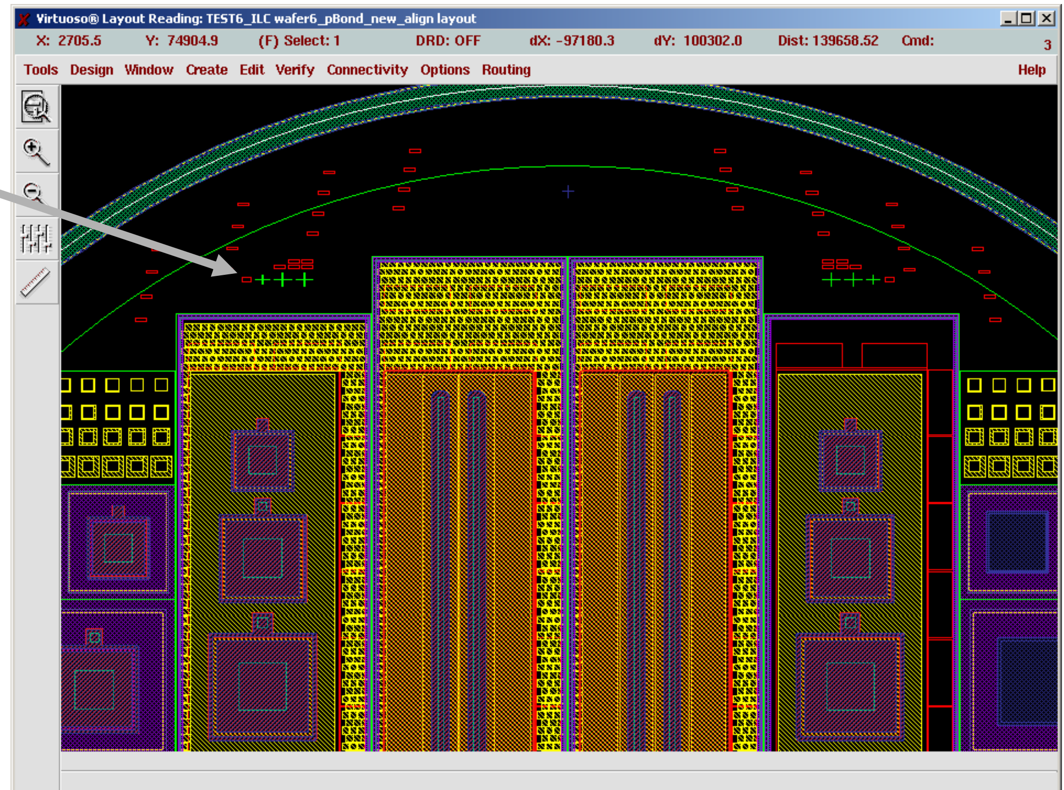
Processing of real thinned DEPFETs scheduled for 2008/2009

Alignment marks in BOX to find the partial p-implant after bonding

Implants like DEPFET config.



unstructured n+ on top
structured p+ in bond region



sLHC Pixel Detectors

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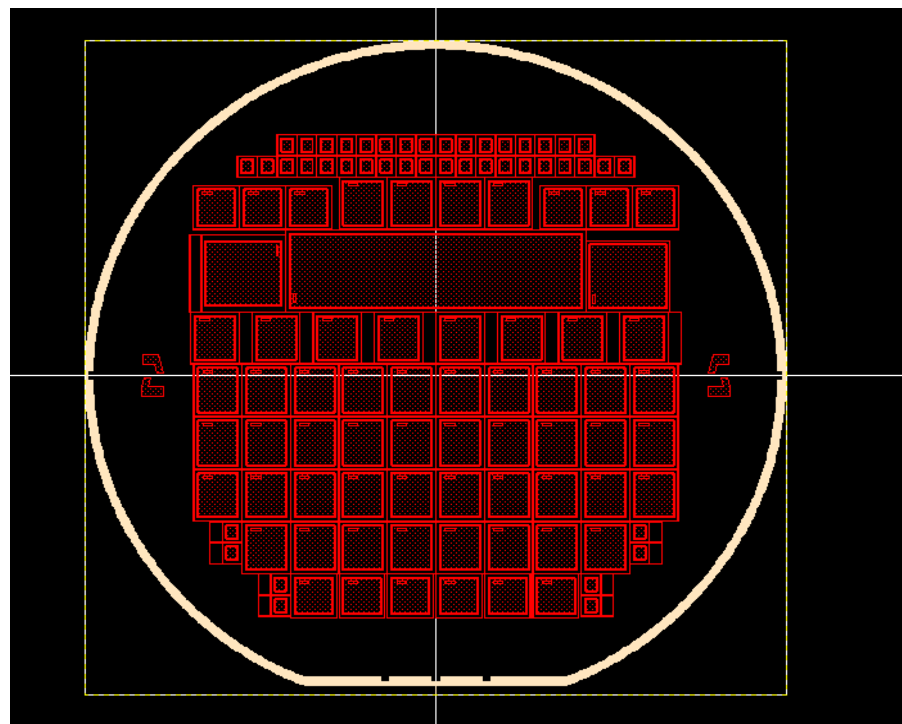
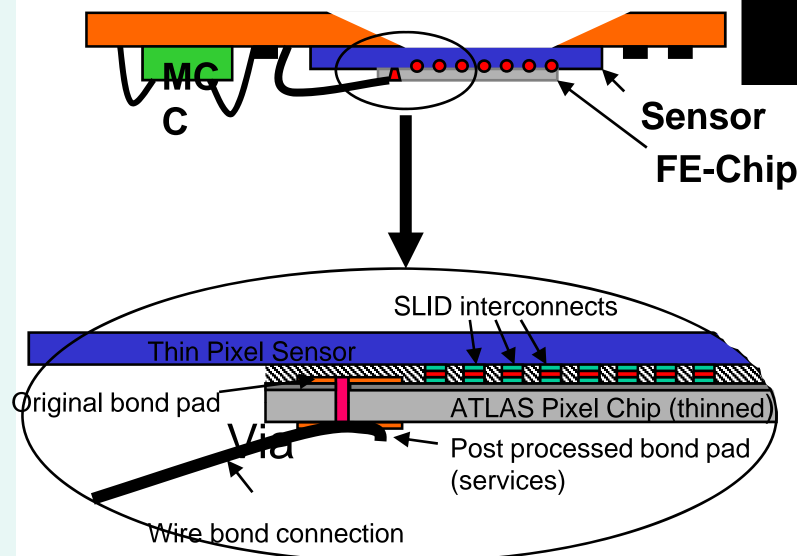
R&D for the sLHC upgrade of the ATLAS pixel detector.
Should withstand 10^{16} n/cm^2

Pixel and mini-strip structures
ATLAS pixel module
n-in-n and n-in-p design
75 μm and 150 μm thick





Objectiv:
Demonstrator using a thin detector Interconnected to a (thinned) ATLAS pixel FE chip using 3D interconnection technologies (vias)

See talk by Marc Weber

Summary

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Processing of thin wafers (< 150 µm, though available) highly non-standard: expensive, not for large scale production.

Back-thinning of processed wafers is industry standard
Thicknesses of ~10 µm can be made.

Problems for detector production if backside processing (uniform or structured is needed, for fully depleted devices).

Solution: SOI wafer and thinning by etching after processing.
Rather conventional process which can be done in industry.

Possible applications:

- sensors for low material precision tracking detectors.
- sensors for highest radiation levels.

First results very promising (electrical, mechanical, rad. hardness).