Monolithic Pixel Sensors for the ILC

Vertex 2007, International Workshop on Vertex Detectors

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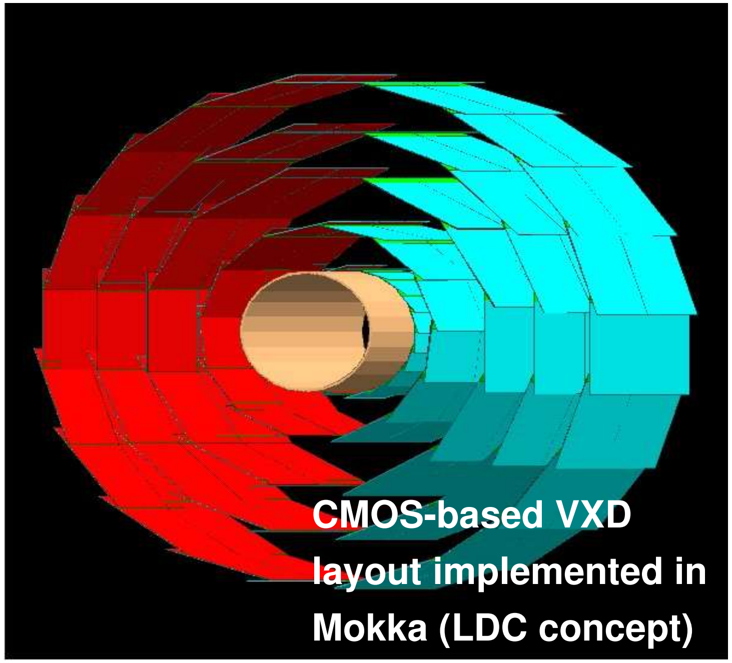
Outline

- Introduction: ILC Vertex Tracker requirements
- Monolithic Active Pixel Sensors for the ILC VXD
- Current R&D trends
- VTX design and integration
- Conclusions

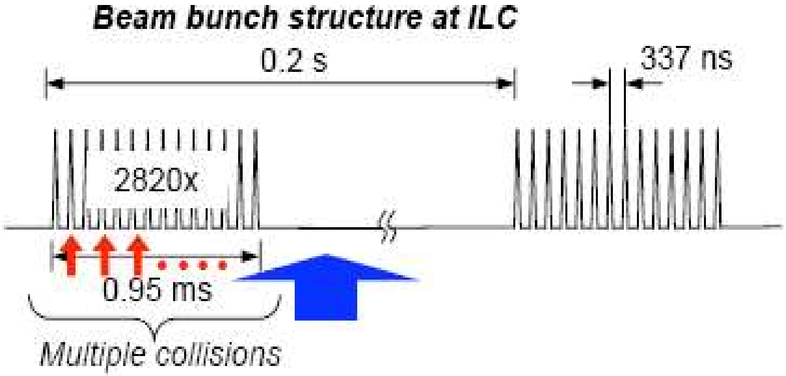
The ILC Vertex Detector

Precision measurements at the ILC will need a vertex detector of unprecedented performance:

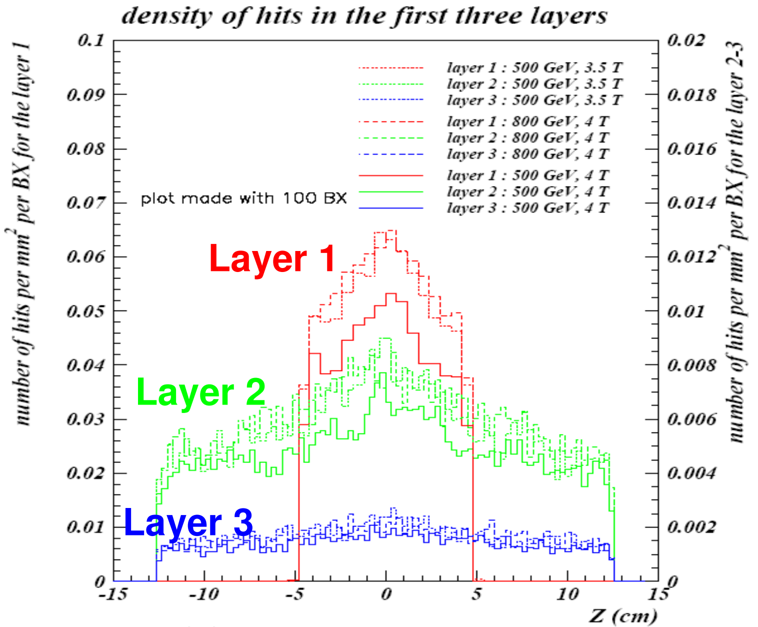
- **High impact parameter resolution**
  - **High granularity**: $\sigma_{sp}<5$ µm → 20 µm pitch pixels with analog readout, 10-15 µm pitch with binary readout
  - **Low multiple scattering**: ~0.1% X_0/layer→ 25-50 µm thin sensor layers, low power dissipation
- **High occupancy**, mainly from **e^+e^- pairs background**
  1) **Fast readout** of full detector multiple times during bunch train
  2) **Local storage of signals** during bunch train, read out during beam-off period (ILC duty cycle 0.5%)
- **Radiation hardness:**
  - Ionizing dose: 50 krad/yr
  - Neutrons: 10^{10} $n_{(1\ MeV)}/cm^2yr$
  - ~10 MeV electrons: 6×10^{11} e/cm^2yr
- Possible **EMI sensitivity**



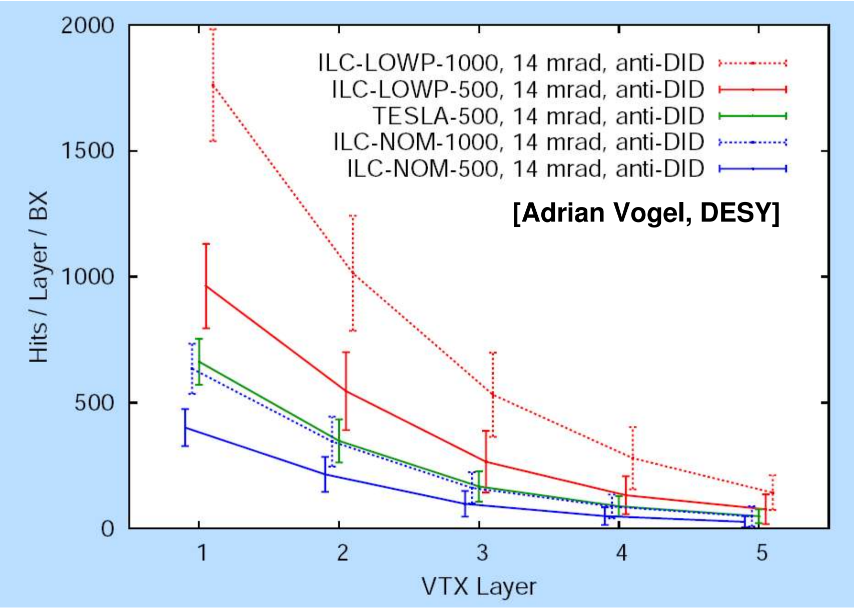
CMOS-based VXD layout implemented in Mokka (LDC concept)



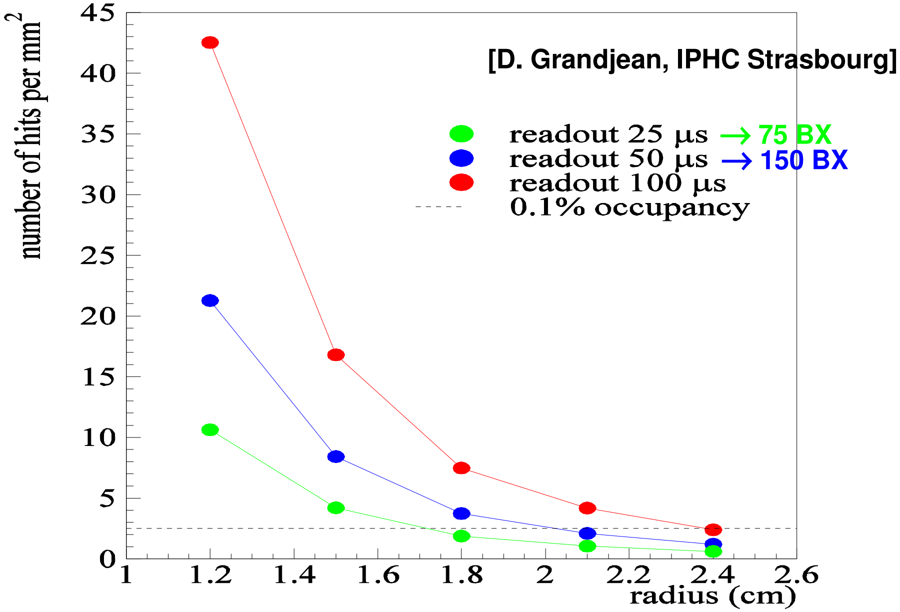
Constraints from background in the VXD



[D. Grandjean, IPHC Strasbourg]



[Adrian Vogel, DESY]

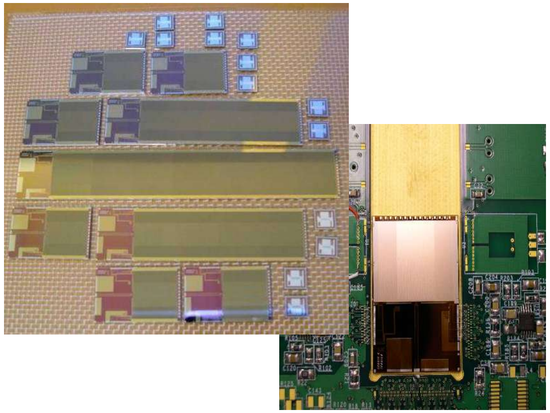


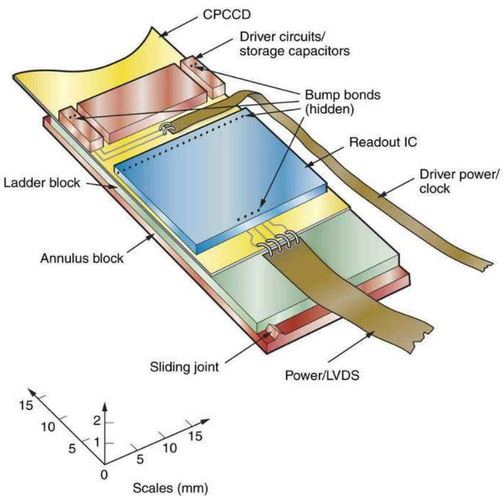
[D. Grandjean, IPHC Strasbourg]

- Background mainly due to low momentum e$^+$/e$^-$ from beamstrahlung photons (due to strong focus of the beam) plus back-scattered photons, neutrons and charged particles
- High occupancy in the vertex layers → constraints on readout speed and data volume
- Necessity for radiation hardness assurance against low momentum (~10 MeV) electrons

Candidate sensor technologies (simplified)

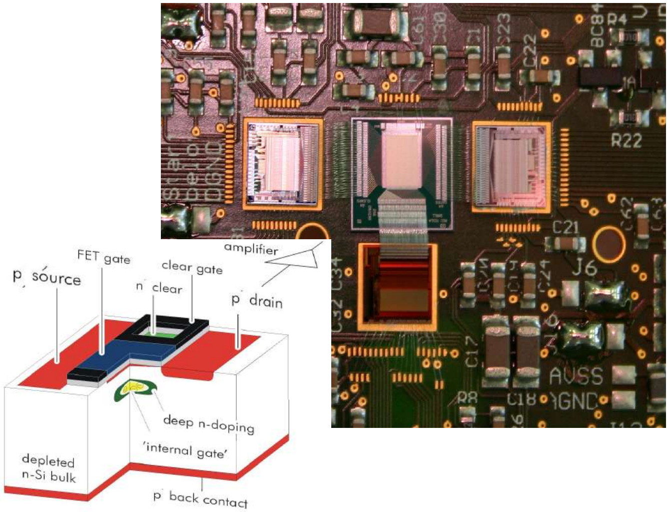
CCDs

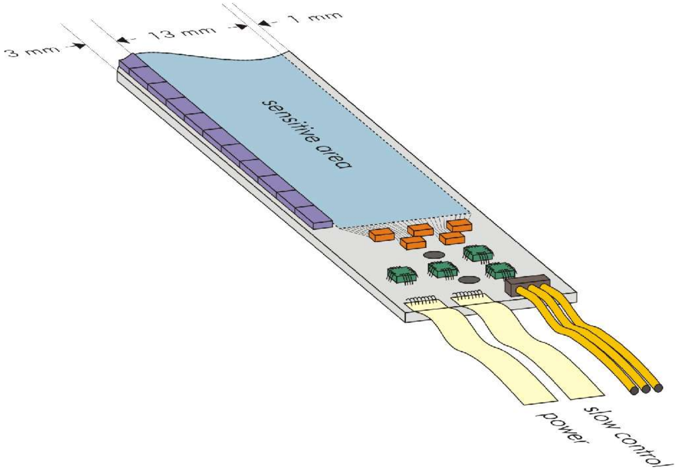




[see talk K. Stefanov]

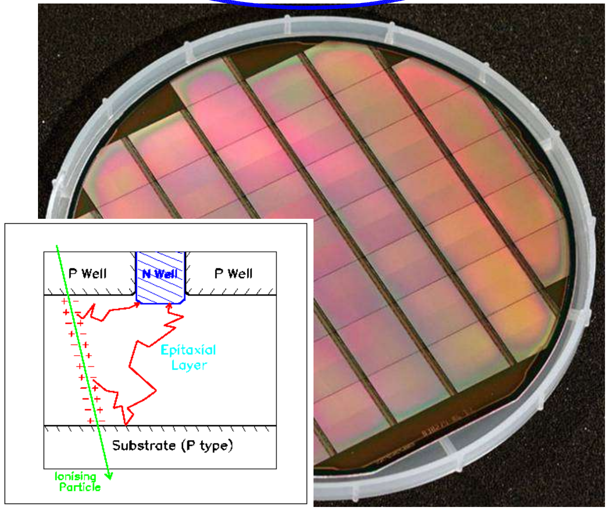
DEPFET

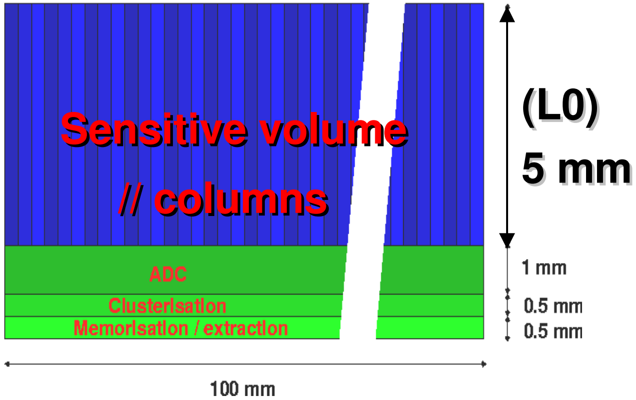




[see talk H.-G. Moser]

MAPS



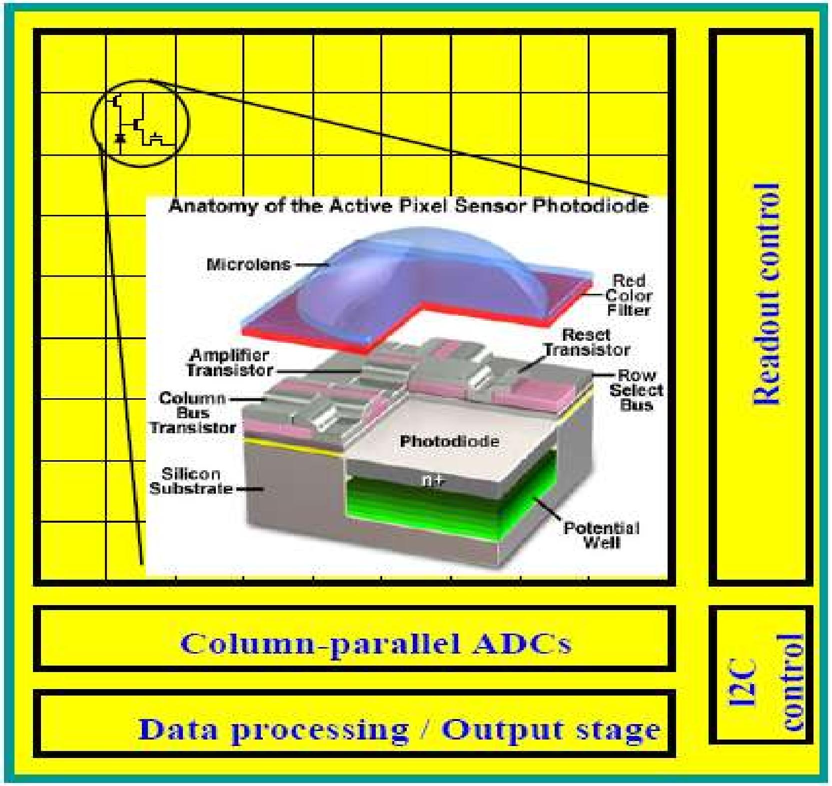


[see also talks P. Lutz, G. Traversi]

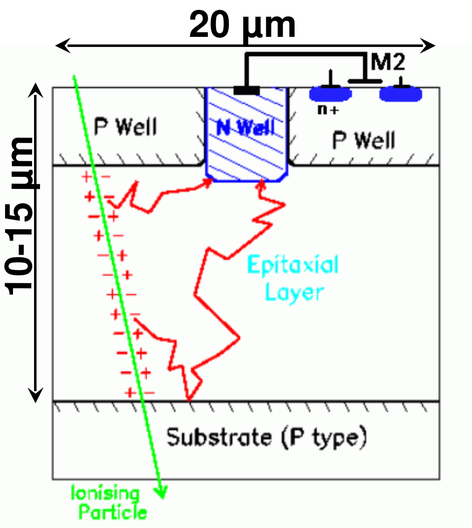
MAPS: from imaging to particle tracking

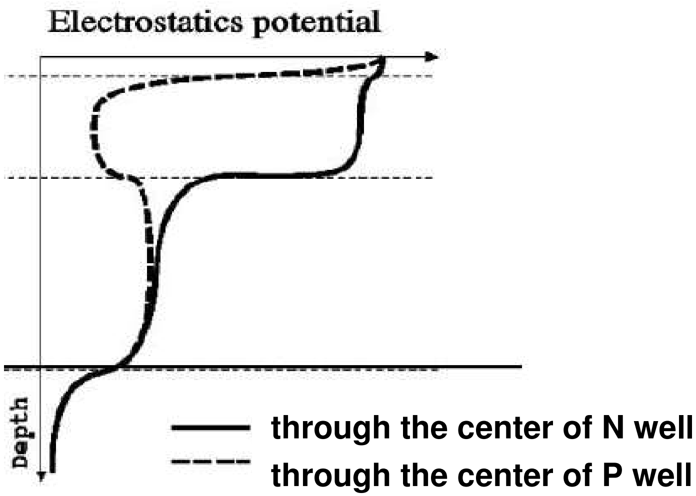
- **Early '90s: CMOS Monolithic Active Pixel Sensors introduced as an alternative to CCDs in visible light imaging**
- Use of standard **CMOS technology**
- **Monolithic**: sensor and readout electronics on the same substrate
- **Active pixel**: an amplifier integrated in each pixel directly buffers the charge signal
- **Advantages**:
  - Low cost
  - Low power dissipation
  - Random access
  - Increased functionalities...

... but **poor fill factor**, i.e. fraction of pixel area which is sensitive to radiation → **not applicable in charged particle tracking**



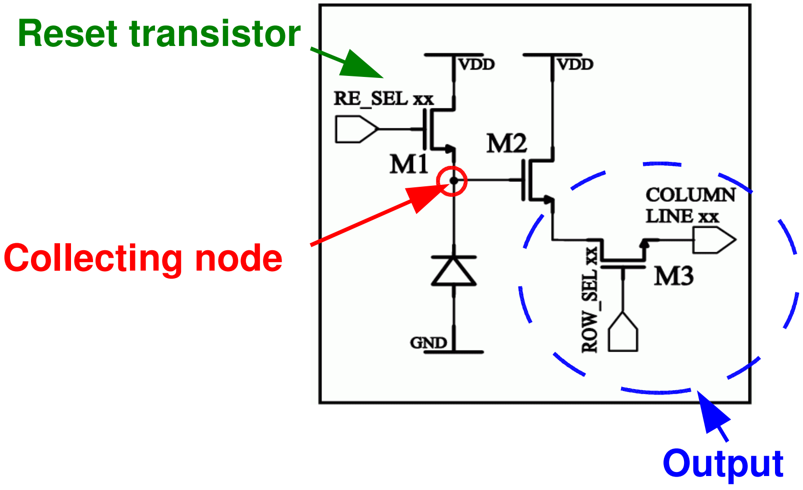
MAPS for charged particle tracking



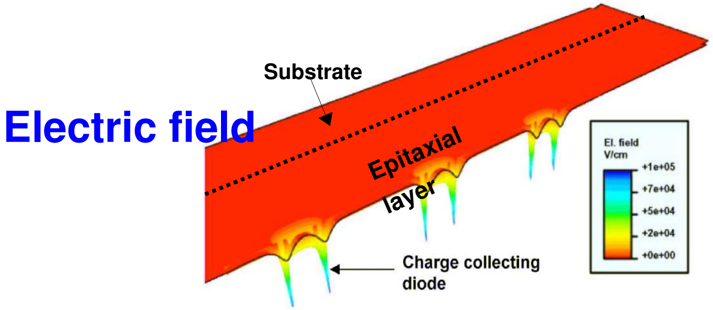


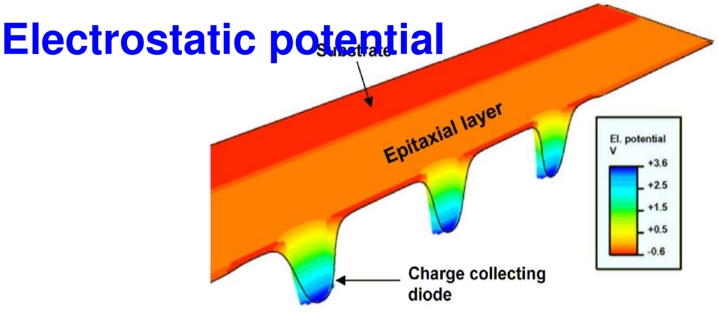
through the center of N well

through the center of P well



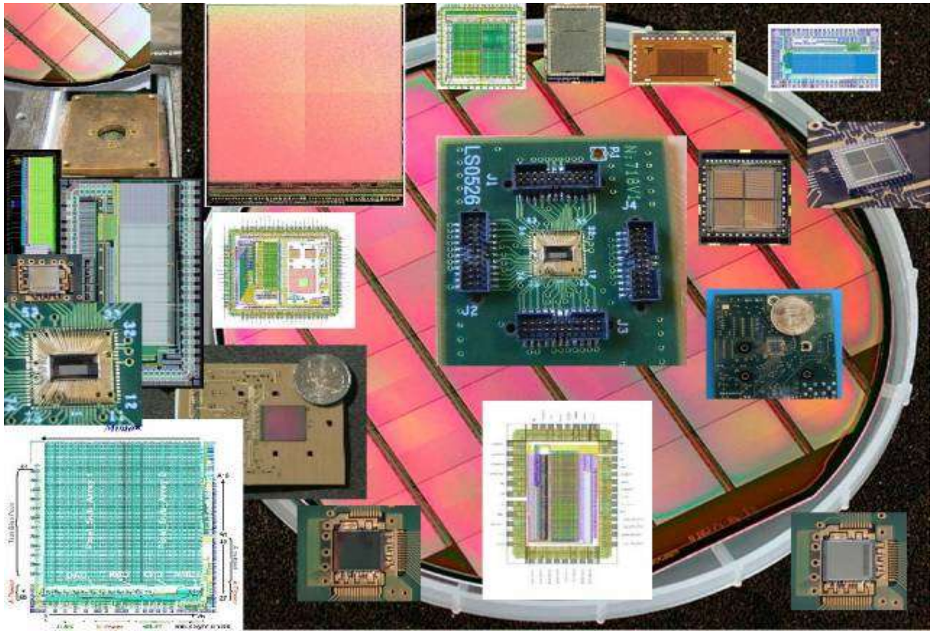
- 2001: proposal of new structure adapted for particle tracking (Turchetta et al., NIM A 458 (2001) 677)
- Double-well CMOS process with epitaxial layer; the generated charge is reflected by the potential barriers due to doping differences and collected by thermal diffusion by the n-well/p-epi diode; collection times ~100 nsec
- Use of CMOS technology: large scale availability at low cost, high granularity, improved readout speed and radiation hardness; the operational voltage is set by the CMOS process → no HV
- Possibility of thinning down the substrate: low material budget

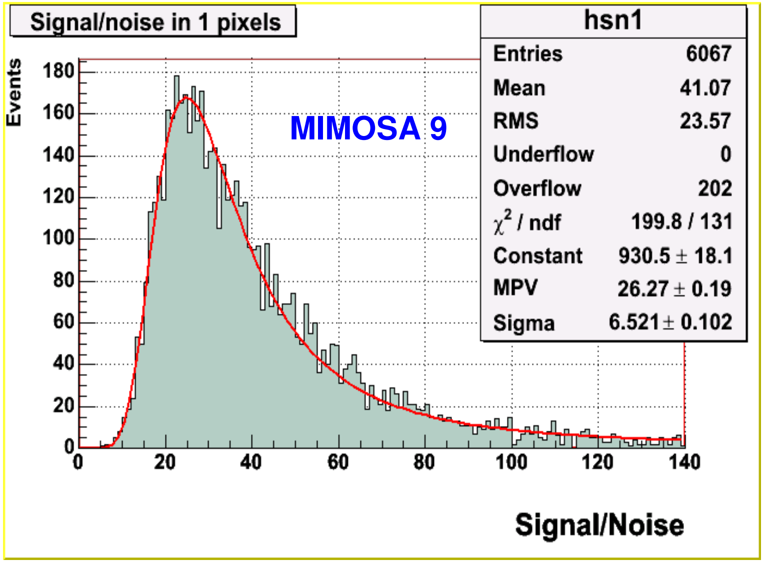


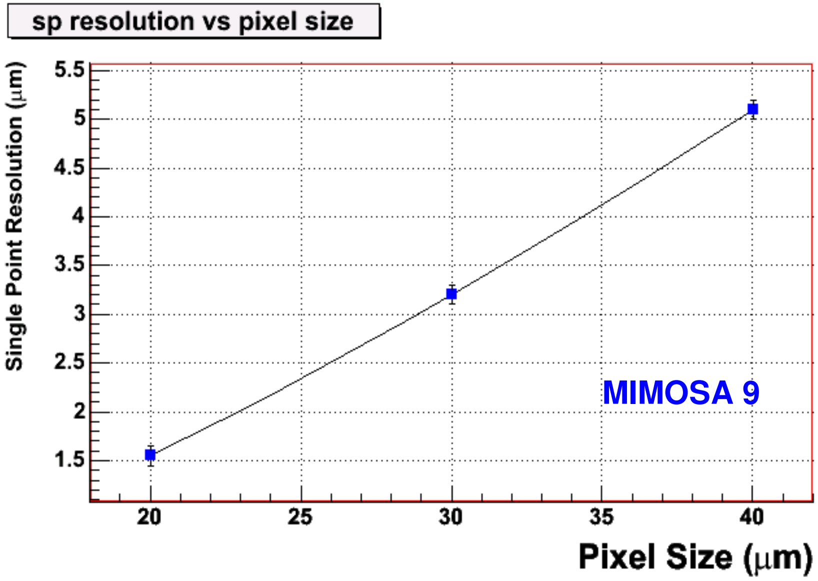


MAPS detection performances

- MIMOSA series from IPHC Strasbourg: several fabrication processes and architectures explored, best performances on AMS 0.35 µm OPTO, 14 µm epilayer
- Tracking performances (100 GeV/c π @ CERN and 6 GeV e^- @ DESY):
  - S/N~20-30
  - noise~10-20 e^-
  - detection efficiency>99%
  - single point resolution: 1.5-2.5 µm
- Performances reproduced with large size prototype (~2×2 cm^2)

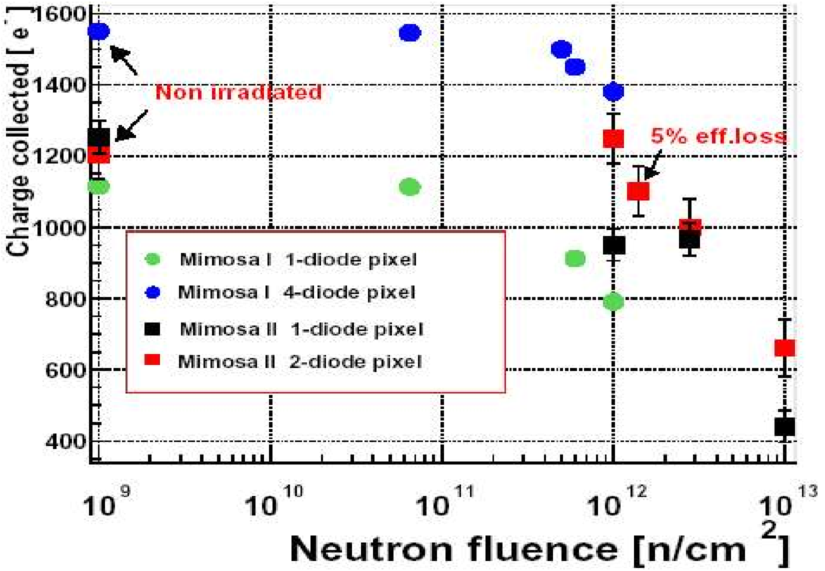


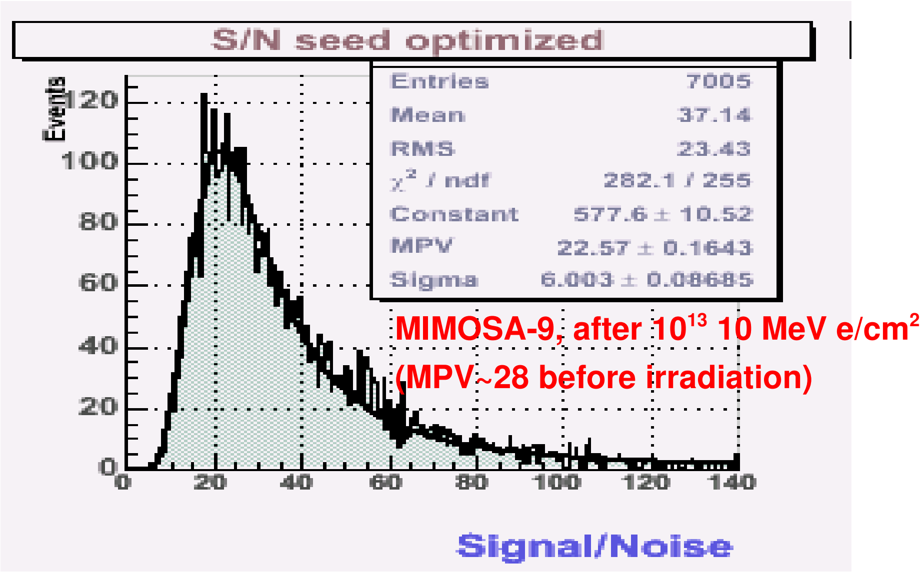




[IPHC, Strasbourg]

Radiation hardness

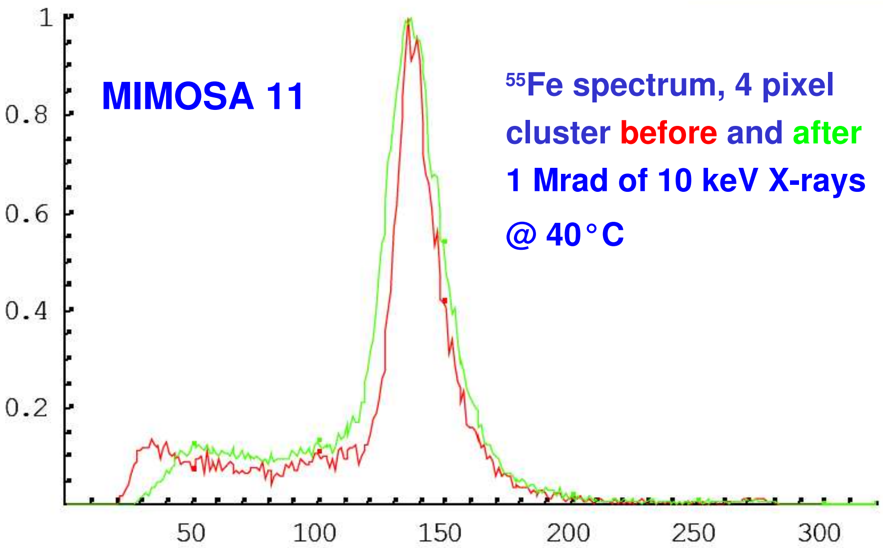




MIMOSA-9, after 10^{13} 10 MeV e/cm^2

(MPV~28 before irradiation)

- Neutron irradiation: charge losses and decrease of efficiency observed after ~10^{12} n_{eq}/cm^2
- Electron irradiation: performance of irradiated prototype recovered with cooling to T<-10ºC
- Improved tolerance to ionizing radiation up to 1 Mrad thanks to improved pixel layout (thin oxide, guard-ring)
- **ILC requirements for radiation hardness are met**

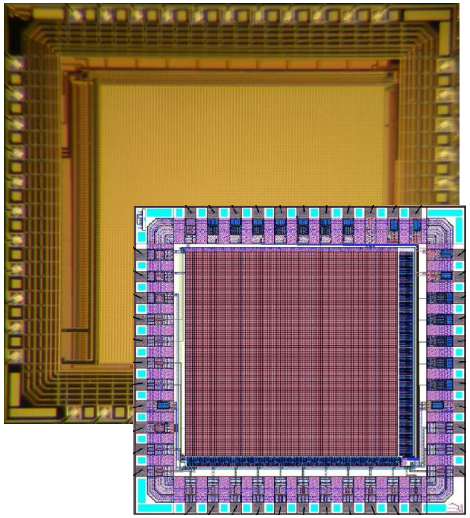


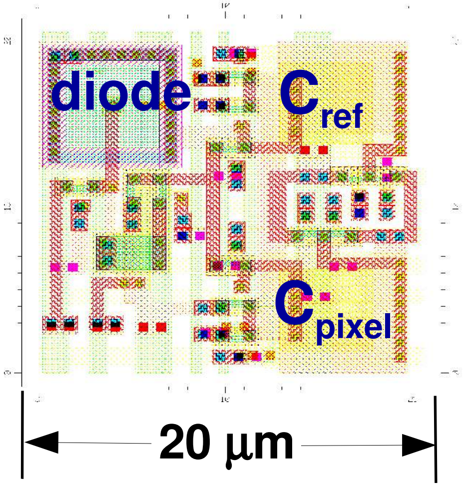
MIMOSA 11

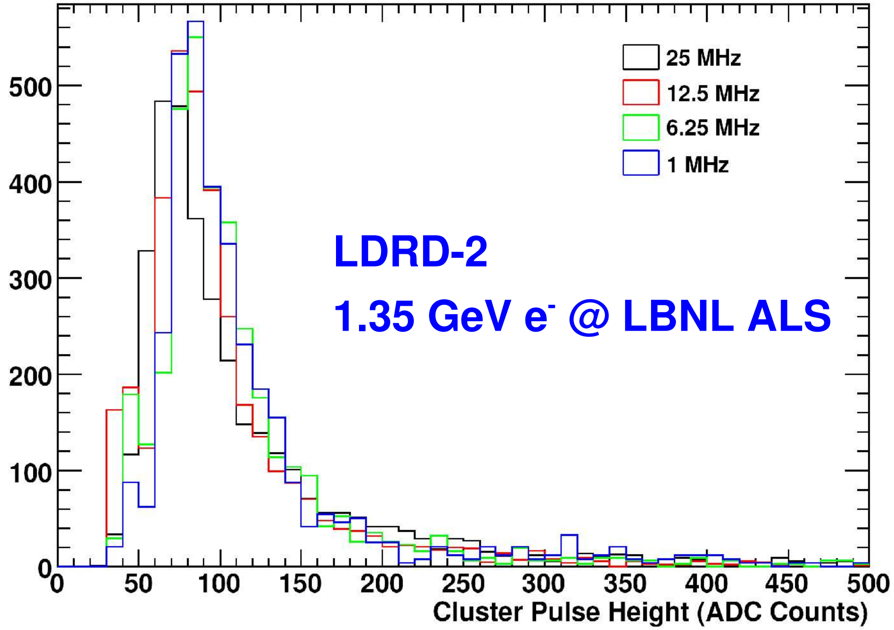
^{55}Fe spectrum, 4 pixel cluster before and after 1 Mrad of 10 keV X-rays @ 40 °C

[IPHC, Strasbourg]

Integrated functionalities: in-pixel CDS





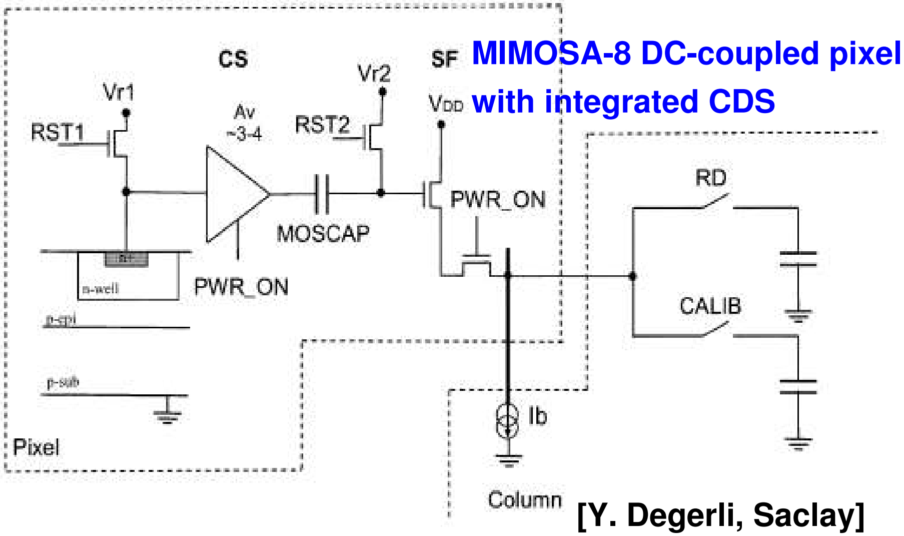


LDRD-2

1.35 GeV e^- @ LBNL ALS

- LDRD-2 @ LBNL: AMS 0.35 µm process, 20×20 µm² pitch with in-pixel CDS: signal and pedestal level stored on pixel capacitors, successfully tested up to 25MHz

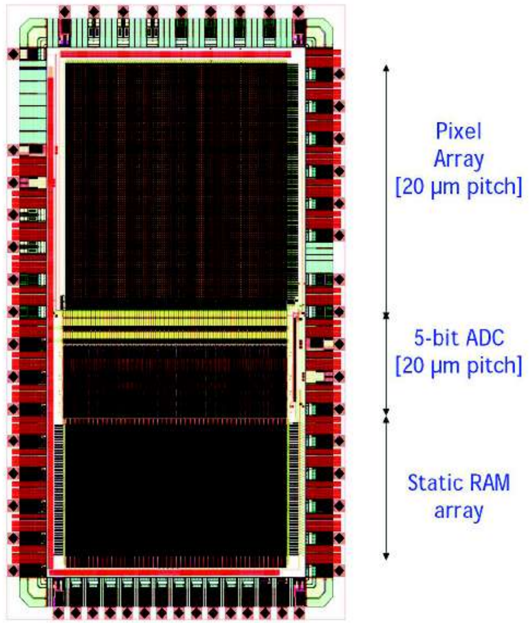
- Several MIMOSA prototypes: in-pixel double sampling circuitry; reset and signal levels stored in capacitors at the end of the column (see talk P. Lutz for details)

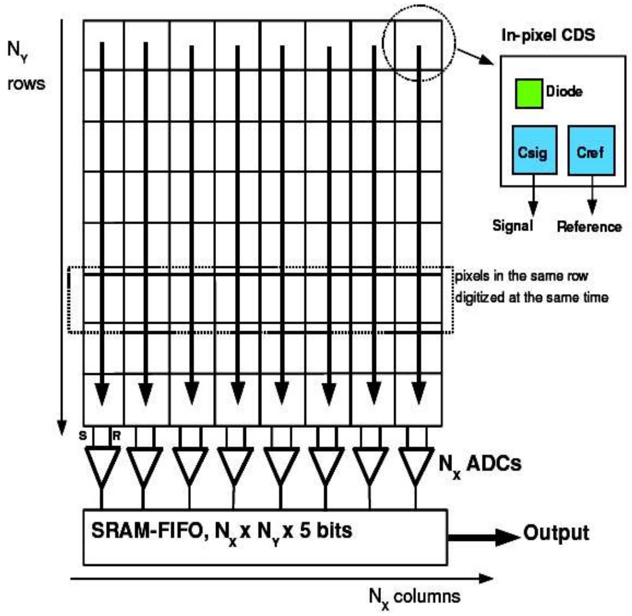


MIMOSA-8 DC-coupled pixel with integrated CDS

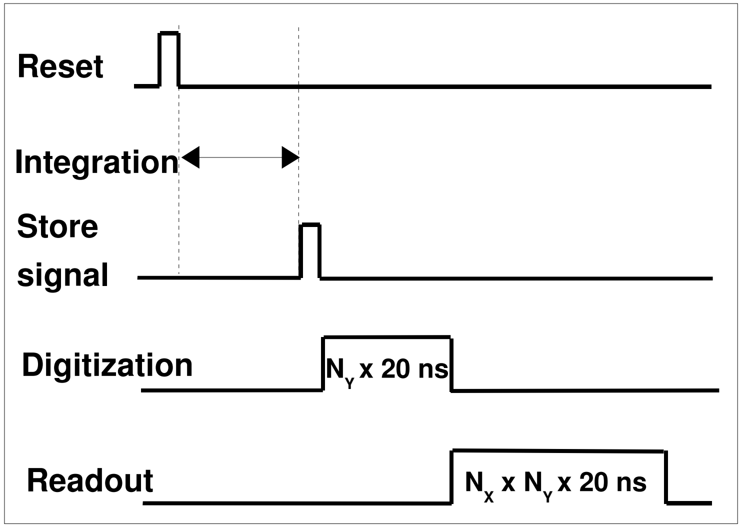
[Y. Degerli, Saclay]

Integrated functionalities: digitization





Sample readout scheme @ 50 MHz



- LDRD-3 @ LBNL: AMS 0.35 µm OPTO process, 96×96 pixels, 20 µm pitch. Available October 2007.
- In-pixel CDS from LDRD-2, readout at 50 MHz
- At the end of each column:
    - 5-bit successive approximation, fully-differential ADCs @ 300 MHz
    - SRAM memory cell

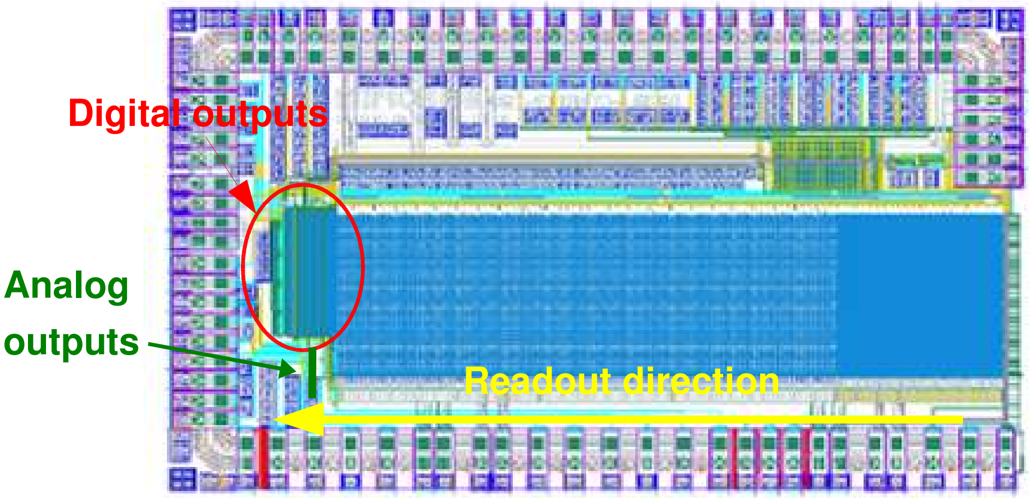
- Several ADC architectures being explored by IN2P3-DAPNIA collaboration: flash, SAR, Wilkinson.

Test of test structures under way, fabrication of sensor prototypes foreseen in 2008

Readout architecture: fast CP readout

- Fast column-parallel readout needed in order to read the sensor multiple times during the 1 ms bunch train; actual readout frequency depends on length of columns, i.e. integration time
- Analog readout or binary readout?
  - Analog option requires integrated ADCs: increase dead area at the edge of the ladder and power dissipation, but good position resolution can be obtained with ~20 μm pixel
  - Binary readout needs higher granularity to preserve position resolution (thus increasing number of pixels and data volume), but simplifies data processing and sparsification

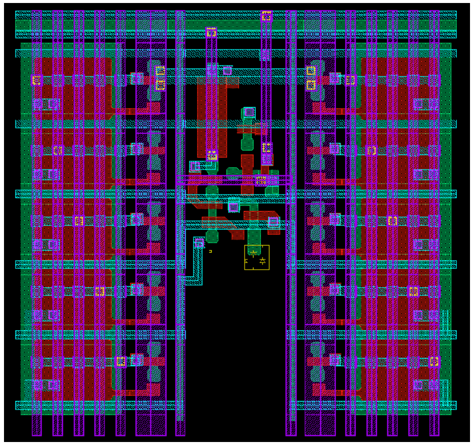
- MIMOSA-8 prototype: TSMC 0.25 μm, 8 μm epilayer, 25 μm pitch, int. time<50 μs, analog & digital output with discriminator at the end of column



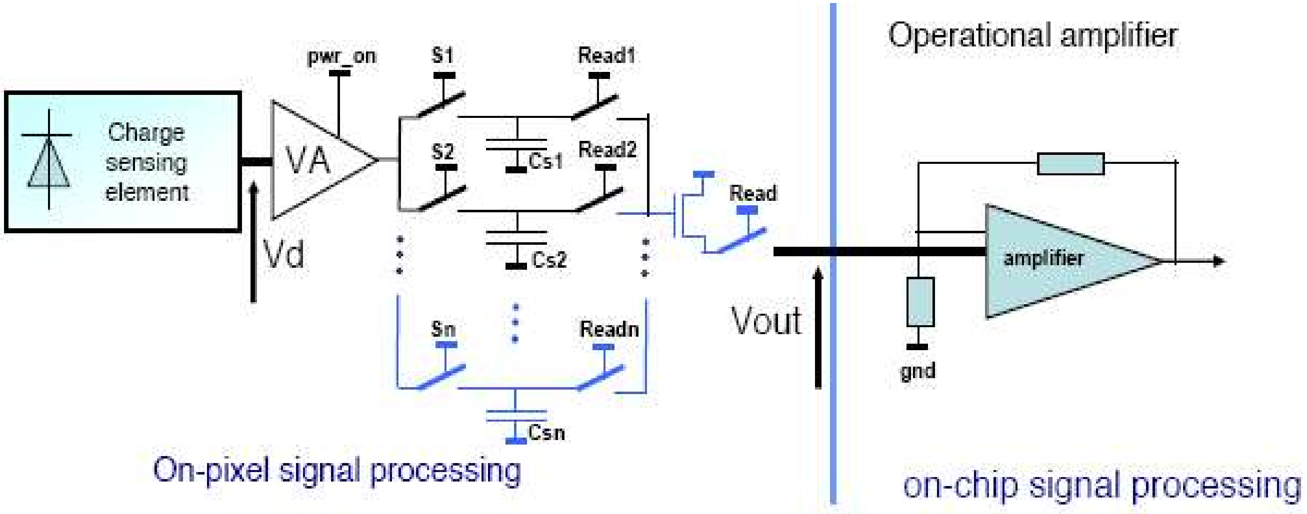
[IPHC, Strasbourg]

- Good noise performance (ENC~15 e^-), low pixel-to-pixel dispersion
- Test-beam(digital part): efficiency~99%, fake hit rate<10^{-3}/pixel/event for low discriminator S/N cut
- Architecture recently replicated in AMS 0.35 μm OPTO process (MIMOSA-16)

Readout architecture: local storage of signals

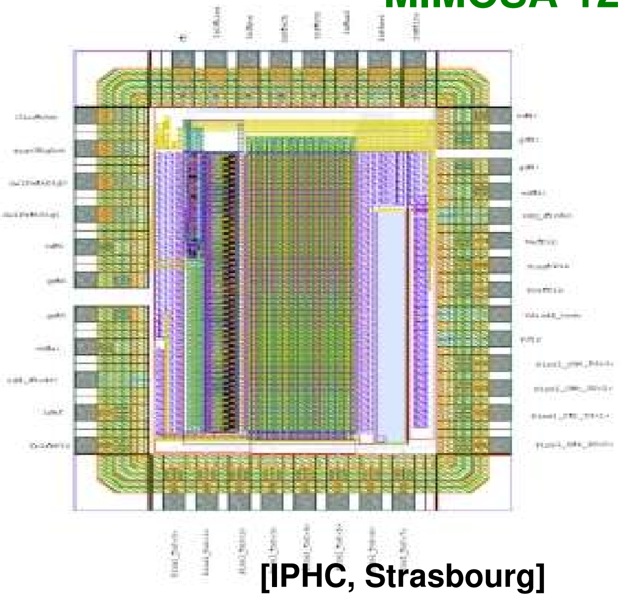


[RAL/Liverpool, UK]



- Multi-memory pixel architecture with delayed read-out (FAPS) first introduced by UK groups (RAL/Liverpool)
- MIMOSA-12 prototype in AMS 0.35 µm, 35 µm pitch: implements 4 capacitors/pixel (50, 100, 200 fF), various types (MOS caps are smaller but less precise, poly are more precise but larger)
- Aim for minimal size capacitors providing statisfactory precision
- Look for trade-off between pixel pitch and number of capacitors

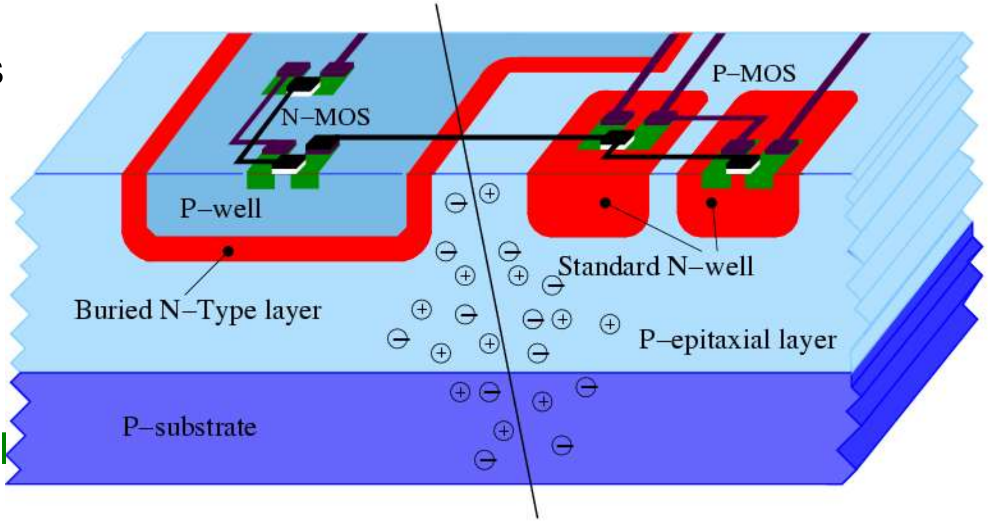
MIMOSA-12

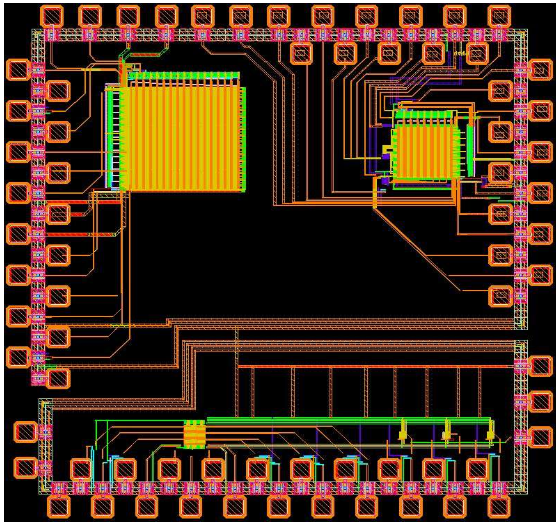


[IPHC, Strasbourg]

MAPS in triple well technology

- Triple-well process: deep n-well used to shield the standard p-well; p-well hosts nMOS transistors as in standard MAPS, standard n-well may host pMOS transistors
- Deep n-well can be used to collect the charge generated in the epitaxial layer; possible inefficiency due to presence of standard n-well
- Possibility for increased complexity of the in-pixel circuitry: sparsification, time stamping



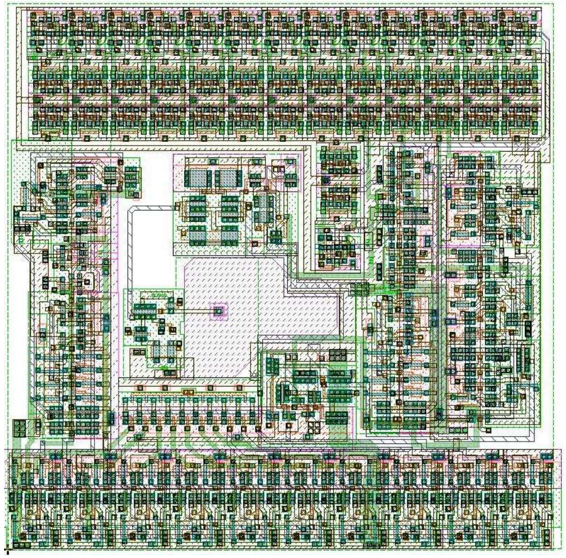


- Series of APSEL chips fabricated by INFN SLIM collaboration, proof of principle.
- New prototype in STM 0.13 μm triple well CMOS tech. with in-pixel discriminator and digital section with 5-bit time stamp and data sparsification logic, 164 transistors in 25x25 μm^2 pixel
- Technology might allow time stamping during bunch train and inter-bunch readout, tailored to structure of ILC beam, EMI insensitive

[see G. Traversi's talk]

MAPS with time stamping

- Single bunch crossing tagging: bunch-by-bunch time tag for each pixel to keep low occupancy
- Readout strategy as envisioned in triple well: buffer data during the 3000 bunches in a train and readout data during the bunch trains
- In-pixel comparator + deep memory with bunch clock bus

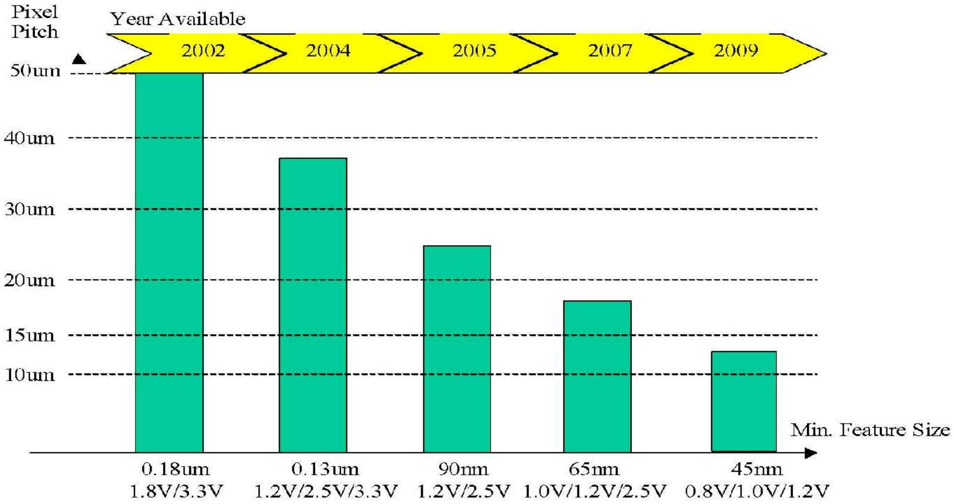


[J. Brau, Oregon]

563 Transistors (2 buffers +calibration)

50 μm x 50 μm

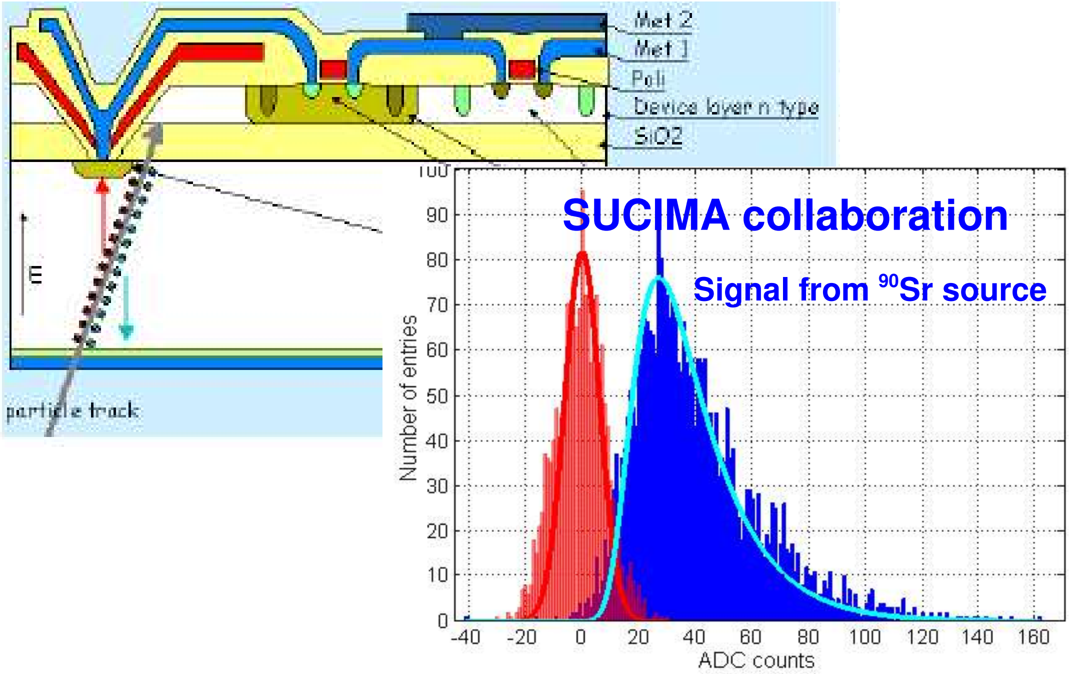
Technology Roadmap: Macropixel size estimation vs. Mixed-signal Process Technologies

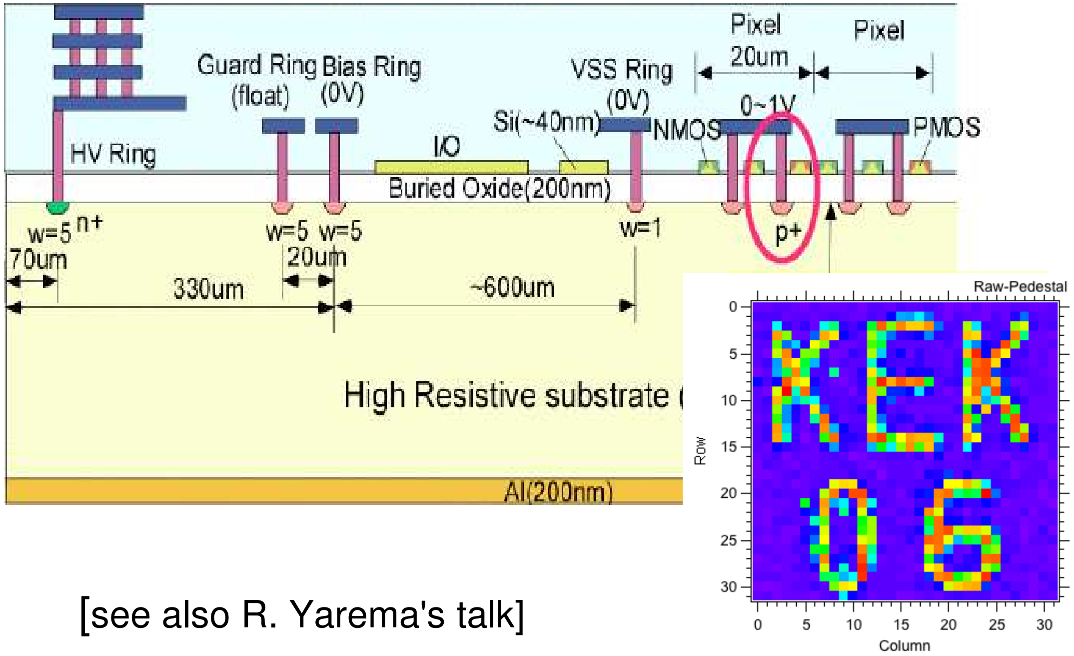


- Chronopixel: completed design of first prototype, to be fabricated in 0.18 μm TSMC technology.
- 50x50 μm pixel to house >500 transistors; need to scale down (45 nm) to fit in 20 μm pixel
- Need triple well tech. in ultimate design to increase pixel sensitive area

SOI monolithic pixels

- Silicon-On-Insulator technology
- Electronics layer isolated from high-resistivity substrate by buried oxide; depletion of substrate and readout integrated on sensor top
- Proof of principle from SUCIMA collaboration, prototype in 3 µm process (IET, Poland), though not compatible with standard CMOS



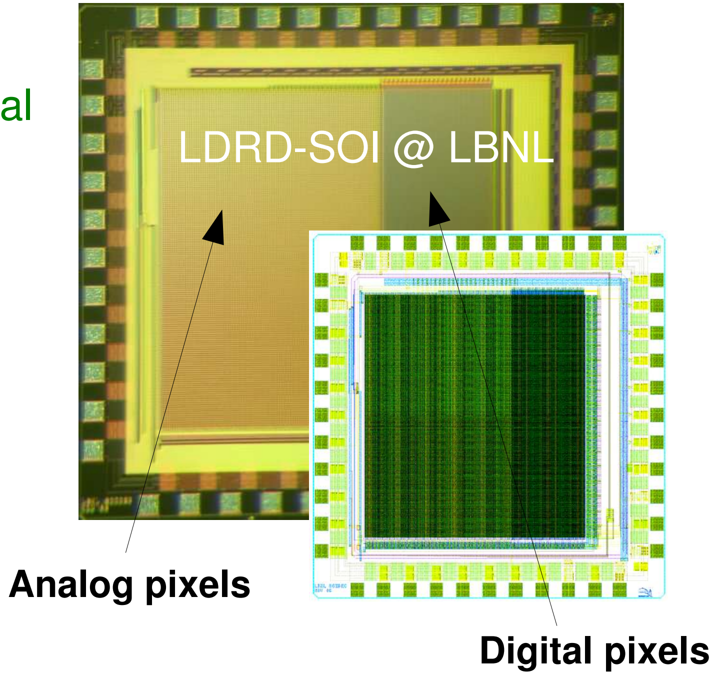


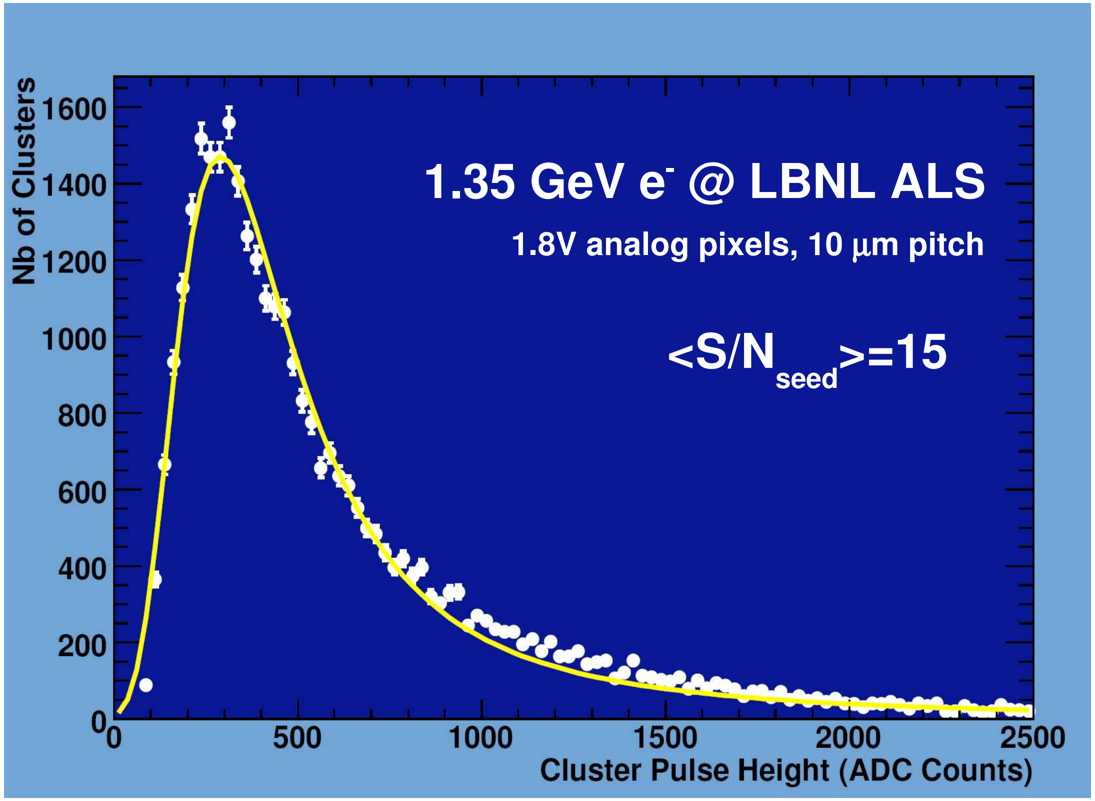
- Novel 0.15 µm fully-depleted SOI process from OKI; combines high-res substrate with full CMOS circuitry on top layer; high-speed, low power dissipation digital design possible, latch-up immunity
- 350 µm substrate, 200 nm buried oxide, 40 nm CMOS layer, fully depleted at operational voltages
- Functionality demonstrated by KEK chip in '06

[see also R. Yarema's talk]

First beam on FD-SOI pixel prototype

- LDRD-SOI chip @ LBNL: 160x150 pixels, 10x10 μm^2 pixels
- 2 analog parts (1.0V and 1.8V) with simple 3T architecture, 1 digital part; 1x1 μm^2 and 5x5 μm^2 diodes
- Part of Dec. '06 pilot run through KEK, including chip submissions from KEK, LBNL, FNAL, Uni. Hawaii





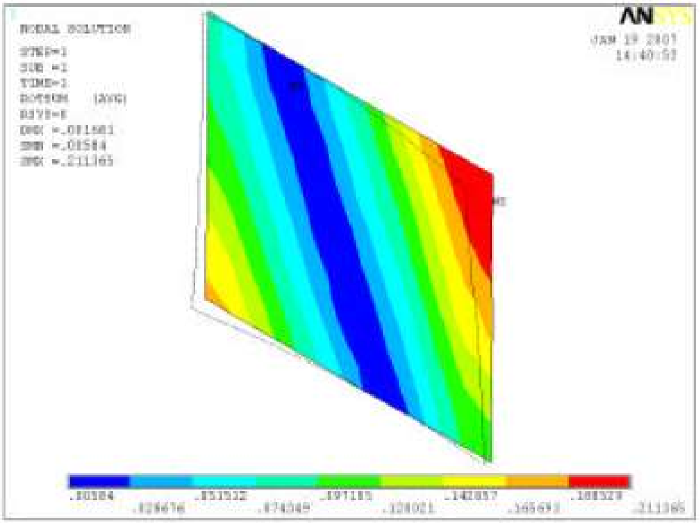
- Beam-test with 1.35 GeV e^- @ LBNL ALS
- Significant back-gating effect, but chip can be depleted @ 10-15V with good particle detection performances
- Laser studies under way to calibrate signal vs. depletion voltage
- Estimation of radiation hardness under way

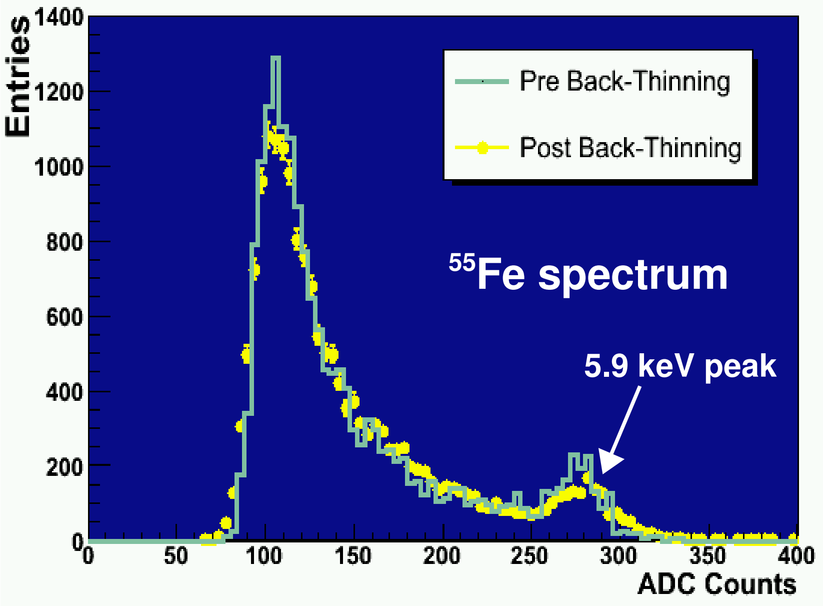
Back-thinning

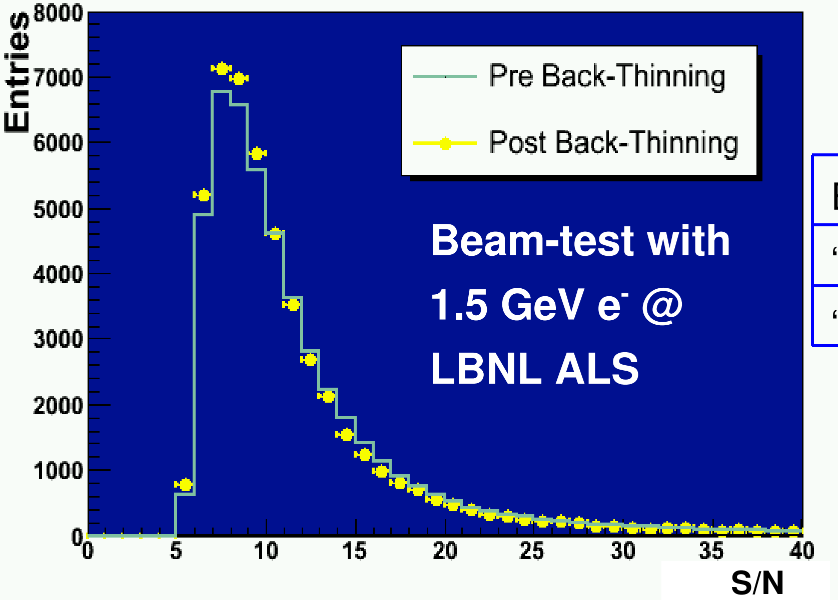
- Back-thinning of diced chips using grinding process by Aptek Industries (San Jose, CA)
- LBNL: thinned over 15 MIMOSA-5 chips: 1 M pixels, 17 µm pitch, 17x19 mm² surface, AMS 0.6 µm process
- Achieved 40 µm thickness, yield of functional chips~90%
- Extensive characterization pre- and post-back-thinning to study possible effects on detection performance

→ **feasibility of back-thinning CMOS sensors demonstrated**

Measured surface map of 50 µm thin chip



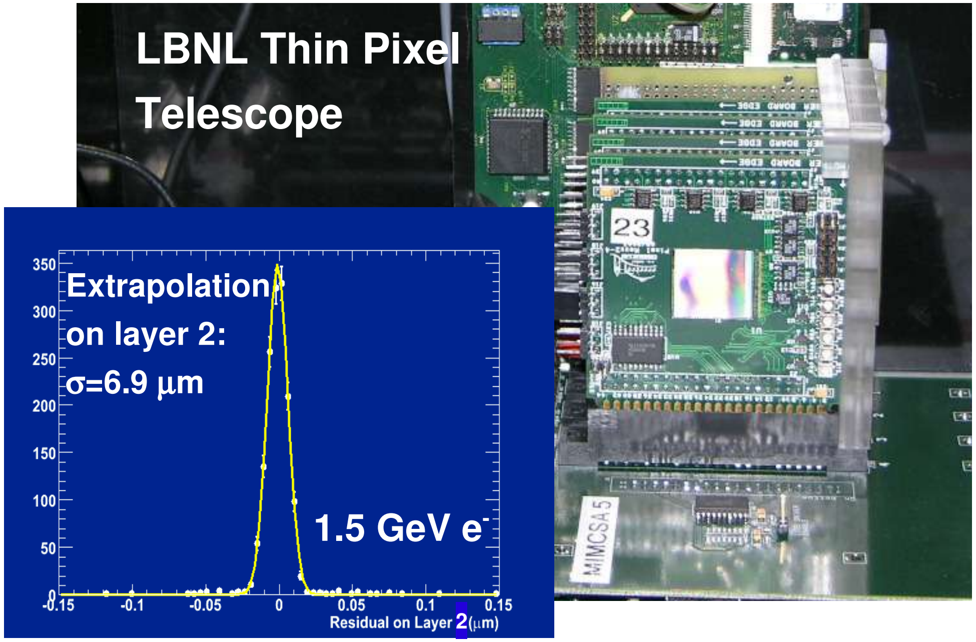




Measured average sensor thickness

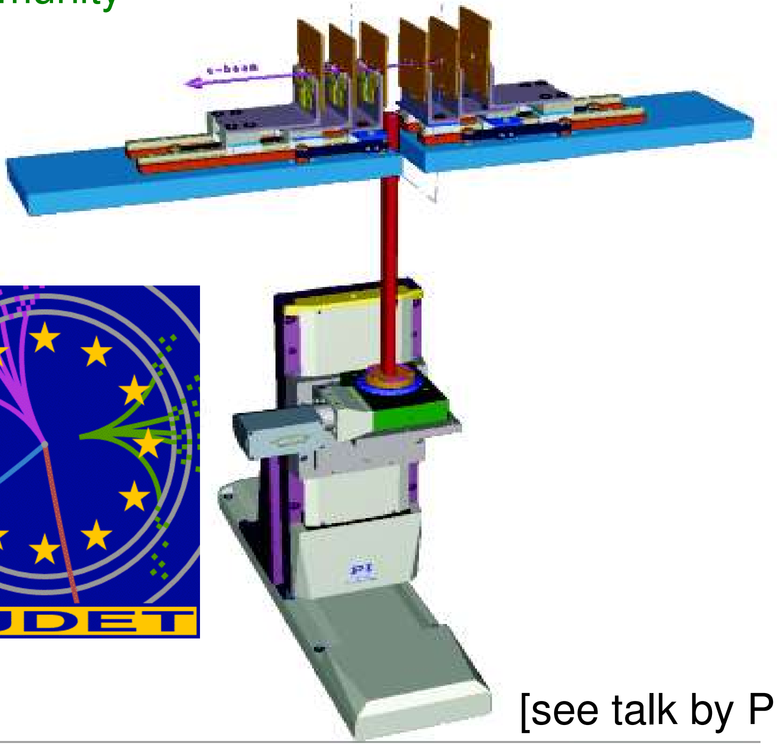
Before	(550±0.5) µm
“50 µm”	(50±7) µm
“40 µm”	(41±6) µm

CMOS pixel telescopes as a tracker test-bench



- LBNL: 4 layers of 50 μm thin MIMOSA-5 chips, precisely spaced by 1.5 cm (ILC VTX like geom.); 512x512 pixels (17 μm) on each plane, parallel readout with on-line sparsification by DAS
- Good extrapolation resolution in low momentum environment thanks to low material budget
- Telescope extensively tested at LBNL-ALS with 1.5 GeV e^- and deployed in tracking tests with 120 GeV p at FNAL MTBF

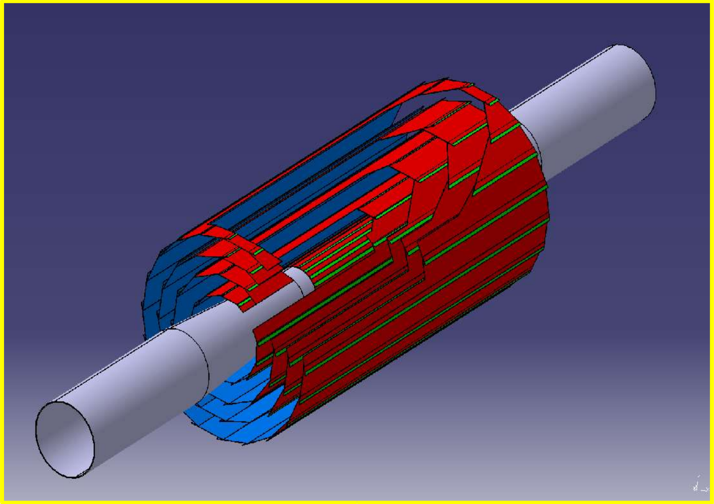
- EUDET JRA-1 effort on 6 plane CMOS telescope
- First demonstrator built based on MIMOSA chips
- Final telescope with reticle-size chip, binary pixels
- Plan to reach ~1 μm resolution with DESY 1-6 GeV e^- beam with aid of high-resolution plane close to DUT
- Equip DESY/CERN testbeam facilities, available to the community

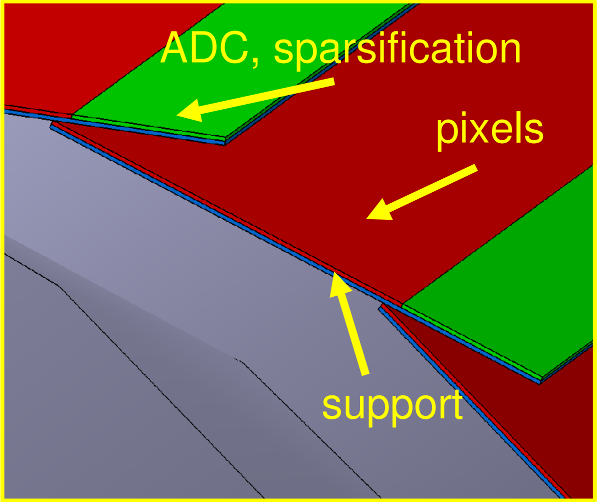


EUDET

[see talk by P. Lutz]

Vertex design and integration

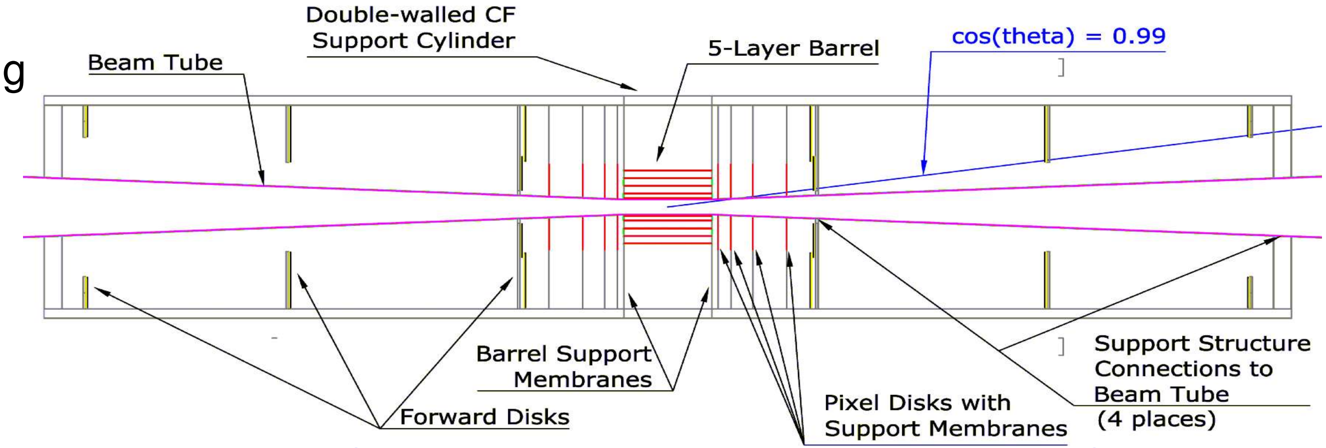




- Proposed VXD concept based on CMOS monolithic pixels
- 5 cylindrical layers, R=15-60 mm, different pitch/layer, ~300 million pixels
- Design implemented in LDC concept simulation framework

- Inner VXD layers: need for fast CP readout and integrated signal processing (CDS, ADC, sparsification)
- Outer VXD layers: lower rate but larger data flux, implement larger pixels with local storage of charge signals, readout during beam-off periods

- Different detector concepts studying various options for VXD geometry, barrel only vs barrel plus forward disks
- On-going work on simulation of ladder geometry and mechanical support

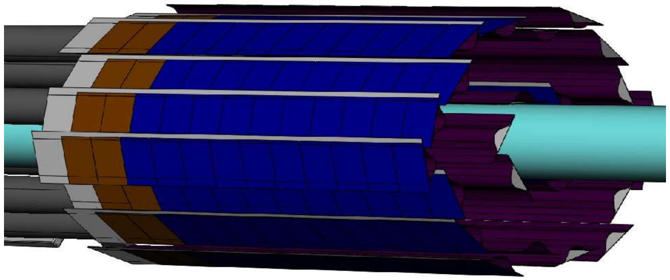


Aerial view of the SiD vertex detector mechanical support [Bill Cooper, FNAL]

Learning from the STAR experience

- New high-resolution vertex detector inside existing one
- 2 layers at 1.5 cm and 4.5 cm radii, equipped with CMOS pixels

STAR Heavy Flavor Tracker

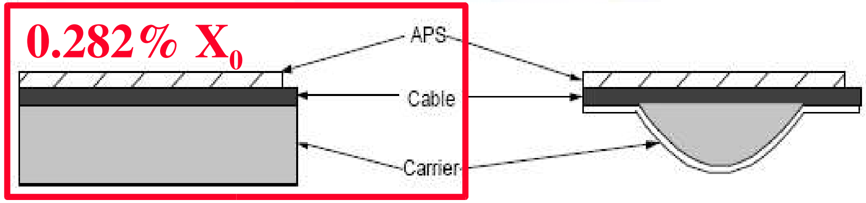


	STAR	ILC
Performance drivers	Low p_T D	b/c/τ tagging
Position resolution	~10 µm	2-4 µm
Radiation length	0.3% X_0/layer	0.1% X_0/layer
Number of layers	2	5-6
Ladders/layer	6+18	?
Operational T	40ºC	-10ºC ... 20ºC
Cooling	Air flow	?
VTX mount	Side mount	Two sides

- 24 ladders, ~100 Mpixels, 30×30 µm^2, ~0.3% X_0/layer, operation at 40ºC, air cooling

- Developed low-mass ladder prototype with thin CMOS sensors achieving <0.3% X_0/layer

[see L. Greiner's talk]



Carrier: 50µm CFC+3.2mm RVC+50µm CFC (=0.11%X_0)

Ladder prototype material budget

Component	% radiation length
MIMOSA detector	**0.0534**
Adhesive	**0.0143**
Cable assembly	**0.090**
Adhesive	**0.0143**
CF / RVC carrier	**0.11**
Total	**0.282**

Conclusions

- Monolithic Active Pixel Sensors as a candidate technology for the ILC Vertex Tracker have shown excellent detection performances through several prototypes exploring different technologies and architectures:
  - ➢ Fast readout achievable with CP architecture/on-chip data reduction
  - ➢ Radiation hardness satisfactory
  - ➢ Thinning to 50 µm established
  - ➢ Implementation of integrated ADC's and data sparsification under way in forthcoming prototypes

- Bulk CMOS process optimized for imaging architecture is adequate for analog architectures with integrated functionalities (e.g. in-pixel CDS and on-chip digitization)

- Emerging technologies such as triple-well CMOS and SOI might be the optimum choice for digital architectures with in-pixel time stamping

- Application in various pixel telescopes and STAR VXD upgrade as test benches in real applications

- Integration issues to be kept in mind in parallel with sensor development (see R. Yarema's talk for 3D sensor integration and Ron Lipton's talk for ILC vertex system integration issues)