

San Diego, April 3rd – 5th, 2012

#### List of sessions:

- Design and Process Hardening
- Single Event Test Facilities
- SEE on Commercial Memories
- Single-Event Transients
- Single-Event Test Methods
- Destructive SEE
- Product, Technology, System SEE

- Lot of space and army oriented topics
- Memory test (NAND flash), Point of load DC/DC converters, ADC converters, FPGAs...
- SET
- Mitigation techniques like "scrubing" (removing errors from a memory's content by re-writing it periodically with correct values)
- SEL protection by an adjustable over current detection that forces a power cycling of the full system in case of SEL detection
- Device hardening by placement of redundant blocks suficciently far apart to not be influenced by the same incident partcle

# Quantity of laser aided diagnostics





Single Event Functional Interrupt

Location and Elimination

via Pulsed Laser Scanning

on a RadHard CMOS 16-bit ADC

Alfio Zanchi, Shinichi Hisano, Craig Hafer, and David B. Kerwin

Aeroflex Colorado Springs, Inc. - Colorado Springs, CO

SEE Symposium – San Diego, CA (U.S.A.) – April 3<sup>rd</sup>, 2012

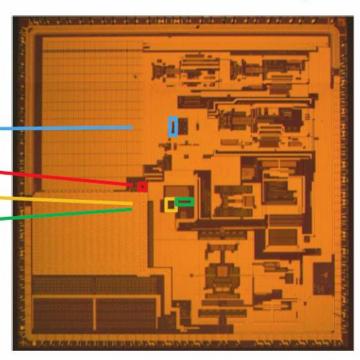
#### SET effects due to E-H in various blocks

#### **Pulsed laser scanning**



- ▼ Factors of uncertainty of the test
  - no direct pulse energy sense (photodiode) available in Aeroflex
  - is metallization completely open over sensitive block: no de-rating?

- ▼ Areas subject to laser pulses
  - Bandgap
  - POR
  - VREF generator
  - Voltage drivers



# Studies of SET with short X-ray pulses



# Single Event Transients Induced by the Absorption of Picosecond X-ray Pulses

David Cardoza, Stephen D. LaLumondiere, Michael A. Tockstein Steven C. Witczak, Yongkun Sin, William T. Lotshaw and Steven C. Moss

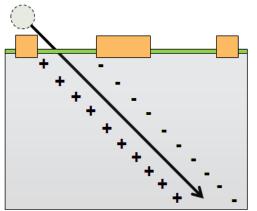
The Electronics and Photonics Laboratory
The Aerospace Corporation

4 April 2012

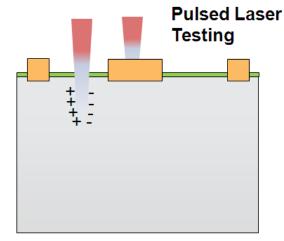
# SEU location by Laser or X-ray

#### **Motivation for Short X-ray Pulses**

#### Traditional Accelerator Facility



- Large Penetration Depth
  - Generates Charge Tracks
- Penetrates Metallization
- Unless microbeam facility or mask used, difficult to spatially locate upset location.



- Focusable relatively high spatial resolution.
- Charge carriers generated in skindepth volume around focus
- Unable to penetrate metallization
- Two photon techniques can be used to evade metallization via backside illumination.



#### XILINX FPGA Devices SEE evaluation



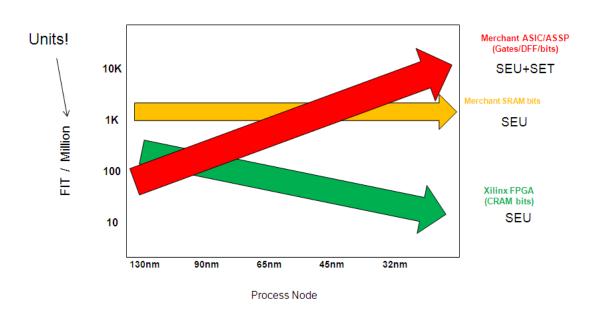
From 250nm to 28nm Terrestrial SER Xilinx FPGA Devices

**Austin Lesea** 

#### XILINX FPGA Devices SEE evaluation

Advances in protection of the configuration memory

#### Xilinx View: our per bit FIT gets better





#### Destructive test of IGBTs





# Trench Fieldstop Insulated Gate Bipolar Transistor (IGBT) failures at ground level

Antoine Touboul, Lionel Foro, Frédéric Wrobel, Frédéric Saigné

#### Destructive test of IGBTs



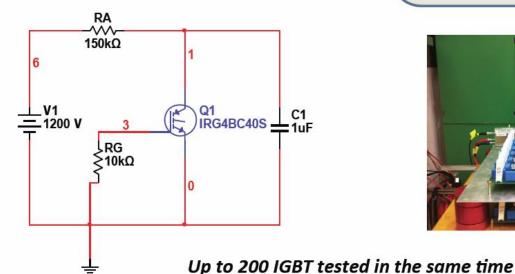
# 1200V-IGBT failures under ANITA atmospheric like spectrum, TSL

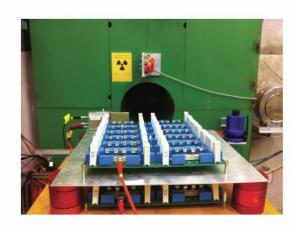
Sensitive state for SEE triggering is OFF state

 $V_{CE}$  from 70% to 100% of  $V_{CEMAX}$ ,  $V_{GF}$ =0V

Contrary to test of digital devices, the failure does not affect a bit but the whole device itself.

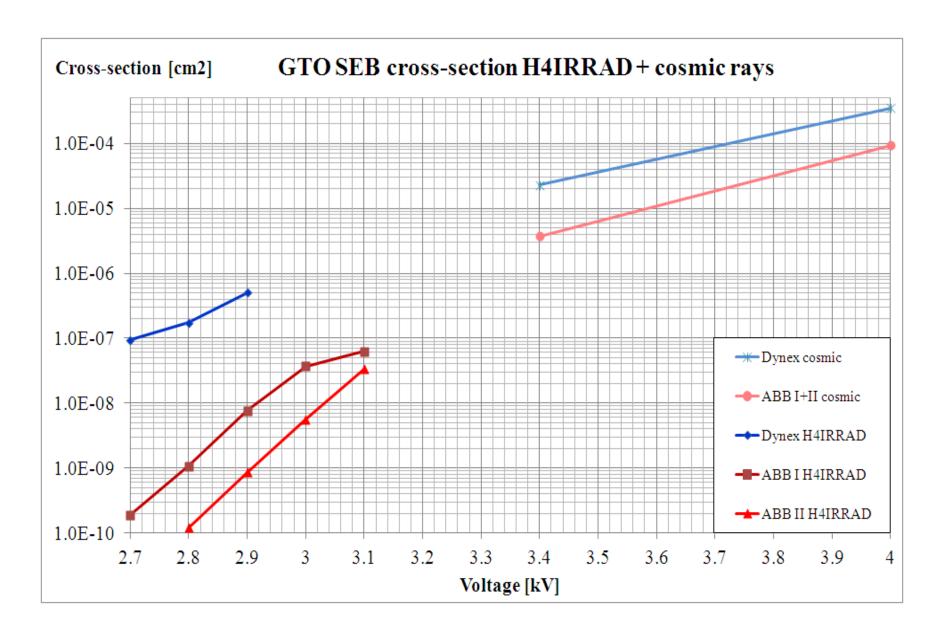
> 1 failure=1 device lost Hard to get good statistics





# Non-destructive SEB tests of HV GTO-like thyristors





### Measurement output example

- Influence of experienced SEBs to c-s measurement Dynex at 2.7 kV:
  - c-s = 1,22.10<sup>-7</sup> cm<sup>2</sup> after first 49 SEBs
  - c-s = 1,24.10<sup>-7</sup> cm<sup>2</sup> after 99 SEBs
  - c-s = 0,92.10<sup>-7</sup> cm<sup>2</sup> after 162 SEBs

