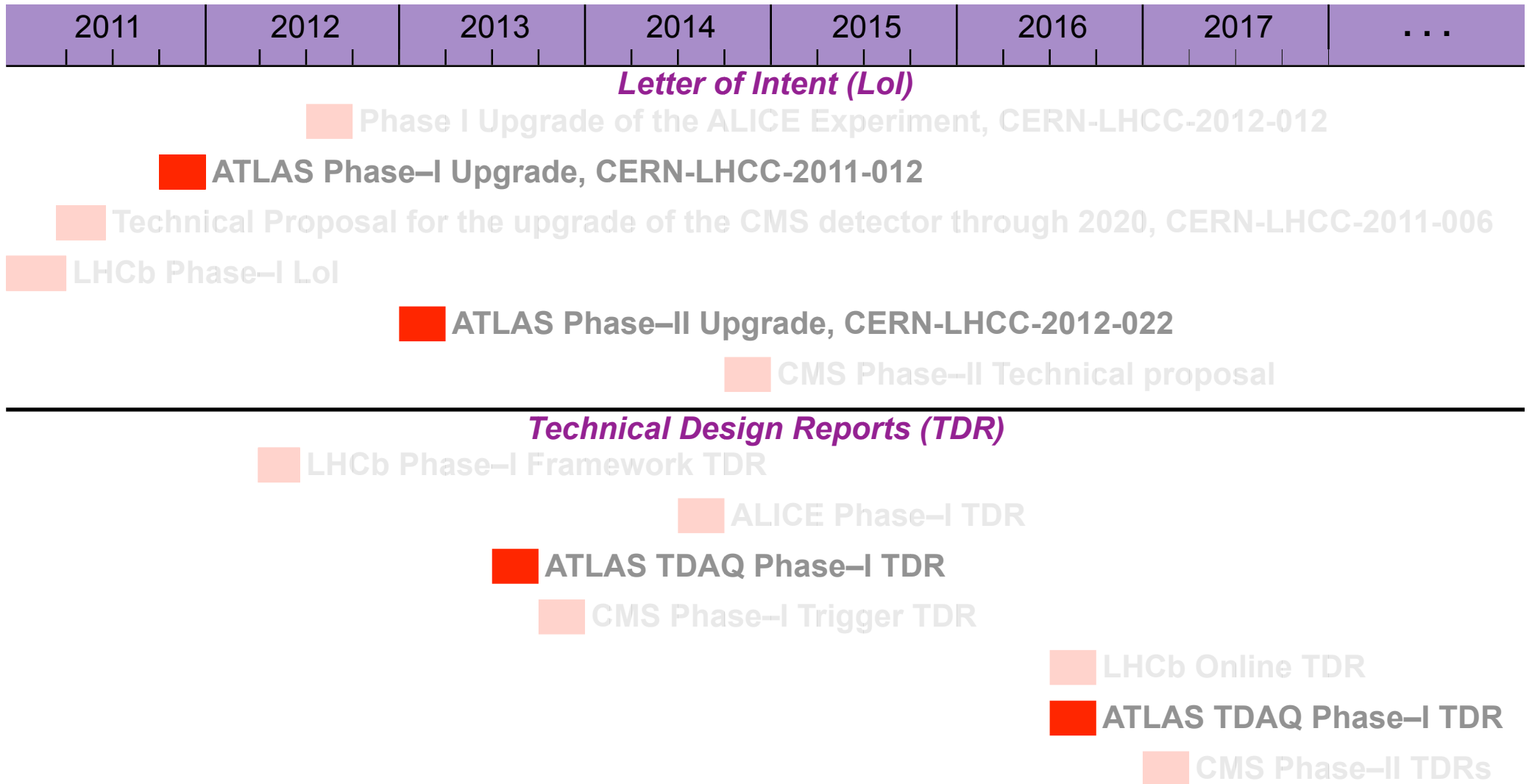


DAQ @ LHC: ATLAS Upgrade overview

- What has been written in these Documents?
 - Well at least for what has a direct impact on DAQ



DAQ @ LHC: ATLAS Upgrade overview

Machine evolution

...	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	...	2030
	Phase 0 Run 1		LS1		Run 2		LS2		Phase I Run 3		LS3		Phase II Run 4			
	(Prepare Run 2) Consolidation				(Prepare Phase I) Ultimate luminosity $\sqrt{s} = 13\sim 14$ TeV 25 ns bunch spacing				(Prepare Phase II) HL-LHC							
	$L_{inst} \sim 1 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ $\mu \sim 27$ $\int L_{inst} \sim 50 \text{ fb}^{-1}$				$L_{inst} \sim 2\text{--}3 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ $\mu \sim 55\text{--}81$ $\int L_{inst} > 350 \text{ fb}^{-1}$				$L_{inst} \sim 5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ $\mu \sim 140$ [with levelling] $L_{inst} \sim 6\text{--}7 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ $\mu \sim 192$ [without levelling] $\int L_{inst} \sim 3000 \text{ fb}^{-1}$							

DAQ @ LHC: ATLAS Upgrade overview

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DAQ @ LHC: ATLAS Upgrade overview

□ ATLAS evolution at a glance

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	Other				Other				Other							

DAQ @ LHC: ATLAS Upgrade overview

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	Other				Other				Other							

DAQ @ LHC: ATLAS Upgrade overview

- Prepare for Run 2–3
 - Peak luminosity of $2\text{--}3 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$
 - μ up to 80

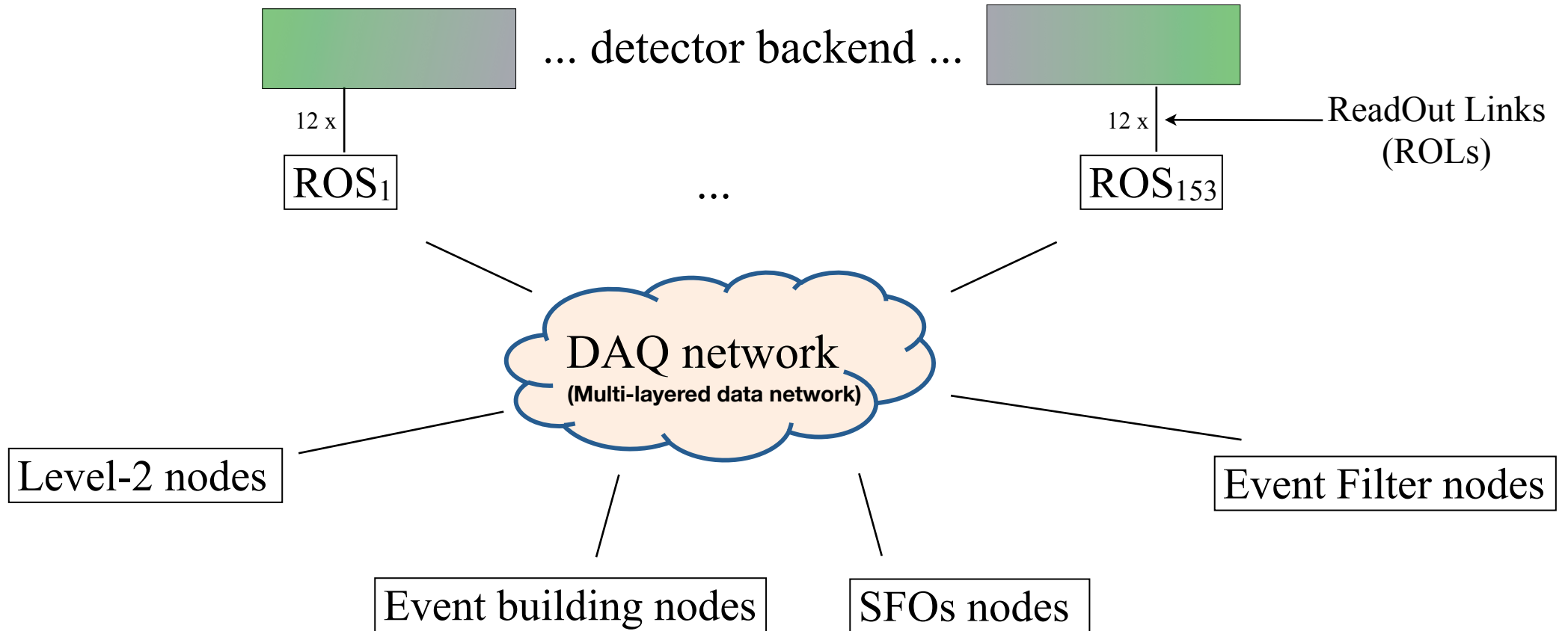
μ	Fraction of total							Total/MB
	Pixel	SCT	TRT	LAr	Tile	Muon	TDAQ	
30	6%	6%	13%	58%	7%	5%	3%	~1.2
80	10%	10%	17%	49%	6%	4%	4%	~2.4
	LS3 New Inner detector							
200	~3 Mbyte							5

- Level-1 rate 100 kHz
 - TDAQ TDR design values
- Targeting average physics rate to storage of 1 kHz

No change to data flow architecture

DAQ @ LHC: ATLAS Upgrade overview

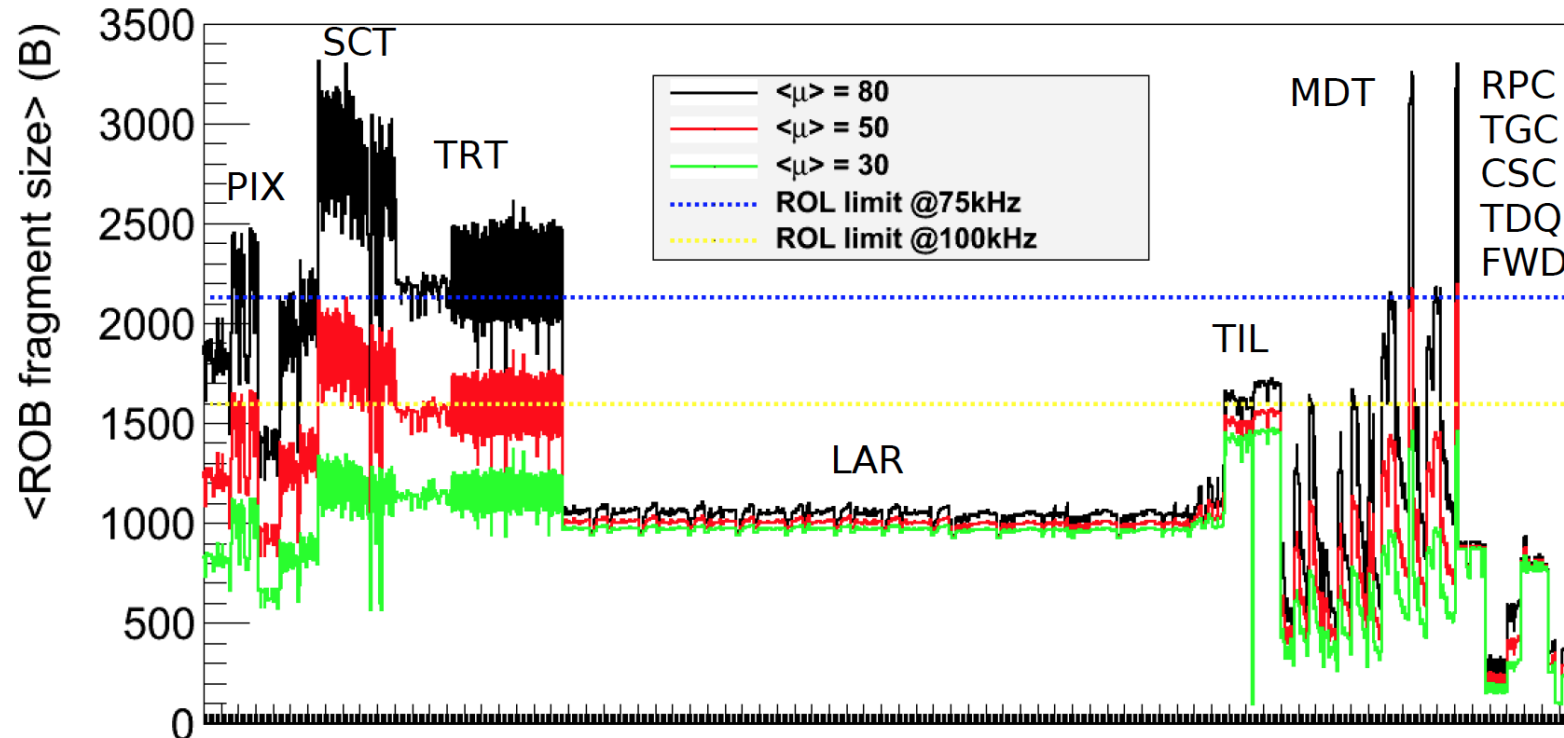
□ ATLAS TDAQ ... to first order



DAQ @ LHC: ATLAS Upgrade overview

□ ROS input bandwidth

- TDR (2003): 100 kHz and 1.6 kbyte ROD fragments at design luminosity



□ No particular issues

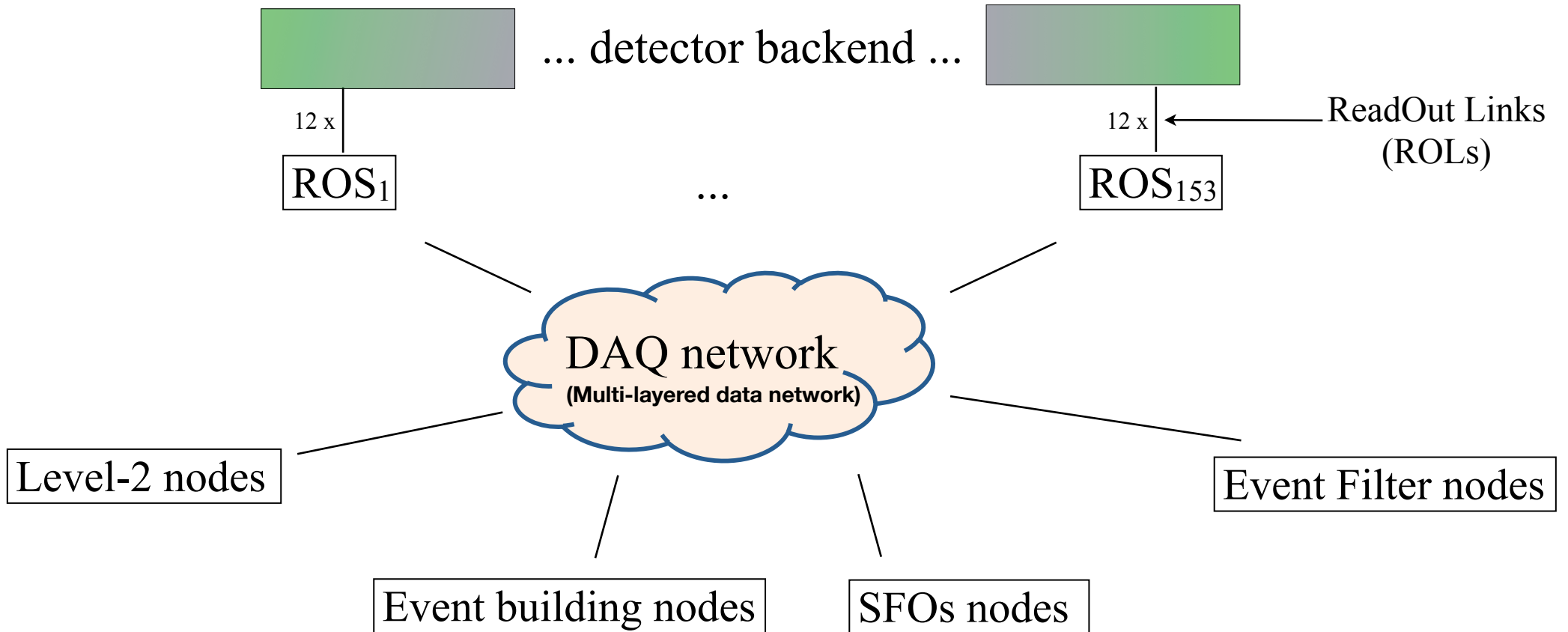
- o Detectors will de-multiplex
 - i.e. deploy more ROLs
 - DAQ deploy more ROSSs
- o New detector (IBL) and upgraded CSC RODs compatible with current ROL
 - interface & bandwidth

DAQ @ LHC: ATLAS Upgrade overview

- ❑ ROS request rate and output bandwidth
 - ❑ Defined by the Trigger menu
 - ❑ Requirements
 - o 25% readout fraction per ROL @ 100 kHz for 12 ROLs @ 160 Mbyte/s
 - o Level-1 accept rate up to 120 kHz
 - o > 200 Mbyte buffer per ROL
 - ❑ Targeting
 - o 50% readout fraction per ROL @ 100 kHz for 12 ROLs @ 160 Mbyte/s
 - ❑ Next generation ROS
 - o New ROBIN: use ALICE Common Readout Receiver Card (C-RORC)
 - o New ROS PC: More performant; 2x10 Gbit Eth.

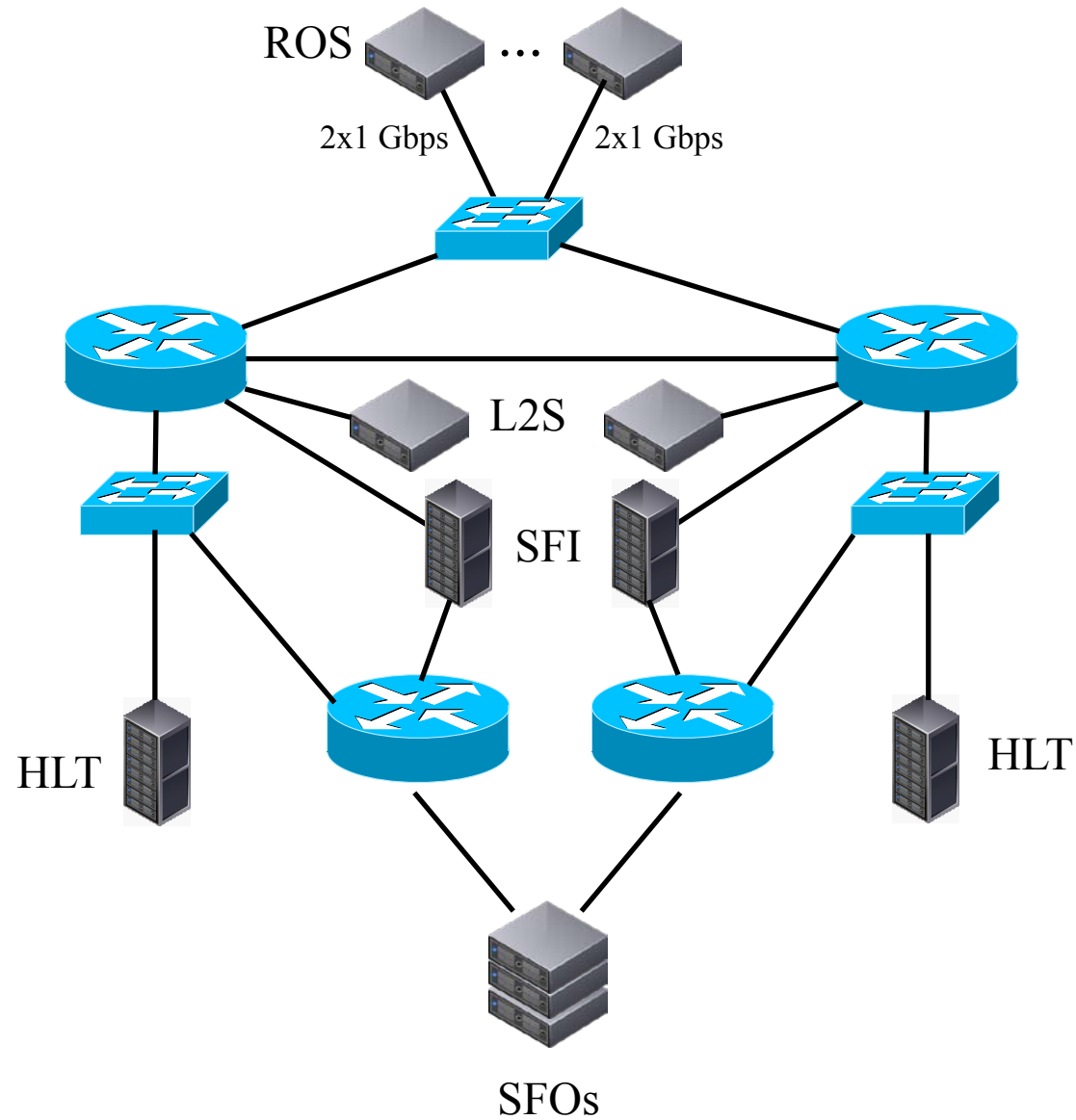
DAQ @ LHC: ATLAS Upgrade overview

□ ATLAS TDAQ ... to first order



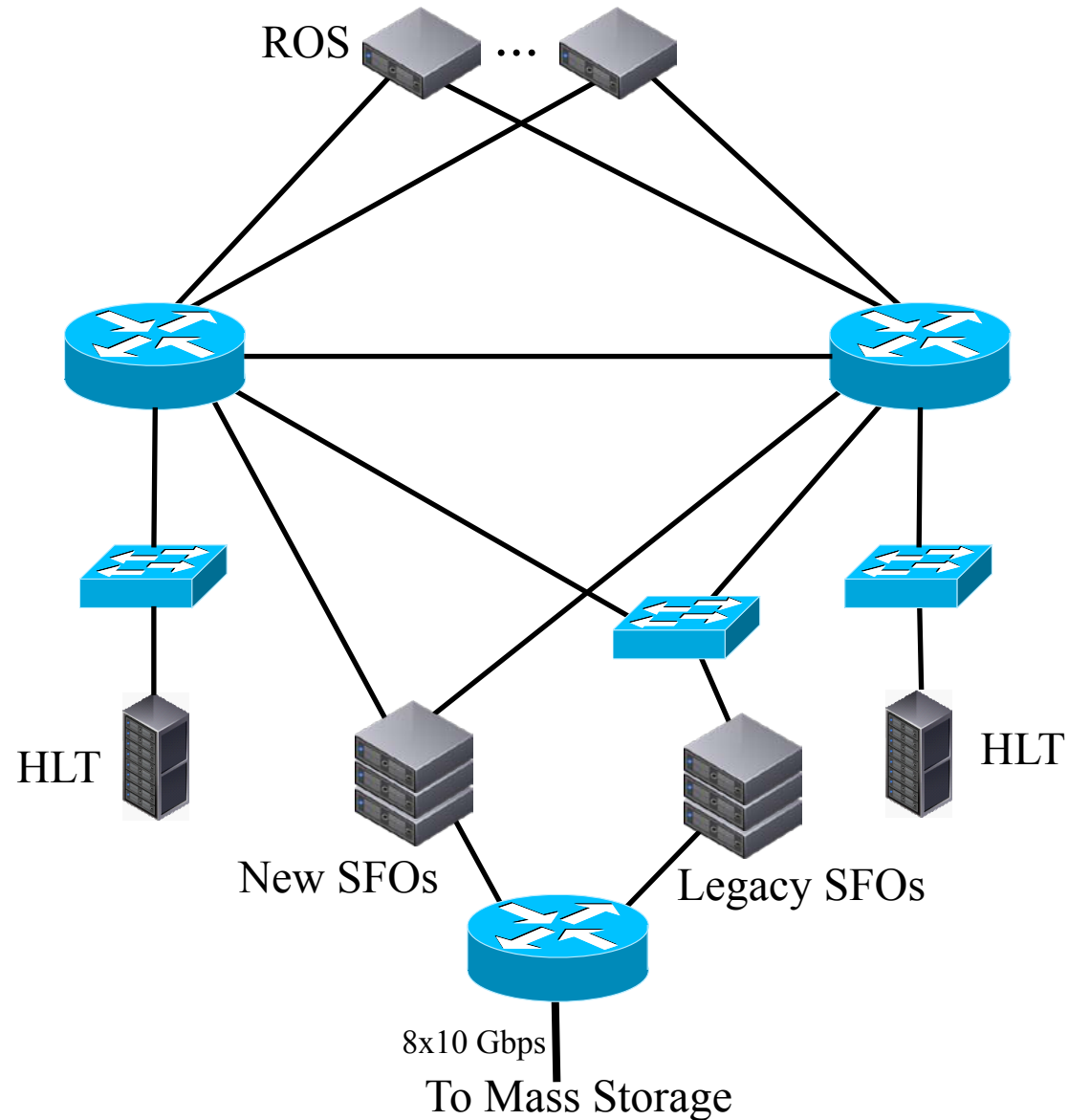
DAQ @ LHC: ATLAS Upgrade overview

□ Last month ...



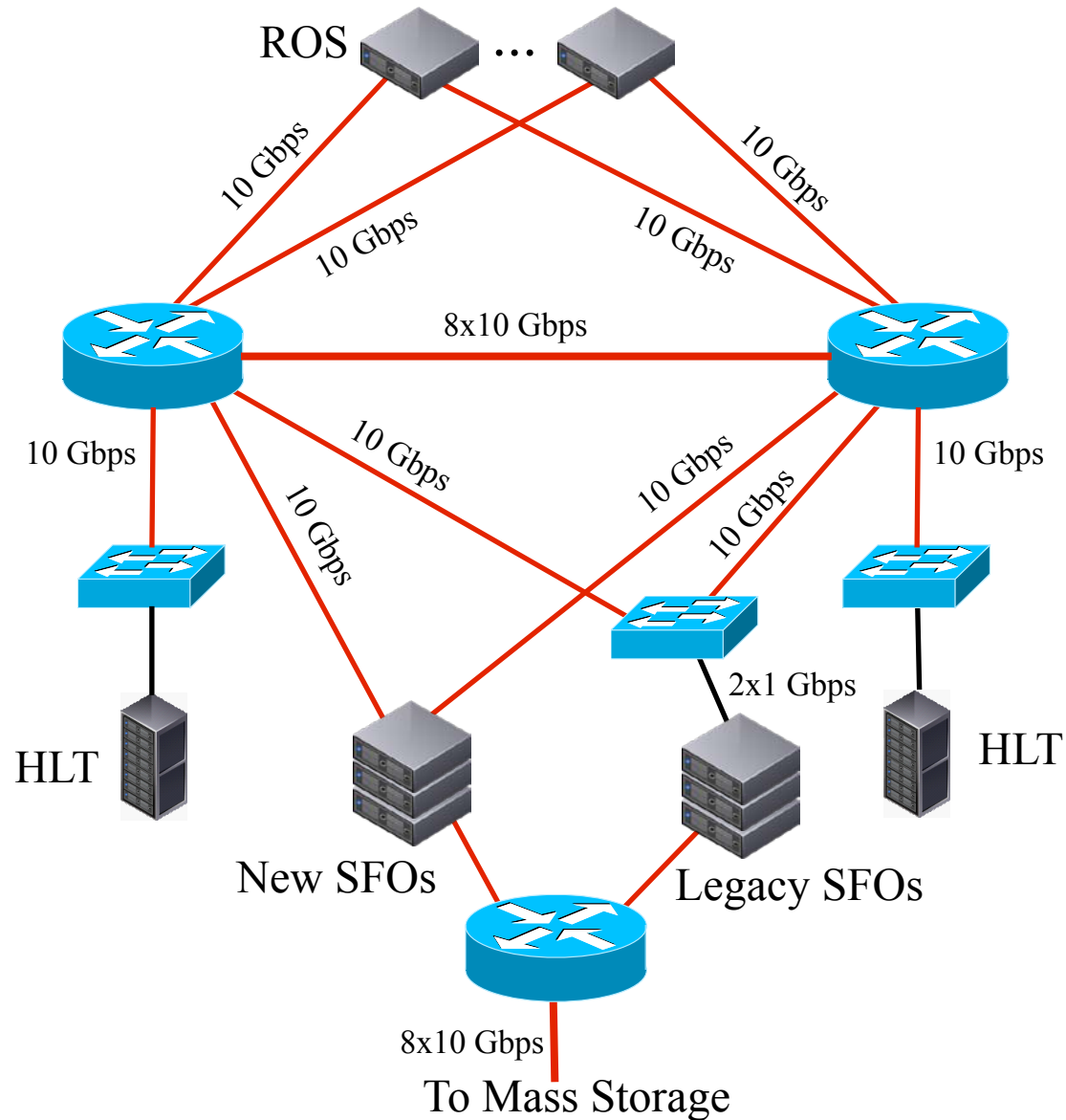
DAQ @ LHC: ATLAS Upgrade overview

□ As of last week (and in progress) ...



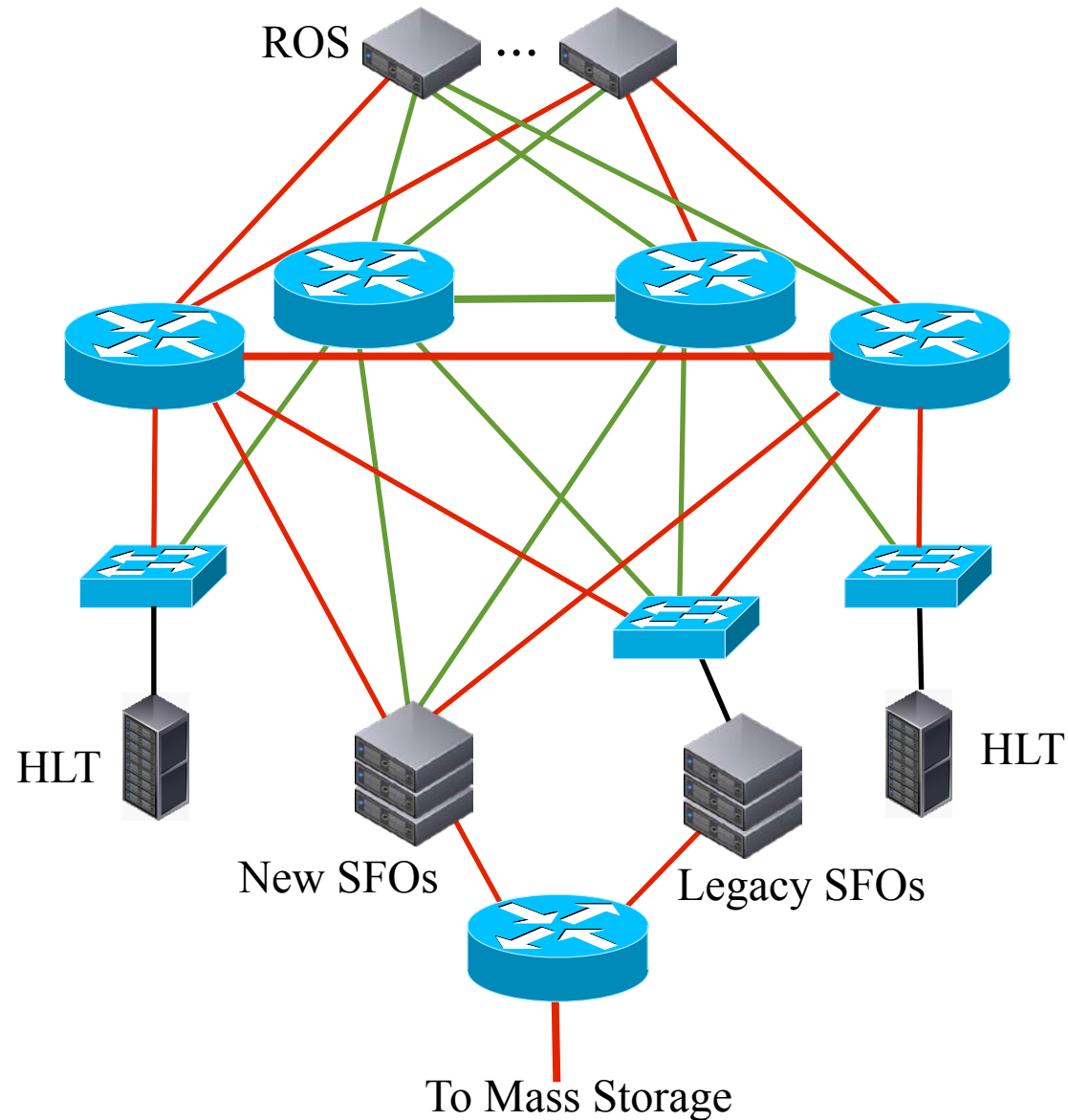
DAQ @ LHC: ATLAS Upgrade overview

□ As of last week ...



DAQ @ LHC: ATLAS Upgrade overview

- Increased connectivity—as required up to 2018



DAQ @ LHC: ATLAS Upgrade overview

□ ATLAS evolution at a glance

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	Other				Other				Other							

DAQ @ LHC: ATLAS Upgrade overview

□ Prepare for Phase II, i.e. Run 4

□ ATLAS Phase II Lol: Level-1 base line proposal

- o Two-stage synchronous First Level Trigger
 - Level-0 accept rate and latency of 500 kHz & ~3 μ s respectively
 - Level-1 accept rate and latency of **200 kHz** & ~17 μ s respectively
- o Event size at μ 200 ~5 Mbyte

□ Level-0 is the Level-1 Trigger used in Run 2–3

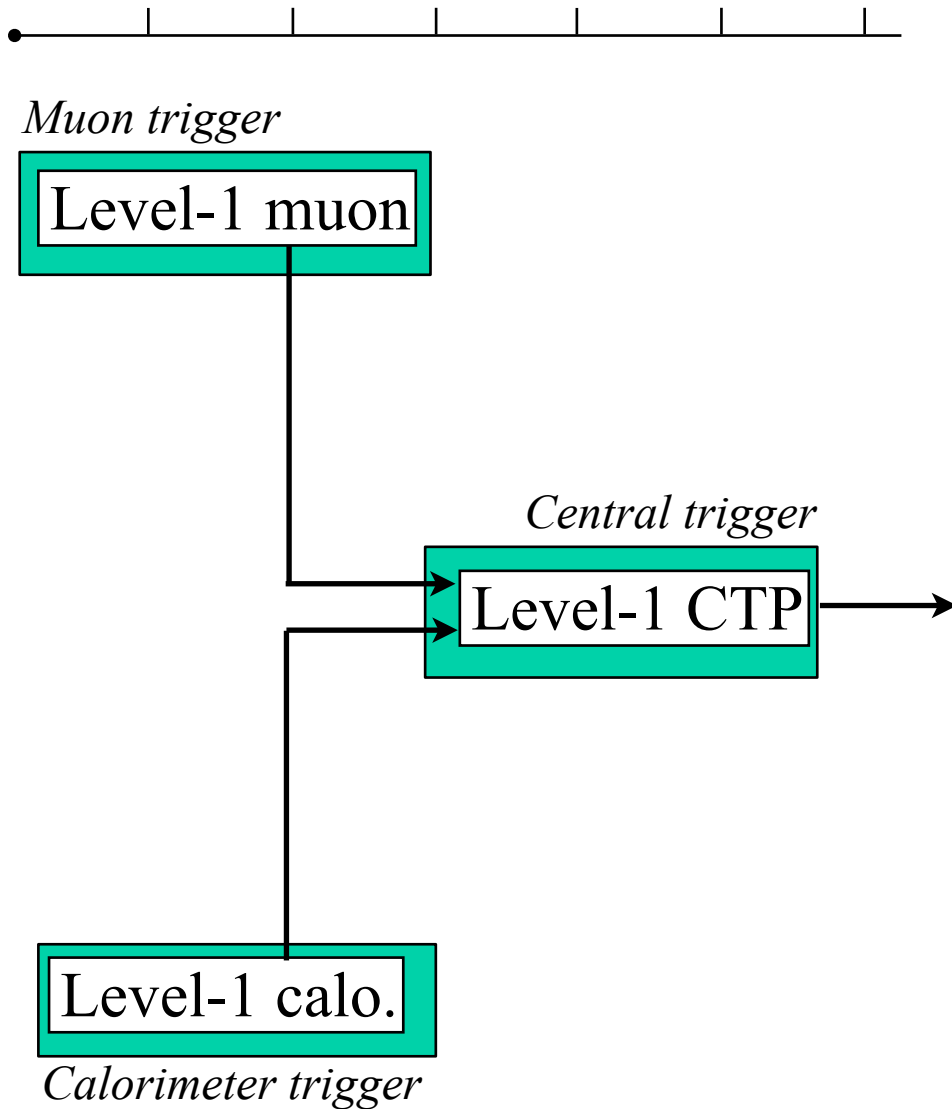
- o Calorimeter trigger: Digital Electron & Jet Feature extractor
 - Including associated changes to calorimeter electronics
 - Excluding today's Level-1 calorimeter trigger system
- o Muon trigger: today's L1Muon and use of New Small Wheel track segment
- o Exception: new Level-0 CTP

□ Level-1

- o RoI based **Track Finding** seeded by Level-0 calorimeter and muon Rols
- o Central trigger processor (including selection based on event topology)
- o Subject to further study, increased granularity calorimeter data (seeded by Level-0)
- o Subject to further study, use of MDT's in the End-cap (and Barrel?)

DAQ @ LHC: ATLAS Upgrade overview

~2 Time (μ s)

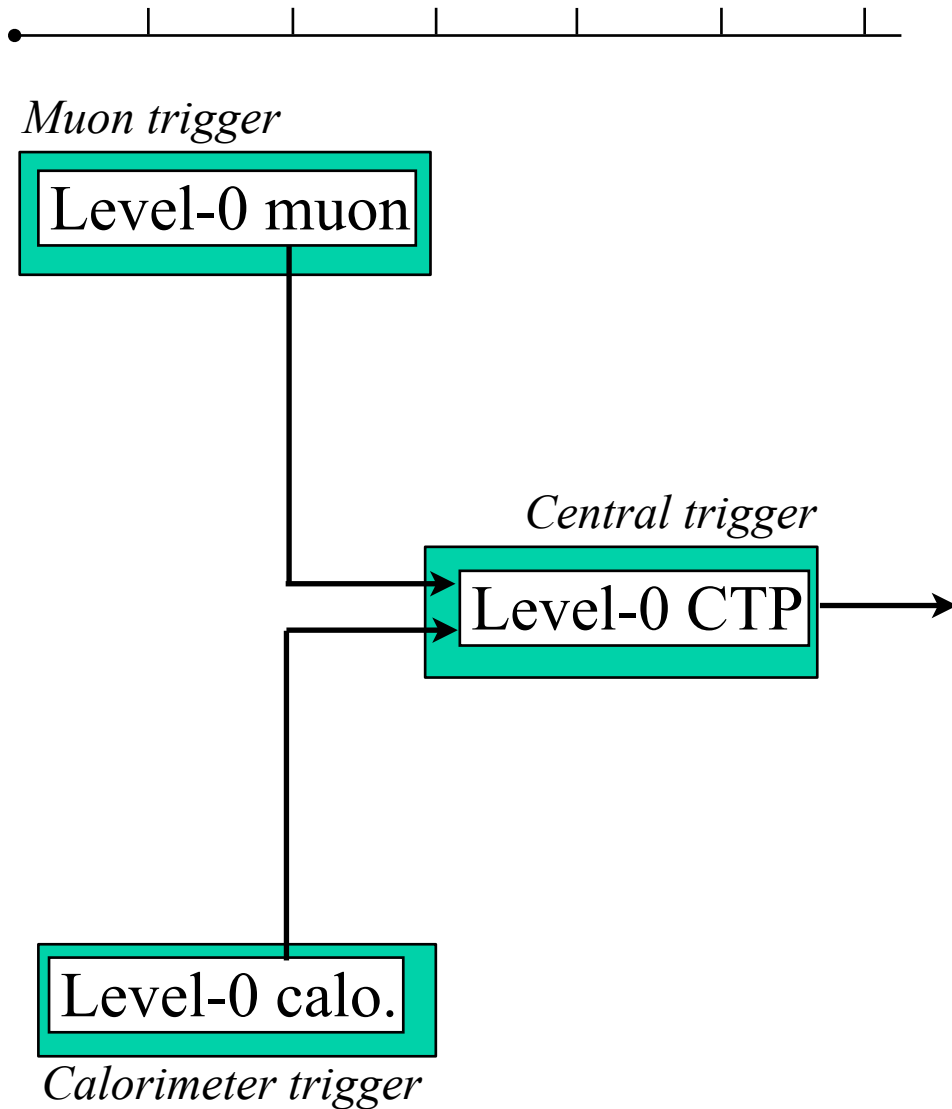


Rate (kHz)

~100

DAQ @ LHC: ATLAS Upgrade overview

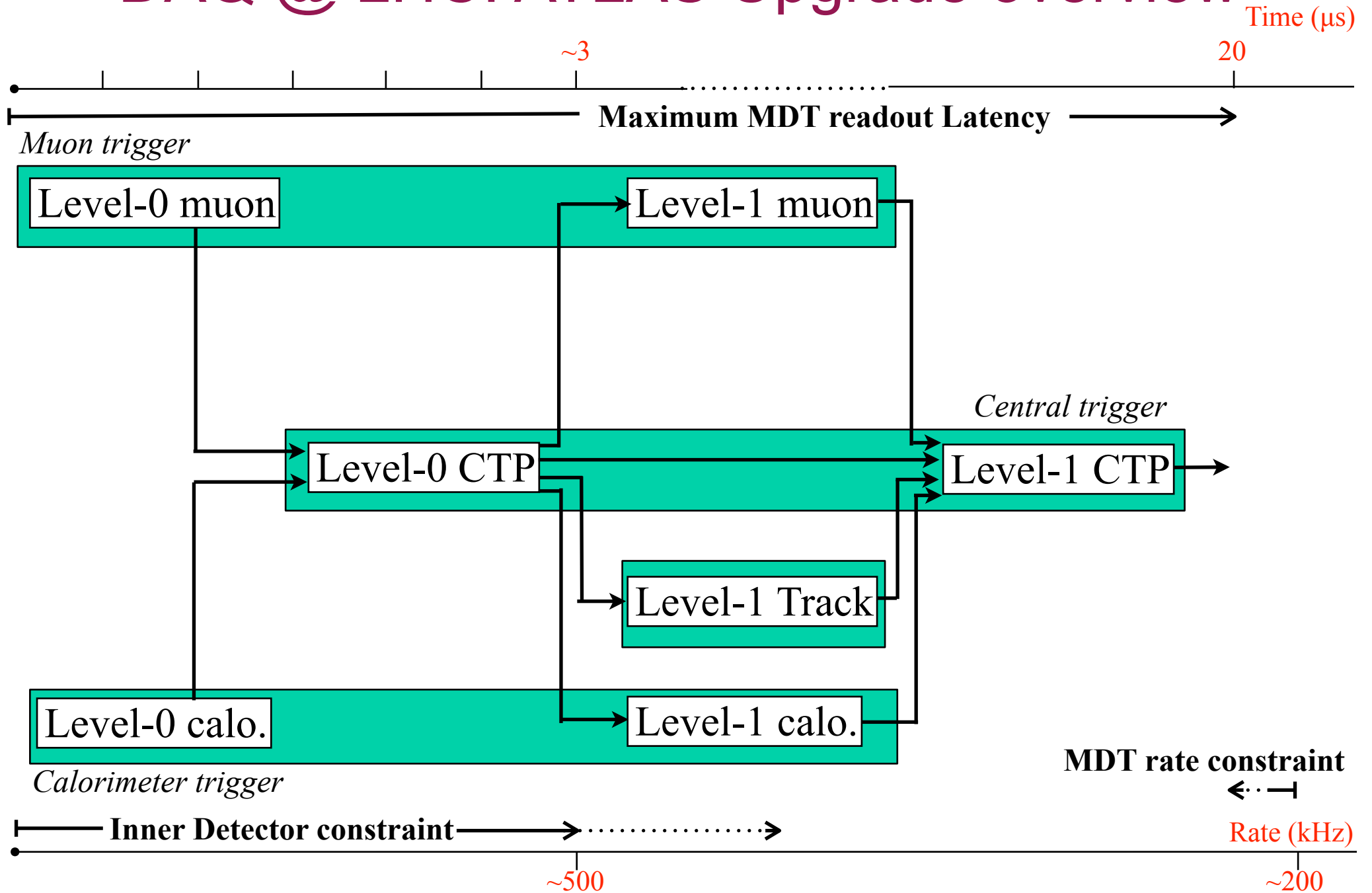
~3 Time (μs)



Rate (kHz)

~500

DAQ @ LHC: ATLAS Upgrade overview



DAQ @ LHC: ATLAS Upgrade overview

□ Summary

□ From 2014–2022

- o 100 kHz * 2.4 Mbyte from detector into read-out buffers
- o HLT selection requires up to 50% through network
→ 1 Tbit/s
- o At least 1 kHz x 2.4 Mbyte to storage

□ From 2022

- o Detector Readout: at least 200 kHz * 5 Mbyte into read-out buffers
 - New detector readout architecture ... blank paper
- o Assume HLT selection still only requires up to 50% through network
→ 5 Tbit/s

□ TDAQ stresses that 200 kHz is a minimal requirement

- o After all, full readout @ 200 kHz ... still only 10 Tbit/s
... 200 kHz → 500 kHz → 1 MHz?

□ Challenge is reading out detector at higher (Level-1) rates

- o (Potentially) legacy on-detector electronics
- o Front-end link bandwidth, i.e. Lol based on today's GBT