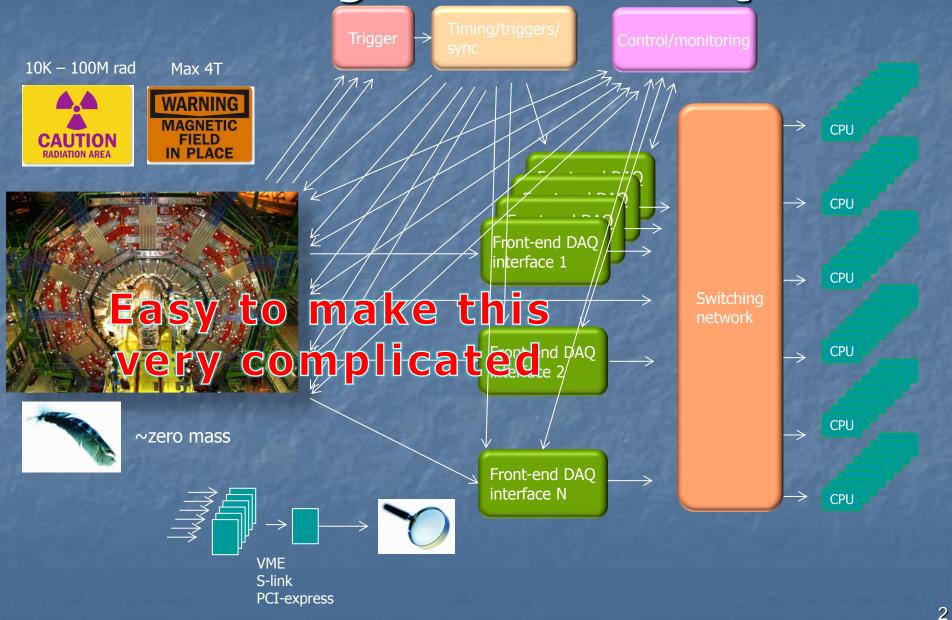
Links from experiments to DAQ systems

Jorgen Christiansen PH-ESE

Getting data into DAQ



Data and Link types

- Readout DAQ:
 - Unidirectional
 - Event frames.
 - High rate
 - Point to point
- Trigger data:
 - Unidirectional
 - High constant data rate
 - Short and constant latency
 - Point to point

- Detector Control System
 - Bidirectional
 - Low/moderate rate ("slow control")
 - Bus/network or point to point
- Timing: Clock, triggers, resets
 - Precise timing (low jitter and constant latency)
 - Low latency
 - Fan-out network (with partitioning)
- We often keep these data types physically separate and each link type has its own specific implementation
- Multiple exceptions
 - Merge timing and control/monitoring: CMS CCU, LHCb SPECS, ,
 - Combine readout and control: ALICE DDL (Used for DCS ?),
 - Use same link implementation for readout and trigger data
 - But never have readout and trigger data on same physical link
 - Down: Control data with Timing. UP: Monitoring data with Readout: ATLAS pixel/SCT, ,

Links in ATLAS

Large confined/enclosed experiment with high radiation. ~100KHz trigger

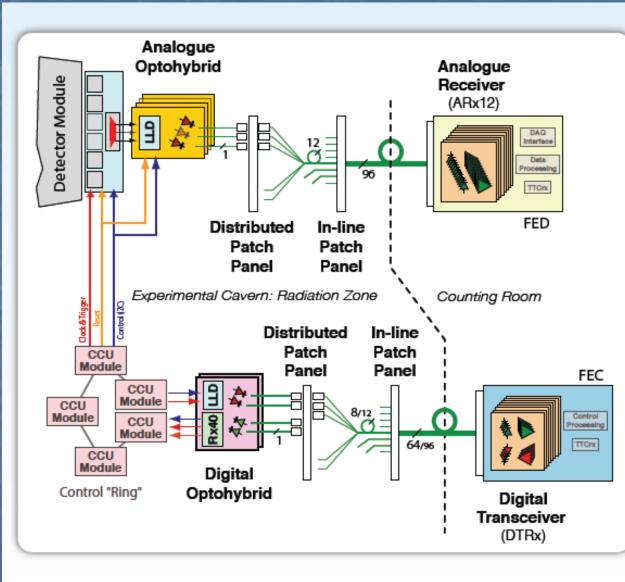
Detector	Purpose	Media	Rate Mbits/s	Quantity	Comment
Pixel	DAQ/TTC/DCS	Optical	40 (80)	250	Custom
SCT	DAQ/TTC/DCS	Optical	40	8200	Custom
TRT	TTC/DCS	LVDS-Cu	40	400	Custom
	DAQ/DCS	LVDS – Optical	40 - 1600	400	GOL
Ecal	TTC	Optical	80		TTC link
	DCS	LVDS-Cu			SPAC
	DAQ	Optical	1600	1600	Glink
	Trigger	Cupper		Sub-det.	Analog
Hcal	TTC	Optical	80		TTC link
	DCS	Cupper			CAN
	DAQ	Optical	1600	512	Glink
	Trigger	Cupper			Analog
CSC, RPC, TGC	DAQ	Optical	1600	1200	Glink
MDT	DAQ	Optical	1600	1200	GOL
CSC	ТТС	Optical	1600	200	Glink
CSC, RPC, TGC, MDT	DCS	Cupper			CAN
RPC	Trigger	Optical	1600		Glink

Links in CMS

Large confined/enclosed experiment with high radiation. ~100KHz trigger

Detector	Purpose	Media	Rate Mbits/s	Quantity	Comment
Pixel - strip	TTC/DCS	Optical	80		CCU, Custom
	DAQ	Optical	40Msamp ~320	40.000	Custom analog
Ecal	TTC/DCS	Optical	80		CCU, Custom
	DAQ	Optical	800	11.000	GOL
	Trigger	Optical			GOL
Hcal	TTC				?
	DCS				?
	DAQ	Optical	800		GOL
	Trigger		800		GOL
Muons	TTC				
	DCS				
	DAQ		800		GOL
	Trigger				

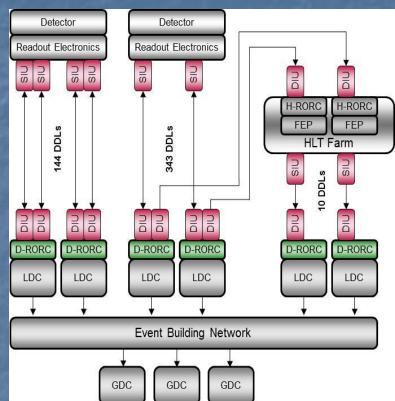
Example: CMS tracker links



Readout System				
INL	1%			
SpNR	48 dB			
BWtyp	70 MHz			
Gain	0.8 V/V			
~40000 Fibres				
Control System				
Data-Rate	80Mb/s			
BER	10-12			
~2500 Fibres				
Length: 40-65m				
Low Mass & Volume				
Non-Magnetic				
Radiation Resistant				

Links in ALICE

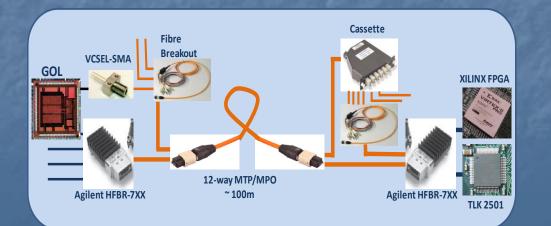
- Low radiation levels (but can not be ignored) Specialized/qualified COTS solutions can be used Low trigger rate (10KHz) but very large events Standardized readout links: DDL Some front-ends use directly DDL interface card . (can stand limited radiation: COTS + SEU tolerance) • Others (inner trackers, TRD) use optical links (e.g. GOL) to crates that then interfaces to DDL. ■ ~400 DDL links of 2125 Mbits/s Link card plugs into PCI-X slots (must evolve with PC backplane technology) DCS: Use of single board computer with Ethernet (Very low radiation levels)
- Trigger data: ?
- TTC



Links in LHCb

- Open detector so easier to get data out
- 1MHz trigger rate
- Came later than the other experiments and profited from link developments already made (GOL).
- Standardized links (with 1 exception)
 - DAQ and trigger data: GOL 1800Mbits/s, ~5.000 Links
 - (Vertex: multiplexed analog links to counting house)
 - DCS: SPECS (Custom COTS) and CAN
 - TTC: TTC

Standardized readout module: TELL1 (with 1 exception)





What to do for the future

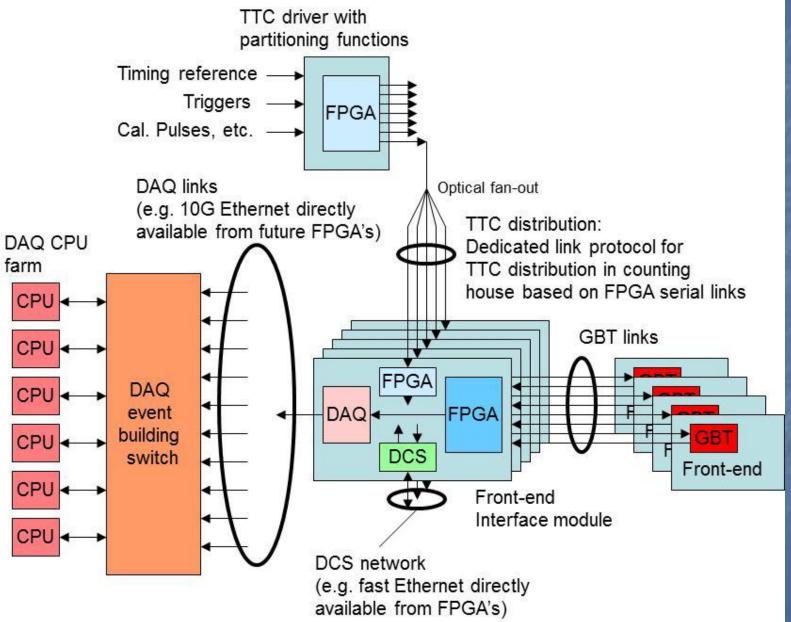
One standardized optical link doing it all. Dream ?. We MUST try !.

- Must be available early to be used/adopted by our community (but takes looong to develop).
- Support for its use

• Requirements:

- General:
 - Optical
 - Bi-directional
 - High data rate: ~ 5Gbits/s (mainly from FE to DAQ) (10Gbits/s version for phase 2 ?)
 - Reliable
 - Low and constant latency (for TTC and trigger data paths)
- Front-end: Radiation hard ASICs (130nm) and radiation qualified opto-electronics
 - Radiation hard (>100Mrad), SEU immunity
 - "Low" power
 - Flexible front-end chip interface
- Back-end: COTS
 - Direct connection to high-end FPGA's with multiple/many serial link interfaces
- Project : GBT ASICs, Versatile opto, FPGA firmware, GBT Link Interface Board (GLIB).
 - This is one of our major projects in the PH-ESE group in collaboration with external groups to have our "dream" link ready for the upgrade community within ~1 year.
 - This has been a large investment (money and manpower for the last 5 years)

How can this look



GBT, Versatile, GLIB



Summary & Conclusions

Current LHC DAQ systems

- Front-end links not directly part of what we term(ed) (common/central) DAQ systems, but they have had a
 major impact on the data collection (DAQ system) architecture, detector interfaces and required system
 debugging.
- A large number of different links implies a large set of different front-end/DAQ interface modules.
 - Each link and associated link/DAQ interface has been optimized for its specific use in each sub-detector system
- We tend to physically separated TTC, Slow control/monitoring, DAQ data and Trigger data information.
 - Many exceptions in different sub-systems with different mixtures.
- No satisfactory rad hard link existed to cover all the different needs

Future front-end links and interfaces

- One link can carry all types of information: GBT + Versatile
 - If one link fails then we completely loose everything from this detector part (but this is in practice also the case if any of the "4" distinct links fails to a detector part). Redundancy is an other (long) discussion subject.
 - Different links/networks/fan-outs/etc. for the different information in the counting house (use of COTS) ?.
 - A "standardized" radhard high rate optical link must be available early to be adopted by our community and takes significant time and resources to develop: Start development **as early as possible**!.
- One type of front-end DAQ module for all sub-detectors ?
 - FPGA's are extremely versatile and powerful (and continuously becomes even more powerful)
 FPGA's now use internal standardized data busses and networks (what we before did at the crate level)
 - **Implement final module as late as possible** to profit from the latest generation technology.

 The front-end links and interface modules are vital and critical parts of DAQ/data collection systems !.

Why not DAQ network interface directly in front-ends ? This is obviously what we would ideally like but: Complicated DAQ network interfaces (network) protocol, packet routing, data retransmission, buffering, etc.) will be very hard to (build to) work reliable in hostile radiation environment. We can not use flexible high performance COTS components (FPGA's, DSP, CPU, etc.) Power consumption Mass We can not upgrade DAQ network as hardwired into "old" front-end electronics.