2012 H4IRRAD test campaigns
Summary of results

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2012 H4IRRAD test campaigns

3 H4IRRAD slots have been defined in 2012

- 1st slot – May 15, 2012 – June 3, 2012
  - MAX5541 – 16-bit DAC
  - ADS1281 – Delta-Sigma ADC
  - DS18B20 – 1-wire thermometer
  - DS2401 – 1-wire ID
  - SPLargeUHD9 – 130nm SP SRAM
- 2nd slot – Aug 03, 2012 – Aug 17, 2012
  - MAX5541 – 16-bit DAC
  - MIC37302 – Voltage regulator
- 3rd slot – Nov 15, 2012 – Dac 3, 2012
  - MIC37302 – Voltage regulator
  - FGClite proto

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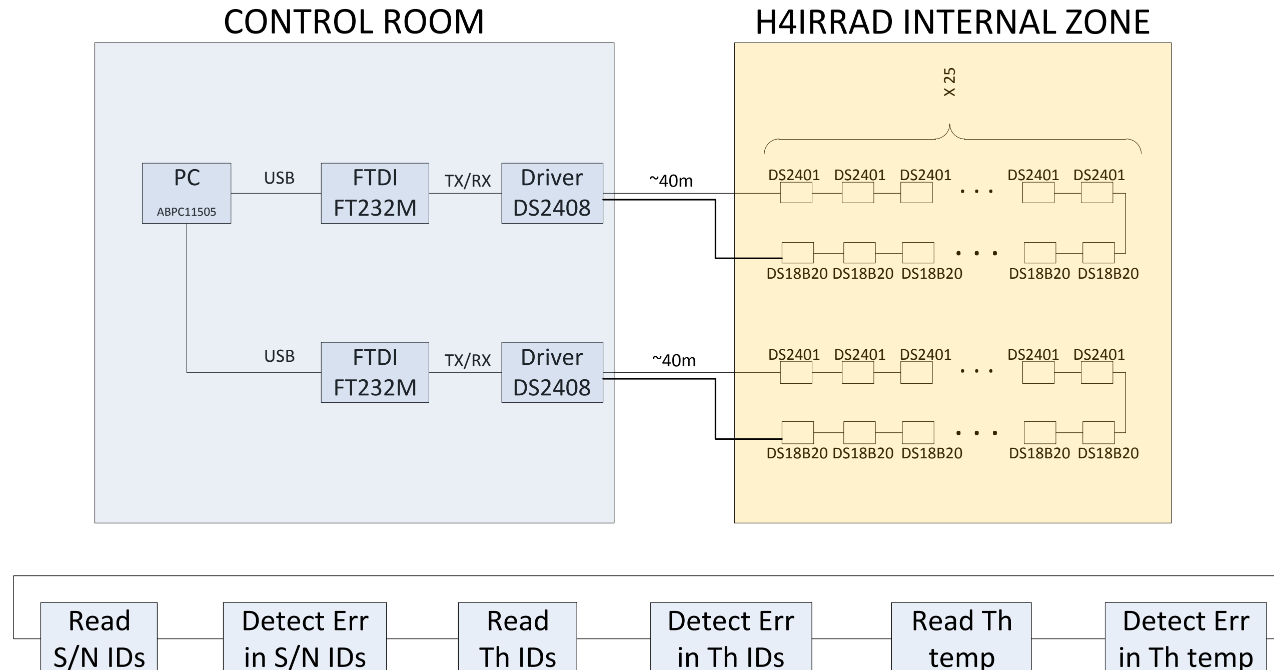
DS18B20/DS2401 (1/3)

DUT description:

DUT name	DUT type	Test type	Samples tested	Package	Date code	Lot code
DS18B20	1-wire thermometer	SEE, TID	2 x 25	TO-92	unknown	unknown
DS2401	1-wire ID	SEE, TID	2 x 25	SOT-223	9931C2	DM914705AIB

Tester architecture and test procedure:



DS18B20/DS2401 (2/3)

Beam conditions:

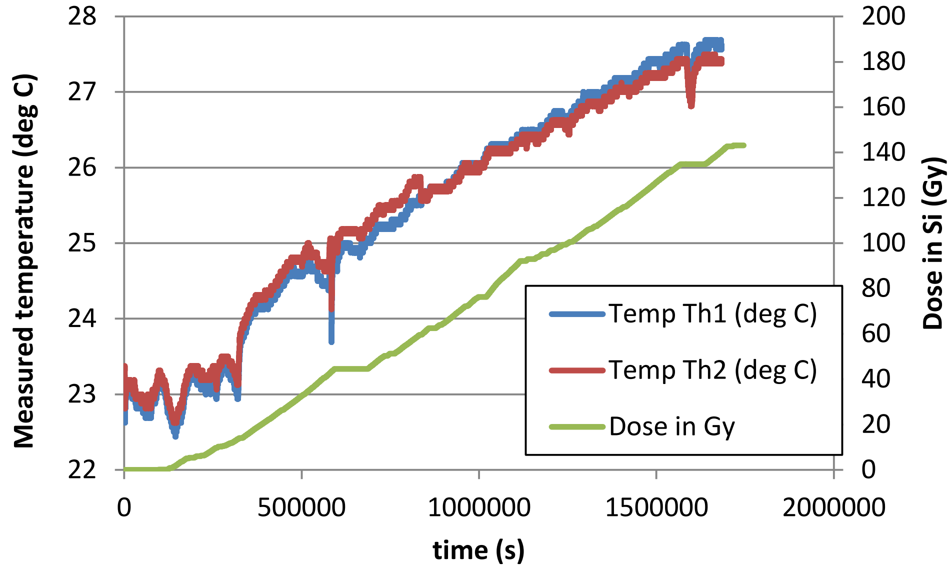
Run	Run start date	Run end date	Dose in Gy ± 50%	HEH per cm2 ± 50%	1 Si MeV Neq ± 50%	thermal neutrons ± x2
1	May 15, 2012 @ 3:05pm	May 22, 2012 @ 12:30pm	4.5E+01	8.1E+10	3.3E+11	3.8E+10
2	May 22, 2012 @ 02:07pm	May 25, 2012 @02:11pm	1.8E+01	3.3E+10	1.3E+11	1.5E+10
3	May 25, 2012 @ 02:11pm	Jun 04, 2012 @09:41am	8.1E+01	1.5E+11	5.9E+11	6.9E+10

SEE test results:

Run	Run start date	Run end date	Iterations	S/N ID err	S/N comm err	Th ID err	Th Comm Err	Th temp err
1	May 15, 2012 @ 3:05pm	May 22, 2012 @ 12:30pm	19217	0	0	0	9	6
2	May 22, 2012 @ 02:07pm	May 25, 2012 @02:11pm	7621	0	0	0	2	1
3	May 25, 2012 @02:11pm	Jun 04, 2012 @09:41am	27229	0	0	0	87	6

DS18B20/DS2401 (3/3)

Temperature drift:



Conclusions:

Temperature measurement drift observed during the slot is equal to 3.3e-2 ±1.2° C/Gy

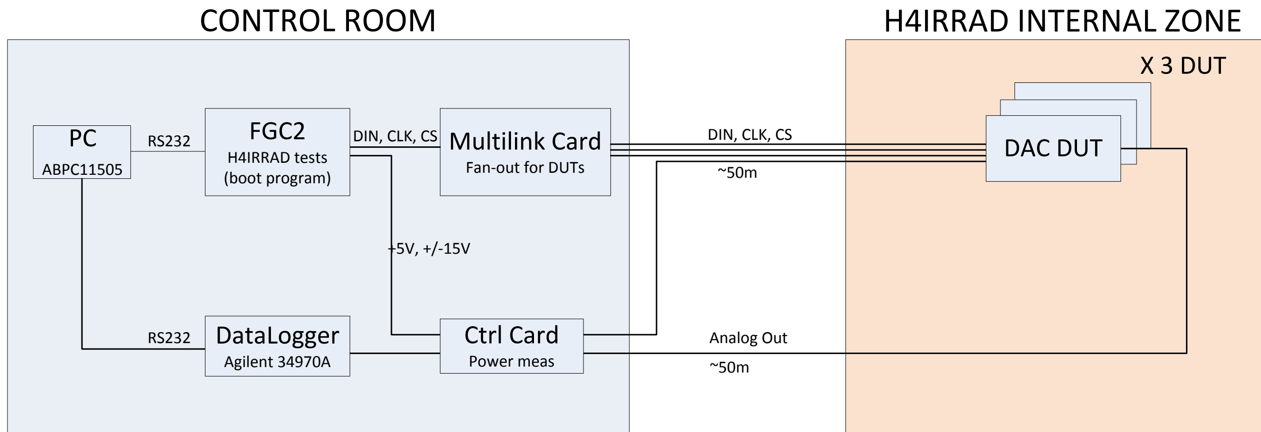
Component	Dose (Gy) ±50%	S/N ID err (cm2/HEH)	S/N comm err (cm2/HEH)	Th ID err (cm2/HEH)	Th Comm Err (cm2/HEH)	Th temp err (cm2/HEH)
S/N (DS2401)	143	<4.4E-12	<4.4E-12	X	x	x
Th (18B20)	143	x	x	<4.4E-12	5.6E-10	9.2E-11

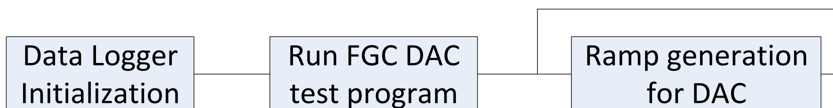
MAX5541 (1/2)

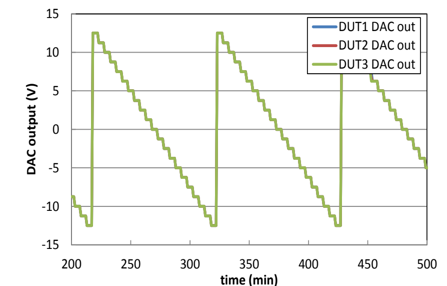
DUT description:

DUT name	DUT type	Test Type	Samples tested	Packag e	Date code	Lot code
MAX5541	16-bit DAC	TID, SEE	3	DIP/SO	unknown	unknown

Tester architecture and test procedure:







MAX5541 (2/2)

Beam conditions:

DUT num	Test start date	Test end date	Dose in Gy ± 50%	HEH per cm2 ± 50%	1 Si MeV Neq ± 50%	thermal neutrons ± x2
1	15/05/2012 12:01	04/06/2012 16:56	1.35E+02	2.14E+11	8.61E+11	1.18E+11
2	15/05/2012 12:01	04/06/2012 16:56	1.23E+02	2.02E+11	8.54E+11	1.16E+11
3	15/05/2012 12:01	04/06/2012 16:56	1.18E+02	1.90E+11	8.18E+11	1.12E+11

Results:

- Components have been irradiated up to 135, 123 and 118 Gy, no power consumption increase after irradiation, all components fully functional
- No SEL have been detected
- No SEFI/SETs have been observed during the slot

SEL XS upper level < 3.80e-12

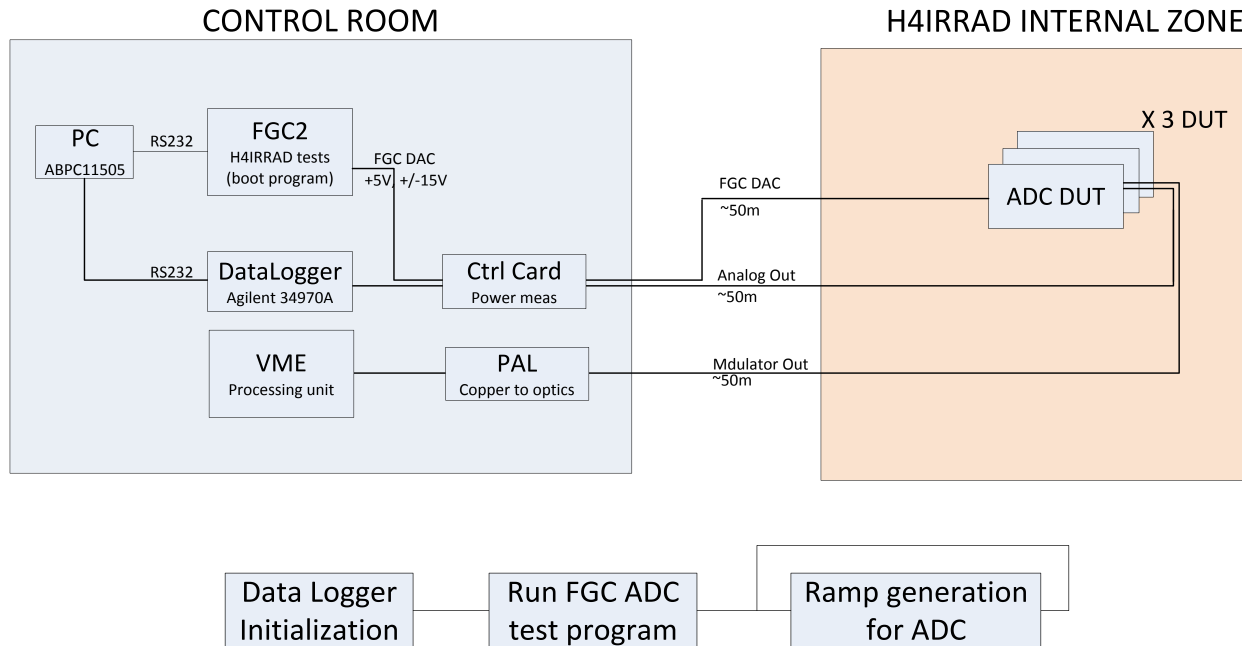
SEU/SEFI XS upper level < 3.80e-12

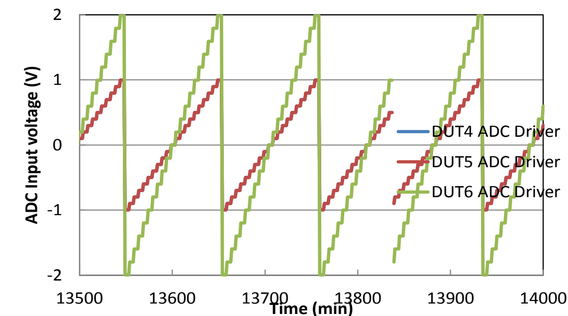
ADS1281 (1/2)

DUT description:

DUT name	DUT type	Test Type	Samples tested	Package	Date code	Lot code
ADS1281	High-Res ADC	TID, SEE	3	TSSOP-24	unknown	unknown

Tester architecture and test procedure:





ADS1281 (2/2)

Beam conditions:

DUT num	Test start date	Test end date	Dose in Gy ± 50%	HEH per cm2 ± 50%	1 Si MeV Neq ± 50%	thermal neutrons ± x2
1	15/05/2012 12:01	04/06/2012 16:56	1.28E+02	2.50E+11	1.00E+12	1.24E+11
2	15/05/2012 12:01	04/06/2012 16:56	1.64E+02	2.34E+11	9.49E+11	1.19E+11
3	15/05/2012 12:01	04/06/2012 16:56	1.32E+02	2.21E+11	9.05E+11	1.23E+11

Results:

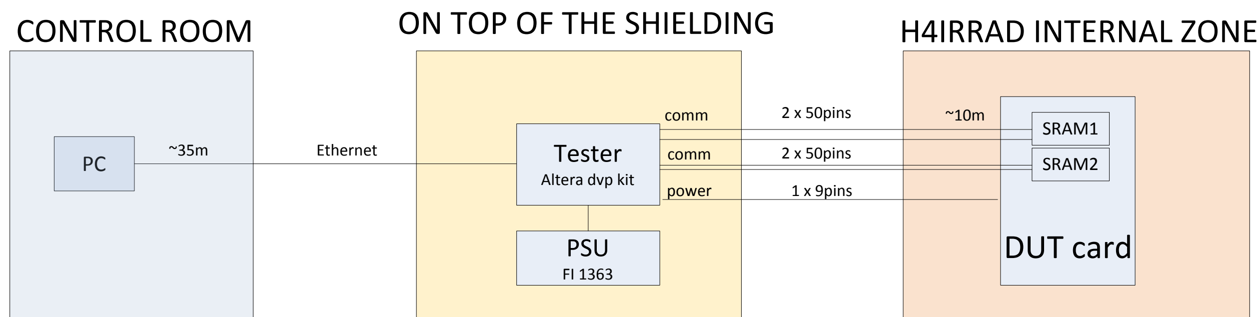
- Components have been irradiated up to 164, 132 and 128 Gy
- No SEL have been detected:
  SEL XS upper level < 8.06E-13
- No SEFI/SETs have been observed during the slot
  SEFI XS upper level < 8.06E-13
  SEU on M0 upper level < 1.31E-12
  SEU on M1 upper level < 1.53E-12
- No significant power consumption increase have been observed

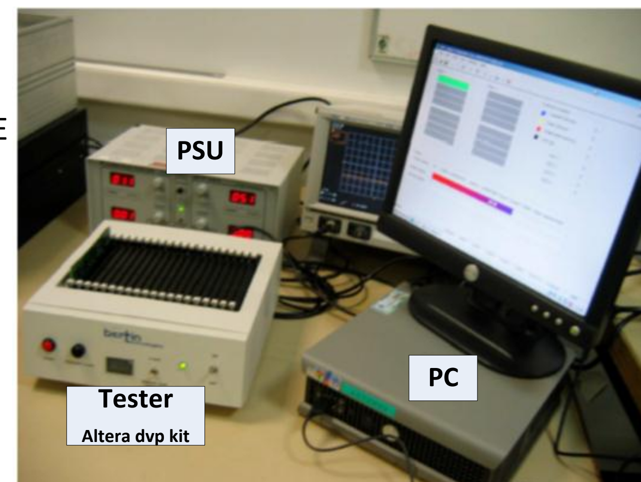
SPLargeUHD9 (1/2)

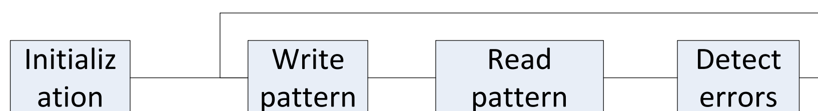
DUT description:

DUT name	DUT type	Test Type	Samples tested	Package	SRAM generator version	Lot code
SPLargeUHD chip 1	CMOS SRAM	TID, SEE	1 x 4Mbit	PBGA 256+16	6.1.1@20021219.0	unknown
SPLargeUHD chip 2	CMOS SRAM	TID, SEE	1 x 4Mbit	PBGA 256+16	6.1.1@20021219.0	unknown

Tester architecture and test procedure:







SPLargeUHD9 (2/2)

Beam conditions:

	Test start date	Test end date	Dose in Gy ± 50%	HEH per cm2 ± 50%	1 Si MeV Neq ± 50%	thermal neutrons ± x2
‘A’/‘5’	15/05/2012 15:00	22/05/2012, 14:54:45	5.2E+01	9.2E+10	3.0E+11	4.0E+10
‘A’/‘5’	23/05/2012, 10:42:30	25/05/2012, 14:07:52	2.1E+01	3.7E+10	1.2E+11	1.6E+10
‘0’/‘1’	25/05/2012, 15:52:16	04/06/2012, 09:02:25	9.4E+01	1.7E+11	5.4E+11	7.2E+10
‘0’/‘1’	15/05/2012 15:00	04/06/2012, 09:02:25	1.6E+02	3.0E+11	9.6E+11	1.3E+11

SEE test results:

Run	#SEU	#MBU (2)	Events Chip1	Events Chip2	SEU XS (cm2/bit)	MBU XS (cm2/bit)	Total XS (cm2/bit)
1 (0xAA/0x55)	53084	193	24716	28368	6.9E-14	7.7E-17	6.9E-14
2 (0x00/0xFF)	18645	1462	8579	10066	6.0E-14	1.5E-15	6.3E-14
3 (0x00/0xFF)	86000	7118	39547	46453	6.1E-14	1.6E-15	6.5E-14

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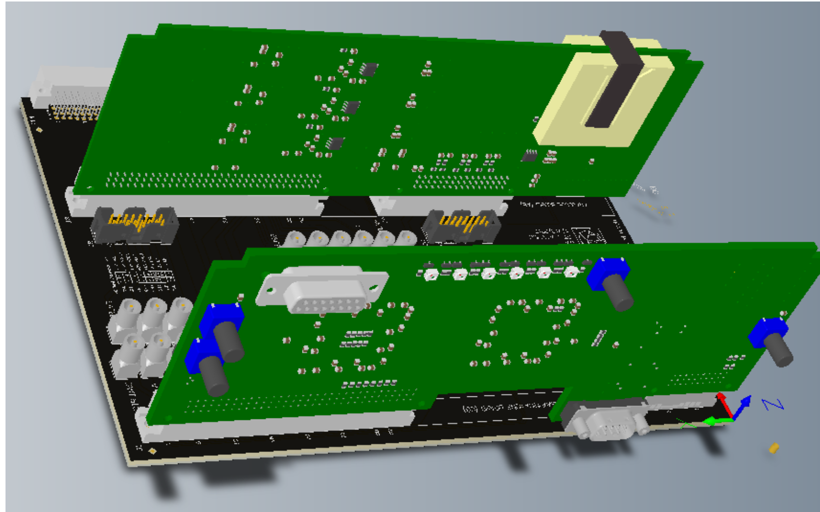

Results:

- First FGClite mixed-field validation: Analog card, Network card and Simplified main board
- GW will send the voltage reference and will read back the measurements on 3 channels
- This test will allow us to:
  - Compute the SEL XS thanks to power monitoring and power cycling feature
  - Compute the SEFI/SEU XS of analog measurements