Digital signal integrity and stability in the ATLAS Level-1 Calorimeter Trigger

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The ATLAS first-level calorimeter trigger is a hardware-based system designed to identify high-pT jets, electron/photon and tau candidates and to measure total and missing ET in the ATLAS calorimeters. Apart from the initial analogue stage, the trigger system consists of a multi-stage pipelined digital processor distributed over several crates of custom-built modules. The high demands for interconnectivity between both crates and modules are solved by a variety of high-speed digital links, using several signaling standards, including both electrical and optical transmission. The techniques used to establish timing regimes, and verify correct connectivity and stable operation of these digital links, will be presented.

Summary

The ATLAS first-level calorimeter trigger (L1Calo) is a hardware-based system with a high degree of adaptability provided by widespread use of FPGAs. The real-time path of the trigger is subdivided into a Preprocessor, which takes analogue signals from the calorimeters and digitizes them, followed by two digital processor systems working in parallel: the Jet/Energy-sum processor and the Cluster Processor. The full system has been installed since the end of 2007, and has now been tested both stand-alone and in integrated runs with the rest of ATLAS over a long period.

The overall performance of the trigger in ATLAS commissioning and early LHC data is discussed in a separate contribution, as is the analysis of the analogue signals from the calorimeters. This contribution will detail the methodology and results of commissioning the many digital links needed to perform the trigger processing.

There are many separate stages of digital connectivity along the various processing paths in the L1Calo system, each with different contraints, and therefore almost as many different solutions to the challenges at each stage. The choices of technology were governed by the required band-width into and out of each processing element, be it an FPGA, module or crate. The basic unit of input to the digital processor is an 8-bit calibrated transverse energy value, of which there are over 7000 instances. The algorithms demand that many of these are used as input to multiple instances of each algorithm. The processing clearly must be performed in parallel, but the overlapping nature of the algorithms means that much of the data must be duplicated to several locations.

The vast majority of the inter-crate digital connectivity is used to transfer the individual energies to the algorithm processing systems. This is achieved using high-speed serial LVDS links. Over 7000 differential pairs are required, and both the exact connectivity and correct timing of these signals is crucial to the performance of the trigger. The methods used to establish a good timing regime, and also to verify that no cables are misconnected, will be presented.
Within the digital processor crates, the challenge of inter-module connectivity is met by a dense custom backplane with approximately 22,000 pins per crate. This carries digital signals of various standards and at different speeds. For the real-time path, the fastest signals run at 160 Mbit/s using a single ended protocol to minimize pin count. These connections also require careful timing and verification, and results of these tests will be shown.

Amongst the other digital links in the system are the readout links, which allow data to be recorded in order to verify the correct performance of the trigger. All significant modules in the system provide read-out data, and a common link solution was used by all modules to send this data. This consists of optical fibres using a serial transmission protocol. All such read-out fibres are routed to Readout Drivers, which differ only in the firmware load needed to format the data for each module. These, and other, links were also tested for stability and correct data transmission, and the methodology and results will be presented.

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