Skiroc : a Front-end Chip to Read Out the Imaging Silicon-Tungsten Calorimeter for ILC

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Abstract

Integration and low-power consumption of the read-out ASIC for the International Linear Collider (ILC) 82-million-channel W-Si calorimeter must reach an unprecedented level as it will be embedded inside the detector. Uniformity and dynamic range performance has to reach the accuracy to achieve calorimetric measurement. A first step towards this goal has been a 10,000-channel physics prototype of 18*18 cm which was in test beam in Fermilab in summer 2008.

A new version of a full integrated read out chip (SKIROC) has been designed to equip the technologic prototype to be built for 2009. Based on the running physics prototype ASIC (FLC_PHY3), it embeds most of the required features expected for the final detector.

The dynamic range has been improved from 500 to 2000 MIP. An auto-trigger capability has been added allowing built-in zero suppress. The number of channel has been doubled reaching 36 to fit smaller silicon pads and the low-noise charge preamplifier now accepts both AC and DC coupled detectors. After an exhaustive description, the measurement results of that new front-end chip will be presented. The results on the technological R&D concurrently conducted on the ultra-thin PCB hosting both the front-end electronic and the silicon detectors will also be described.

• I - INTRODUCTION

Integration and low-power consumption of the read-out ASIC for the International Linear Collider (ILC) 82-million-channel W-Si calorimeter must reach an unprecedented level as it will be embedded inside the detector. Uniformity and dynamic range performance has to reach the accuracy to achieve calorimetric measurement. A first step towards this goal has been a 10,000-channel physics prototype of 18*18 cm which is currently in test beam in Fermilab.

A new front-end chip called SKIROC – standing for *Silikon Kalorimeter Read-Out Chip* – has been designed to read-out the upcoming generation of Si-W calorimeter featuring ILC requirements. The analogue core of SKIROC is based on the front-end electronic designed for that physics prototype. The Maximum input charge has been extended from 500 to 2000 MIP. The number of channel has been doubled – reaching 36 - to fit a pad size reduction in the silicon detector design conducted concurrently. A stand alone working capability comes along with the full power pulsing feature. That means SKIROC does not need any external component such as decoupling capacitance or bias resistor involving a huge room saving. The wake up sequence duration of the power pulsing is around 2μs to ensure a lower than 1% duty cycle in an ILC-like beam structure [1], involving more than two order of magnitude of power saving.
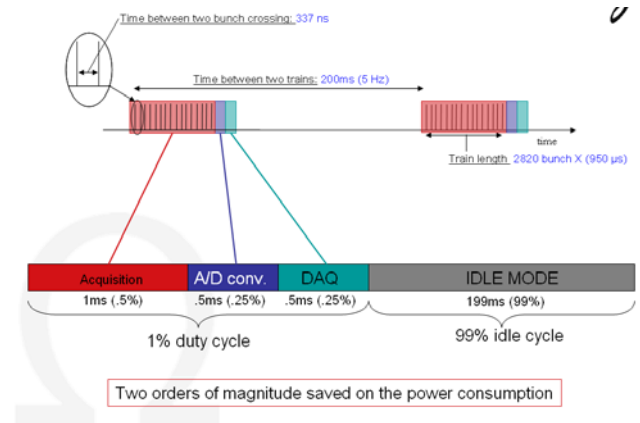

Fig. 1 – ILC beam structure and electronic sequence

Beyond the analogue core improvement, many features have been implemented in SKIROC. A channel by channel auto-trigger capability has been added allowing a built-in zero suppression. A multi-channel ADC is embedded. The trigger and gain selection threshold is set by an internal dual DAC. Voltage references used in the analogue core use a bandgap reference [2]. A digital core driving all the analogue features and the digital communication with the DAQ has been designed and is implemented in a FPGA to get debugged and improved before being embedded in the next version.
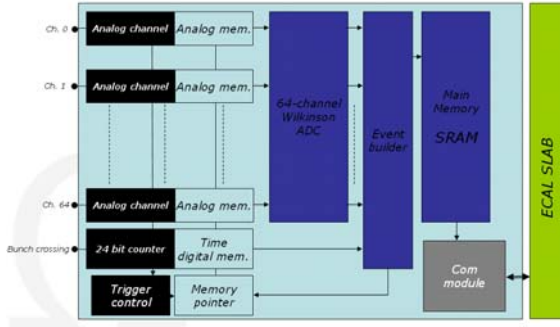
Fig. 2 – SKIROC block scheme

Fig 4 – One channel block diagram

That proceeding will describe the SKIROC chip and present results of the first prototype.

II – SKIROC DESCRIPTION

SKIROC is a 36-channel front-end chip designed to read-out silicon PIN diodes for calorimetry application. It has been designed in a general framework ensuring consistent back-end of different front-end ASIC for several calorimeters (HaRDROC to read out the digital RPC HCAL prototype and SPIROC to read out the SiPM and Sci tiles HCAL prototype are the two others chip existing on that framework)

Its main characteristics are the following:

- AMS SiGe 0.35µm technology
- 20mm² (4mm × 5mm) area
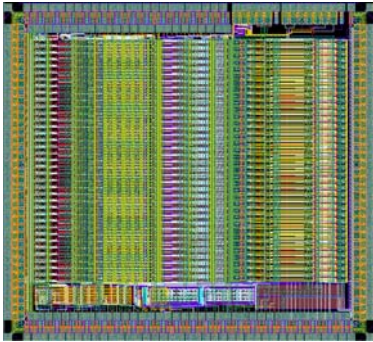- 3.3V power supply
- Package: CQFP240

Fig. 3 – SKIROC layout

Each channel is made of a variable-gain low-noise charge preamplifier followed by both a dual shaper – one with a gain 1 and the other with a gain 10 - to filter the charge measurement and a trigger chain composed of a high gain fast shaper and a discriminator. The measured charge is stored in a 5-depth SCA that can be read either in an analogue way or can be connected to a multi-channel 12 bit Wilkinson ADC. Thresholds are set with a 10-bit DAC for trigger level and for automatic gain selection level. A bandgap ensures the stability versus supply voltage and

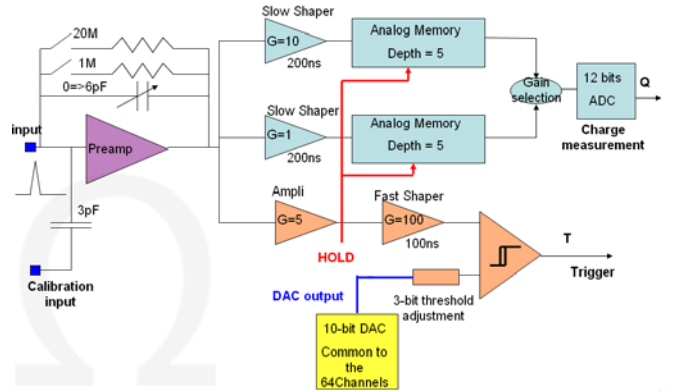temperature for all the requested reference in the analogue core.

The digital signals requested for digital and analogue block communications are outputted using a dynamic multiplexing to reduce the pin count while emulating the digital core in a FPGA.

III – SKIROC MEASUREMENTS

The analogue core of SKIROC has been extensively measured to validate the performance to achieve calorimetric measurement. The pedestal dispersion on the 36 channels is 1.8mV RMS for gain 1 and 2.1 mV for gain 10. These results fit well the statistic dispersion calculated from technology parameters according to transistor size and architecture. That result shows that the layout is correct and does not add neither additional dispersion nor pedestal pattern over the 36 channel. Results on that measurement are shown on Fig. 5.
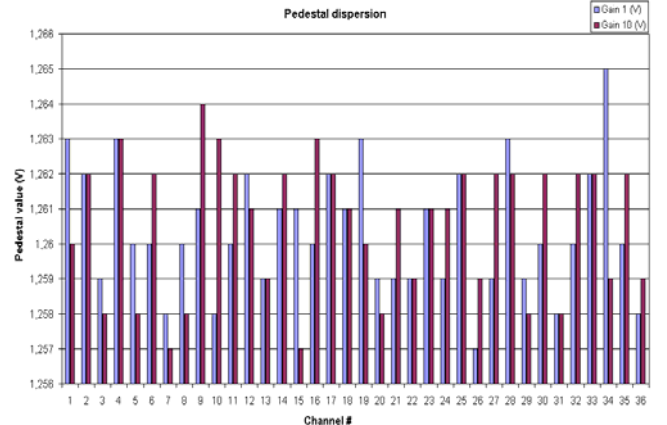

Fig 5 – SKIROC pedestals

The linearity on SKIROC has been measured and fit well the simulation. Due to minor bug in the internal ADC and in the probe bus that allows to check the linearity in an analogue way by probing the output of the slow shaper, it is not possible to extend the measurement to the whole dynamic range. These two bugs are corrected in the next iteration of SKIROC. The linearity is measured ion the two first third of the dynamic range to better than 0.5%. Measurement of that

linearity is shown on Fig. 6 and includes simulation, analogue measurement and digital measurement using the internal 12 bit multichannel Wilkinson ADC.
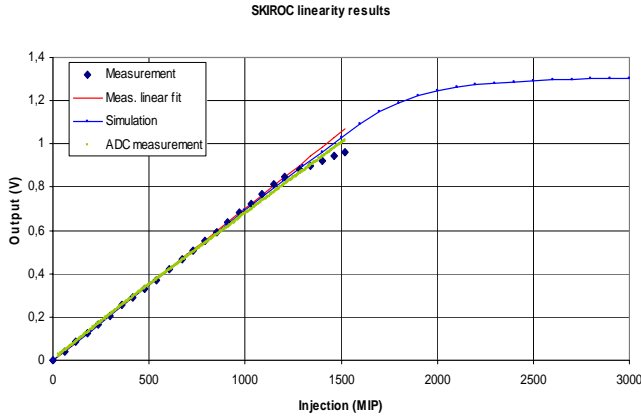

Fig 6 – SKIROC Linearity

The noise and channel dispersion has been measured through the whole acquisition chain including analogue channel, track and hold and internal Wilkinson ADC. These results are shown in Fig. 7 to 9. These results show that the internal does not add significant noise compared to the analogue measurement and validate therefore the use of an internal ADC in terms of noise and digital to analogue coupling.
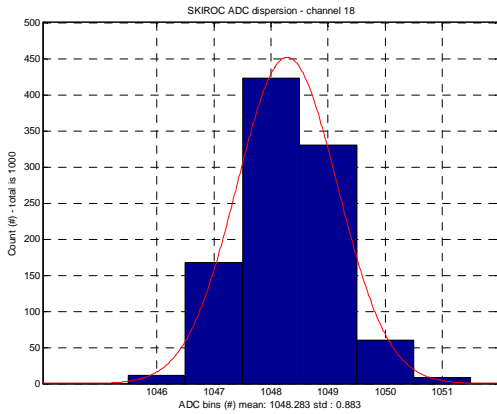

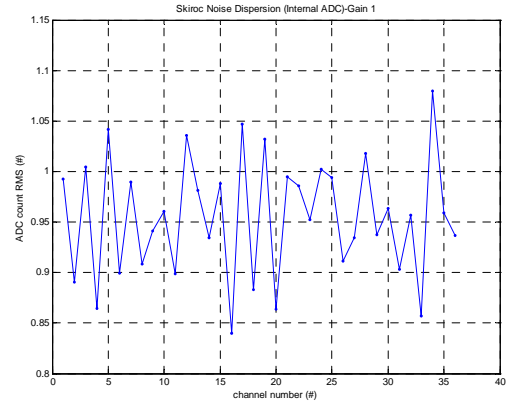Fig 7 – Channel noise, Gain 1

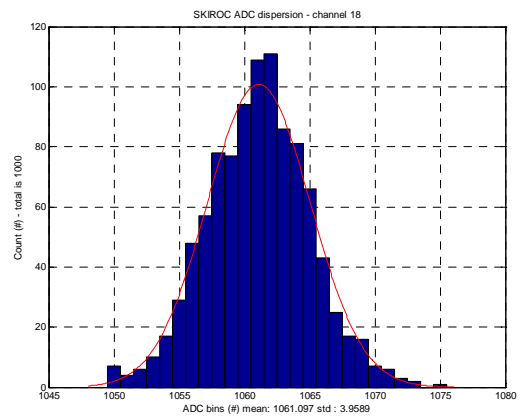

Fig 8 – Channel dispersion, Gain 1
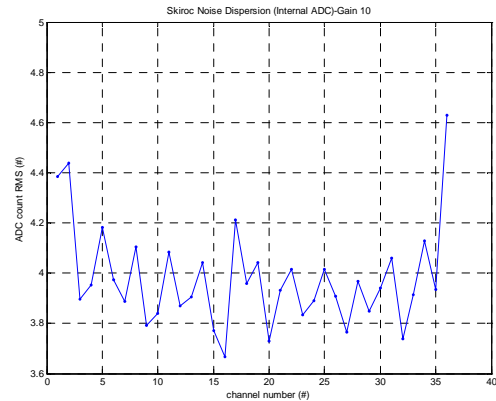

Fig 9 – Channel noise, Gain 10

Fig 10 – Channel dispersion, Gain 10

The equivalent noise charge of the preamplifier is measured around 2000 electrons. After shaping, the simulated MIP to noise ratio is 16 for the trigger line and 11 for the charge measurement. The measurement done on these points shows some non-expected Gaussian noise on both charge measurement and trigger line. The MIP to noise ratio drops to 8 for the charge measurement while it is not well characterized for the trigger path. Crosstalk is around the per mil level in simulation and in measurement.

The bandgap characterization made on a building block shows a 10ppm/°C drift ensuring the stability of the pedestal with temperature. The stability of the voltage reference with power supply is ensured for supply included within 2.8V to 3.8V for a nominal value of 3.3V. A bug in SKIROC Bandgap power pulsing degrades these performances, it has been corrected for the next iteration.

The DAC performances are within expectation by showing a 'static ENOB' of 9.5 bit for a 10 bit DAC. These two internal DAC allows to tune the trigger threshold and the automatic gain selection value.
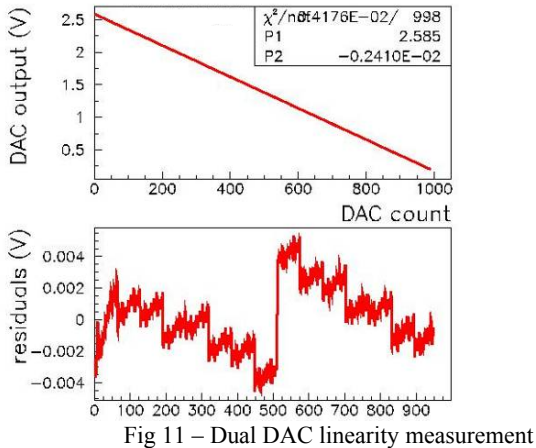

Fig 11 – Dual DAC linearity measurement

SKIROC is announced for march 2009 and will embed many of SKIROC1 blocks that has been validated by the above measurements.

IV – CONCLUSION

The SKIROC chips will be used to equip the 40,000-channel ECAL foreseen for 2009 that will validate the technological choices for the 82-million-channel final detector. Many of the final detector requested features have been embedded and the performance has been greatly improved compared to the physics prototype front-end chip. The production of that ASIC is foreseen in summer 2008 to be able to take data in 2009, before the engineering design report of the final detector planned for 2010 by the ILC Worldwide Study Bureau.

V – REFERENCES

[1] TESLA Technical design report
http://tesla.desy.de/new_pages/TDR_CD/start.htm

[2] Acknowldgement to Fabrice Voisin – Bandgap reference – IN2P3 Microelectronic school. Designer of the bandgap used in SKIROC