SKIROC

The last prototype of a front-end chip for silicon pin diode read-out dedicated to the Si-W ECAL for ILC

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Introduction

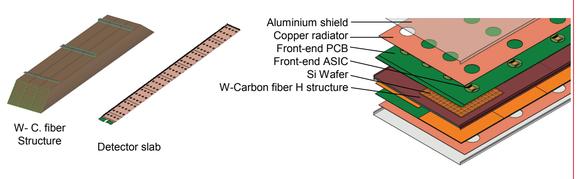
SKIROC (standing for Silicon Kalorimeter Integrated read-Out Chip) has been designed to read out the upcoming W-Si electromagnetic calorimeter technologic prototype. That new generation calorimeter is developed by the Calice collaboration and the EUDET European research program. The aim of that prototype is to validate the feasibility of a full-scale high-granularity ECAL for the international linear collider. Expectations on the front-end electronics are cutting edge to achieve the required integration, compacity and uniformity of calorimetric measurement on **82 millions of channels**.

-**Compacity, integration :** It is necessary for such a high number of channel to have the front-end electronic as close as possible to the detector to minimize the lines and cables that introduce noise through a parasitic capacitance. The feasibility of the calorimeter is involved by the ability to embed the front-end ASIC inside the calorimeter. Meanwhile, the dead material shall be minimized and a cooling system inside the calorimeter would degrade the physics performance. It is therefore necessary to achieve a ultra-low power consumption to avoid active cooling. The ILC beam structure combined with a **power pulsing capability** implemented in the front-end ASIC allow to reach the beyond-state-of-the-art consumption of **25µW/channel** (including ADC and buffer to DAQ).

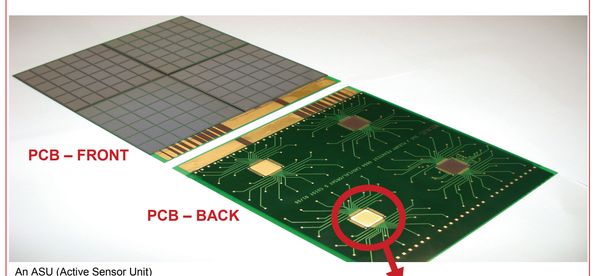
-**Number of channels, performances :** Calorimetric measurement requires a 15 bit resolution. The 12 bit wilkinson ADC combined with the dual shaper embedded in SKIROC ensure a **15.3 bit resolution**. To keep the data flow to the DAQ acceptable, a **zero-suppress** associated to an **internal trigger** has been included to convert and output only valid data (e.g. above an adjustable threshold). That channel by channel self trigger associated with the very low occupancy of the detector allow a data reduction of 10^4 making the data rate acceptable within the tight power budget.

Front-end PCB

The technologic prototype :
- A tungsten-carbon fiber structure
- Detector slabs, hosting silicon wafer and front-end electronic slid in the structure

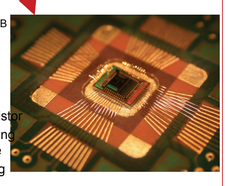


The ASU (Active Sensor Unit) :
- Each detector slab is composed of several Active Sensor Unit (ASU) stitched together
- An ASU is a ultra-thin PCB hosting Si Wafers on one side and VFE electronic on the other

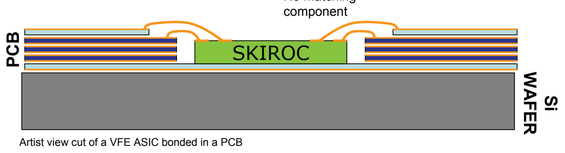


An ASU (Active Sensor Unit)

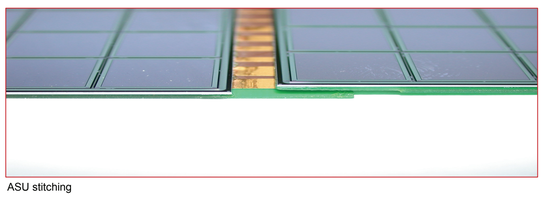
VFE ASIC bonded in a PCB



To ensure such a high integration, the VFE ASIC :
- Run autonomously
- Don't need external component
  - No bias resistor
  - No decoupling capacitance
  - No matching component



Artist view cut of a VFE ASIC bonded in a PCB

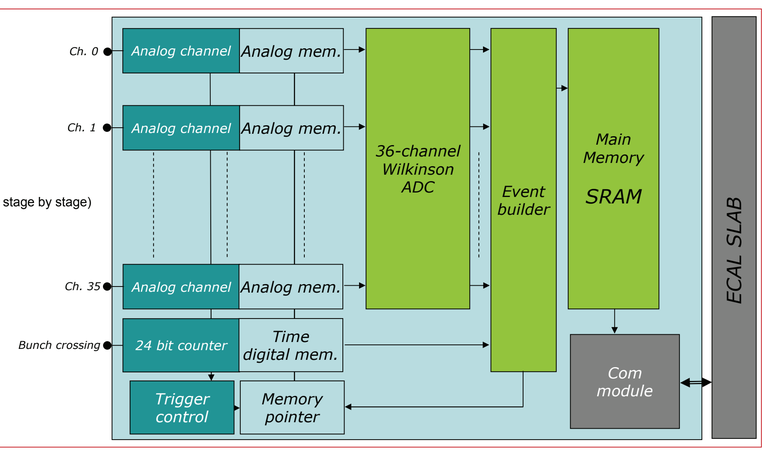


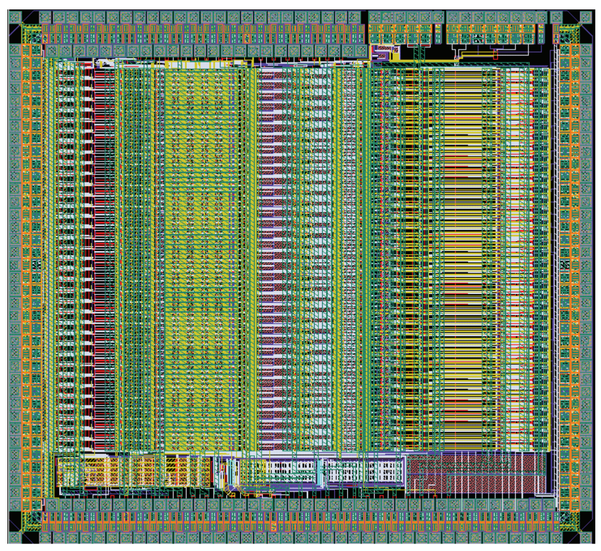
ASU stitching

Characteristics

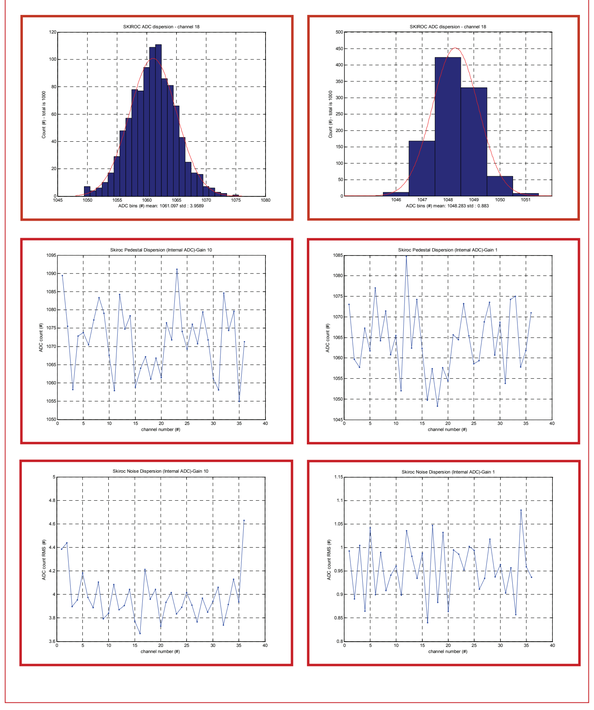
- Designed for 5*5 mm² pads
- 36 channels
- Detector AC/DC coupled
- Auto-trigger
  - MIP/noise ratio on trigger channel : 16
- 2 gains / 12 bit ADC → 2000 MIP
  - MIP/noise ratio : 11
  - Power pulsing (Programmable stage by stage)
- Calibration injection capacitance
- Embedded bandgap for references
- Embedded DAC for trig threshold
- Compatible with physics proto DAQ
  - Serial analogue output
  - External "force trigger"
- Probe bus for debug
- 24 bits Bunch Crossing ID*
- SRAM with data formatting*
- Output & control with daisy-chain*

*digital part are implemented in a FPGA in the first version of the ASIC



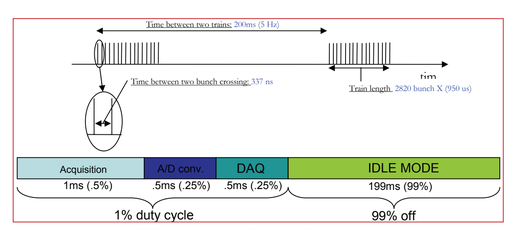


ADC performance



System behaviour

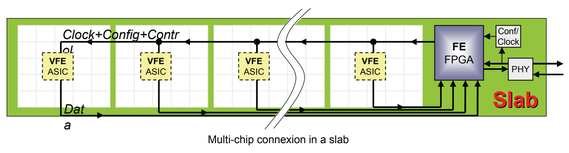
The system on chip has been designed to fit the ILC beam structure. The valid data are stored in each front-end chip during the beam train. The data are then converted in digital and sent to DAQ during the inter-train. When all these operations are done, the chip goes to idle mode to save power.



ILC beam structure and front-end chip operating mode

Acquisition	A/D conversion	DAQ
When an event occur : •Charge is stored in analogue memory •Time is stored in digital (Bunch crossing ID) memory •Trigger is automatically rearmed at next bunch crossing ID Depht of memory is 5 and will be extended to 16 in next version	The data (charge) stored in the analogue memory are sequentially converted in digital and stored in a SRAM. An event in RAM is : •The Bunch Crossing ID •The charge •The shaper gain •The status of the trigger	The events stored in the RAM are outputted through a serial link when the chip gets the token allowing the data transmission. When the transmission is done, the token is transferred to the next chip. 256 chips can be read out through one serial link

Front-end chip operating mode description

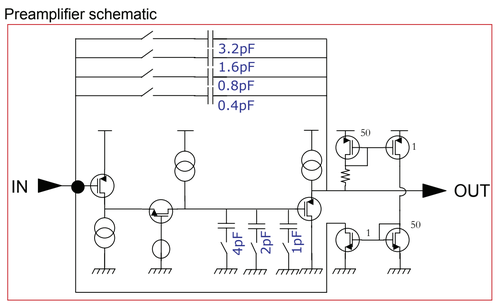


Multi-chip connexion in a slab

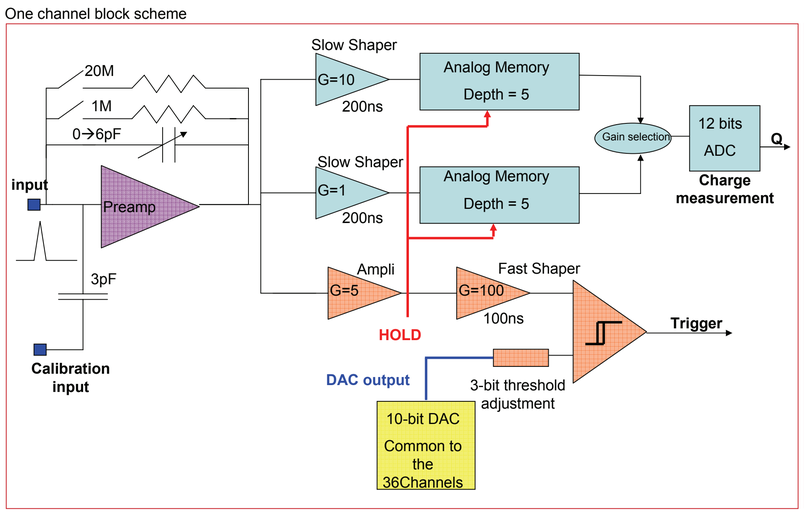
Analogue channel

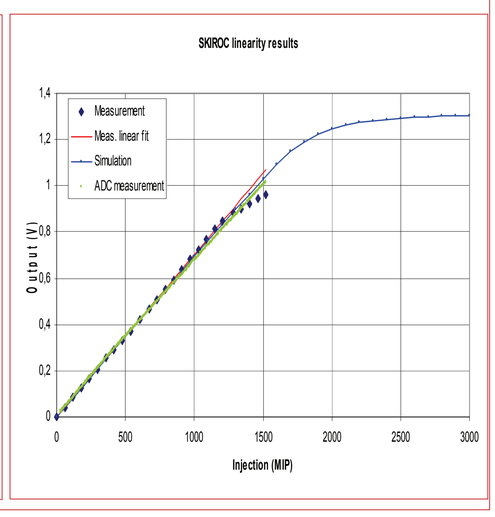
- Low noise – variable gain charge preamplifier
- Slow control selectable calibration injection capacitance
- High gain fast shaper + discriminator for trigger line
- Dual shaper and SCA for charge measurement
- 12 bit wilkinson ADC
- 10 bit DAC for trigger threshold adjustment

Preamplifier schematic



One channel block scheme





LAL and Omega

LAL (*Laboratoire de l'accélérateur linéaire*) is a physics laboratory in Orsay (France), 20 km south from Paris. 350 people including around 100 physicists work on many experiment in cosmology, high energy particle physics and accelerator. Several technology group such as the mechanic or the electronic group work on applications to achieve physicist expectations.

The LAL electronic group (50 people) is divided in 3 units : system unit, microelectronic unit, and test unit. Teams are involved in many big physics experiments such as Atlas, Planck, Auger and ILC. The group can work on project from the manufacturing standard to the production and ensure maintenance.

The microelectronic team has acquired a sharp knowledge in full-custom analog ASIC design. Its specialization is focused on low-noise high-speed front-end chip and on high-precision calibration devices. Its know-how is evolving to system-on-chip designs that embed front-end electronic, auto-trigger system, calibration devices and digital converter.

IN2P3 (Nuclear and particle physics French institute) has recently asked for a rationalization of engineering resources in microelectronic and is building competence poles. Omega is the pilot structure. 10 engineers are currently in the Omega team, ensuring the R&D of several complex chip per year to serve particle physics.

http://omega.in2p3.fr

Orsay MicroElectronics Group Associated