IN2P3

CSNSM LAL LPNHE IPN Orsay

Omega

SPIROC : Silicon PM Readout ASIC

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IN2P3/OMEGA-LAL Orsay

CALICE Calorimeter for ILC

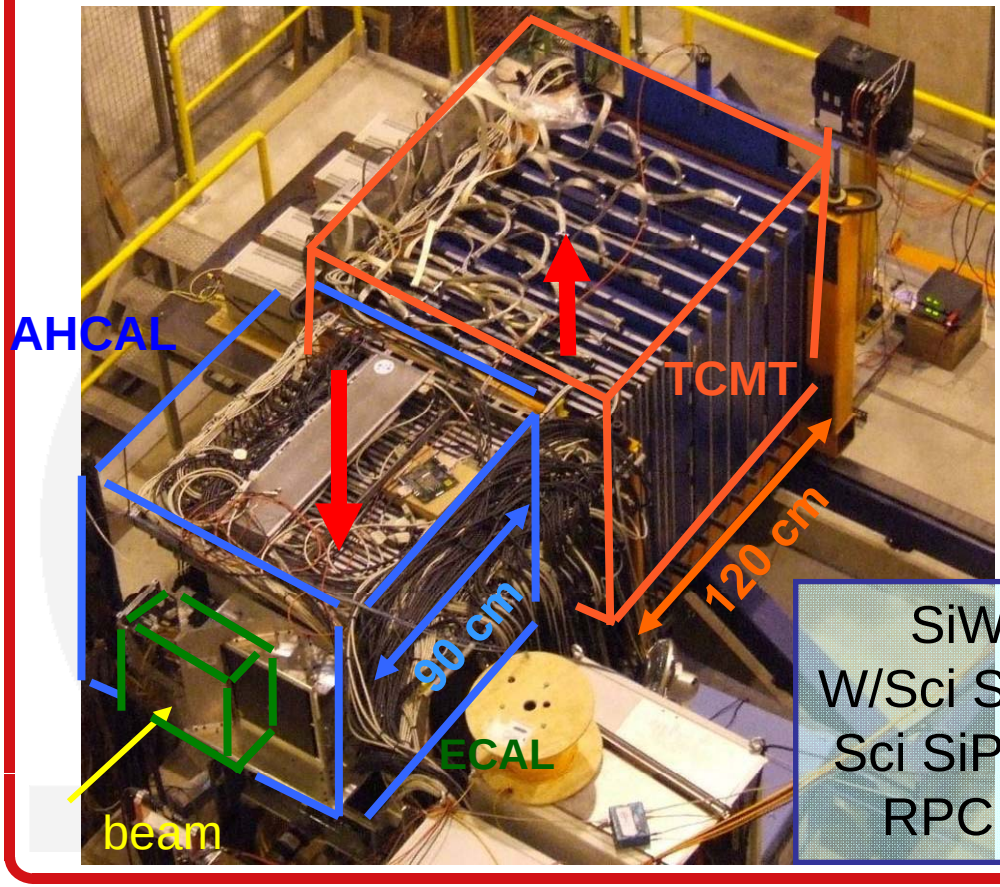
EUDET

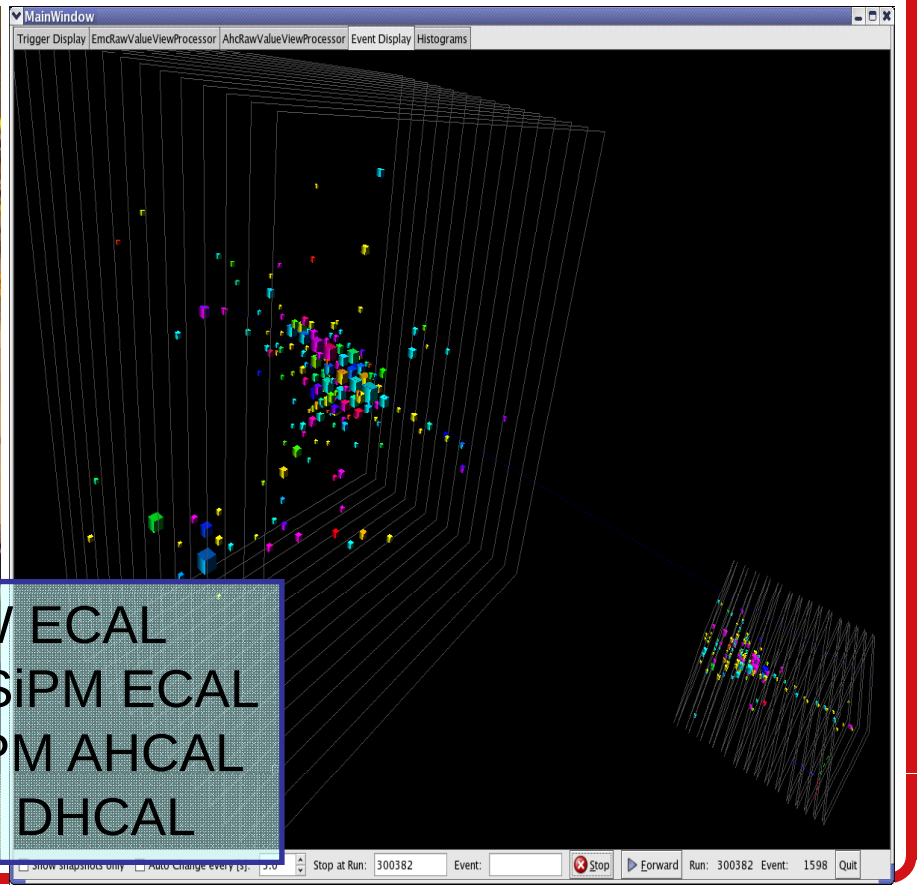
Orsay MicroElectronics Group Associated

CALICE : imaging calorimetry

- After LHC : New imaging calorimetry...at the ILC
- Improve jets measurement by Particle flow algorithm
- CALICE : 281 phys., 47 labs, 12 countries.

Chairperson : JC Brient http:///llr.in2p3.fr/activites/physique/flc/calice.htm

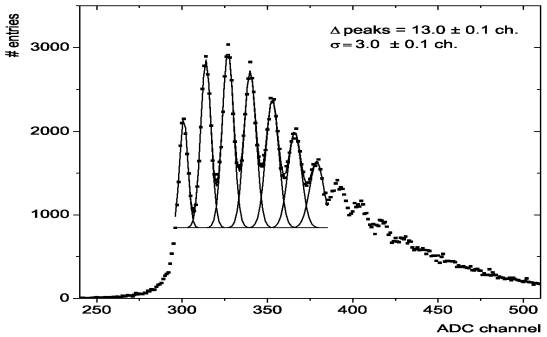


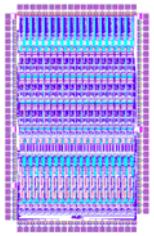


SiW ECAL
W/Sci SiPM ECAL
Sci SiPM AHCAL
RPC DHCAL

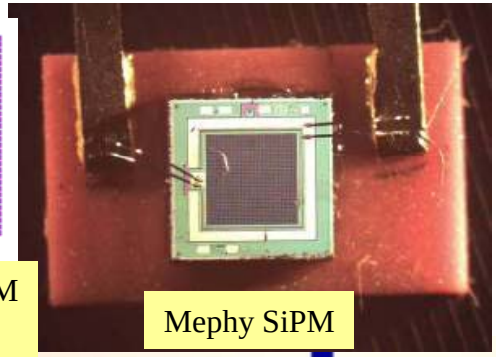
CALICE AHCAL testbeam prototype

- Hadronic calorimeter prototype for the ILC : 1 cubic metre, 38 layers, 2cm steel plates
- 8000 tiles with SiPMs fabricated by MePHY group

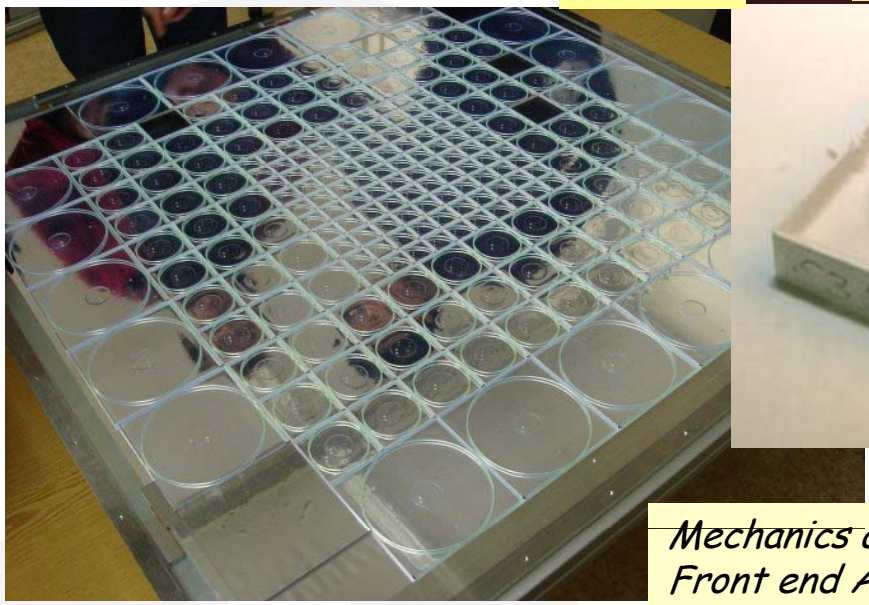


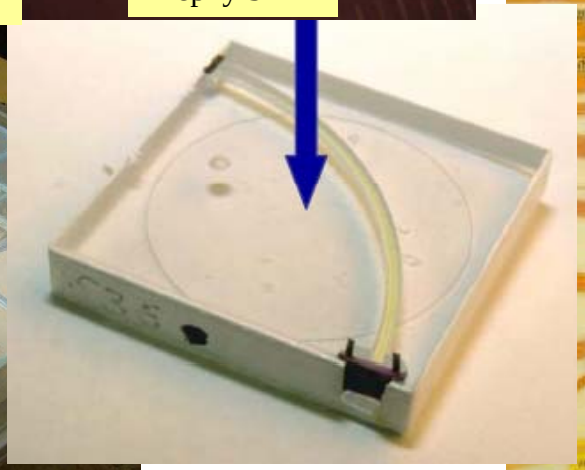


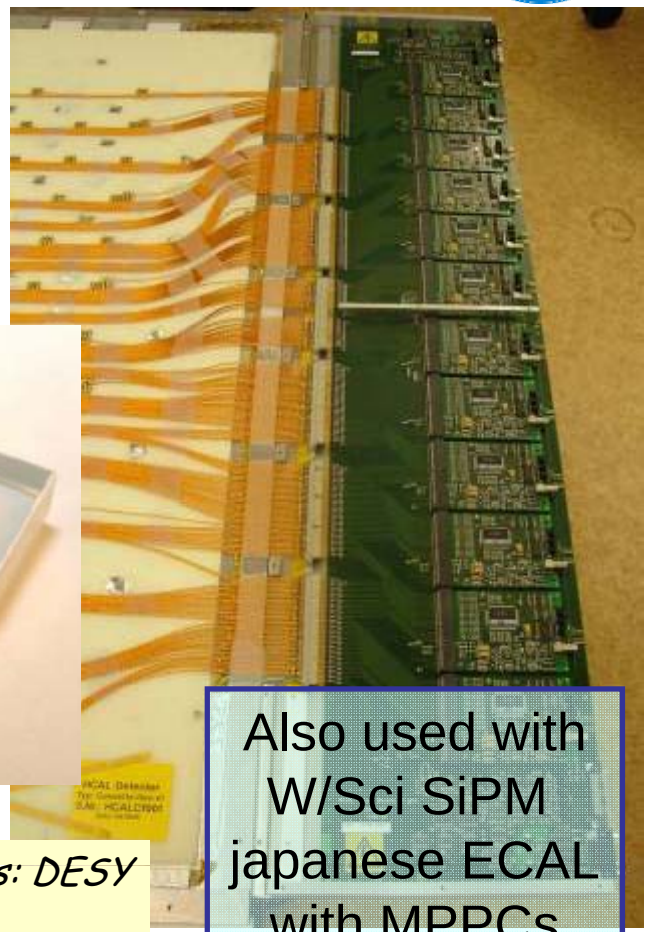
FLC_SiPM ASIC



Mephy SiPM



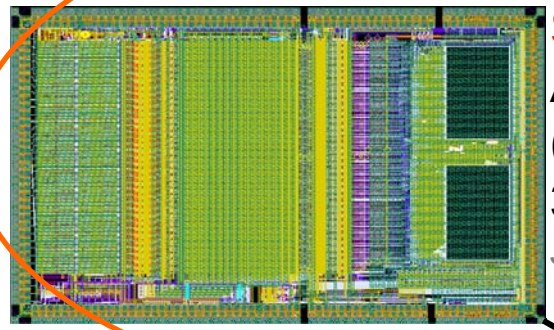




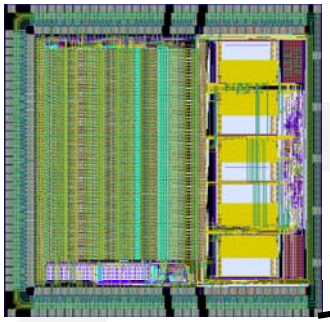
Mechanics and front end boards: DESY
Front end ASICs: LAL

Also used with W/Sci SiPM japanese ECAL with MPPCs

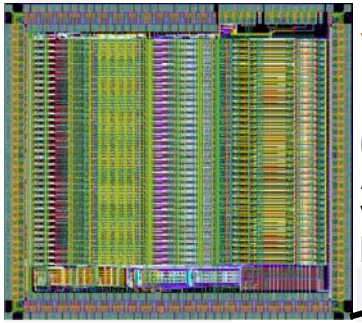
The front-end ASICs : the ROC chips



SPIROC
Analog HCAL
(SiPM)
36 ch. 32mm²
June 07

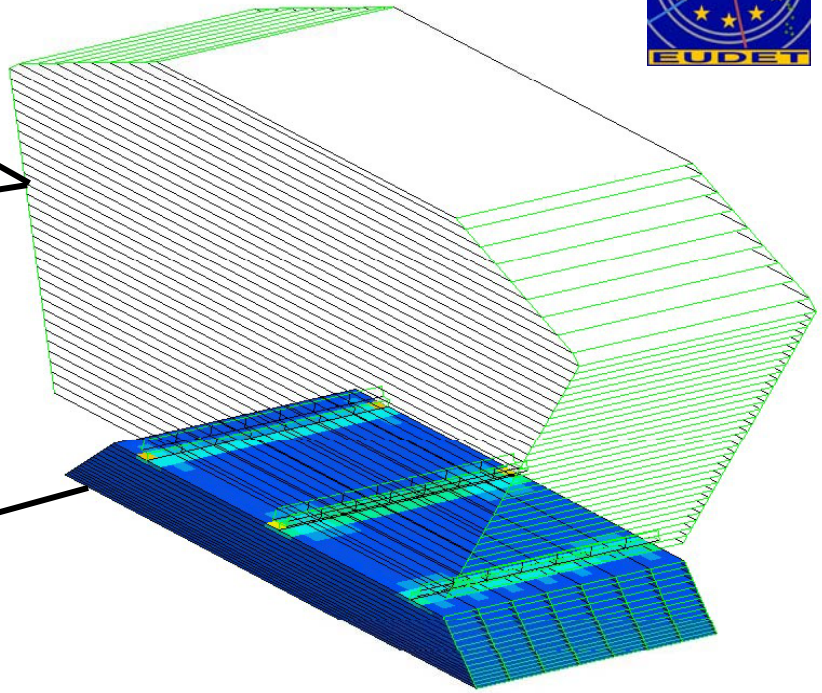


HARDROC
Digital HCAL
(RPC, µmegas or GEMs)
64 ch. 16mm²
Sept 06

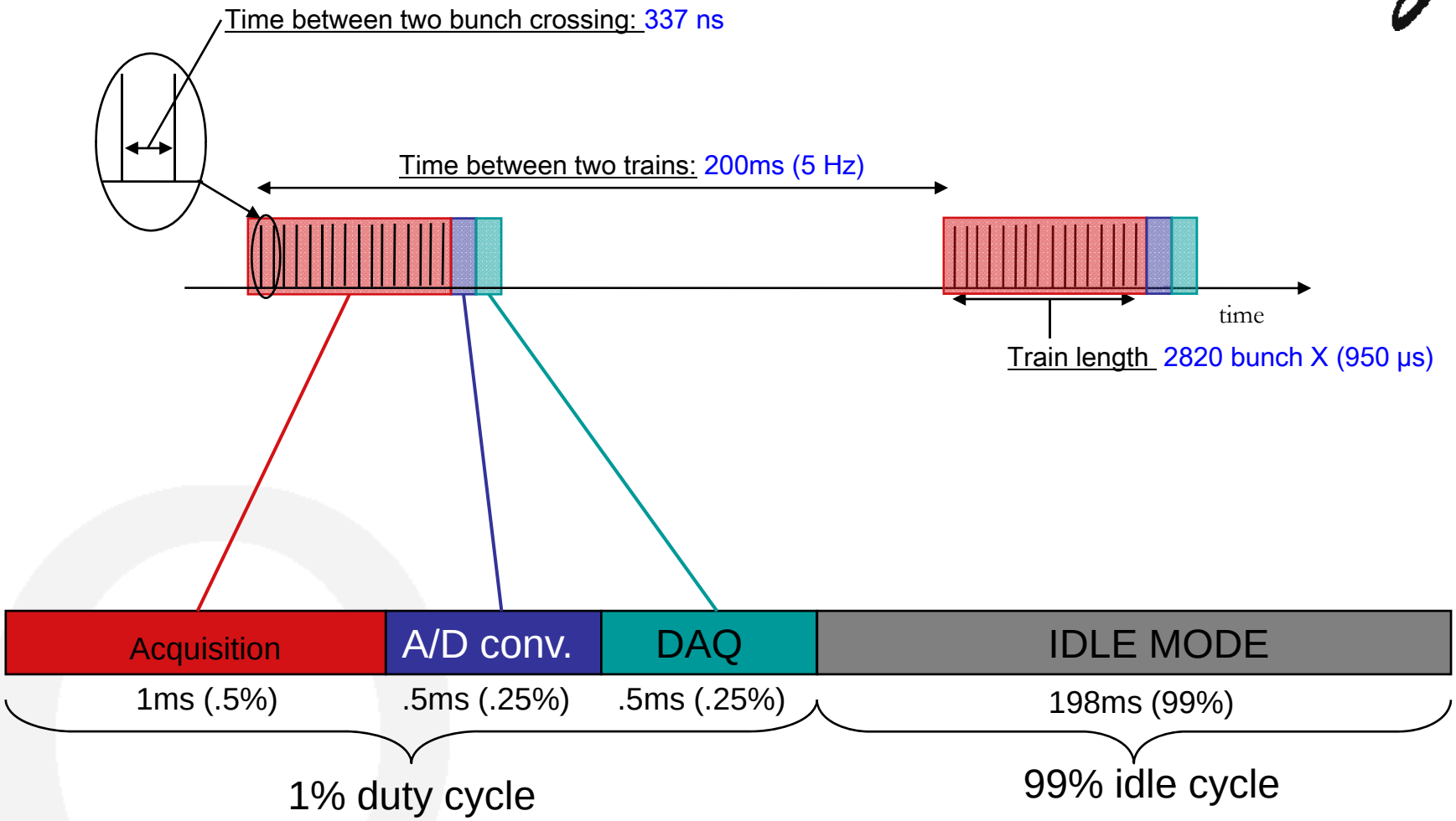


SKIROC
ECAL
(Si PIN diode)
36 ch. 20mm²
Nov 06

- Technological prototypes : full scale modules (~2m)
- EUDET EU funding (06-09)
- ECAL, AHCAL, DHCAL
- B=5T

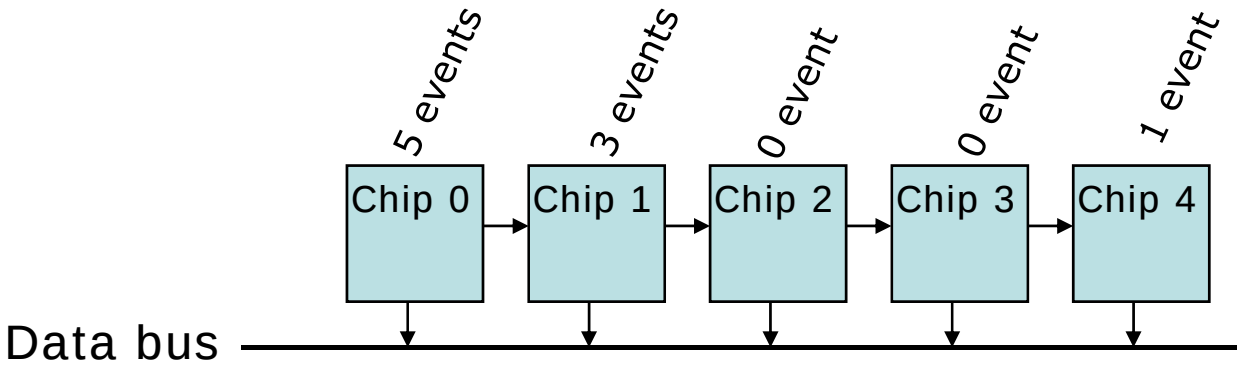


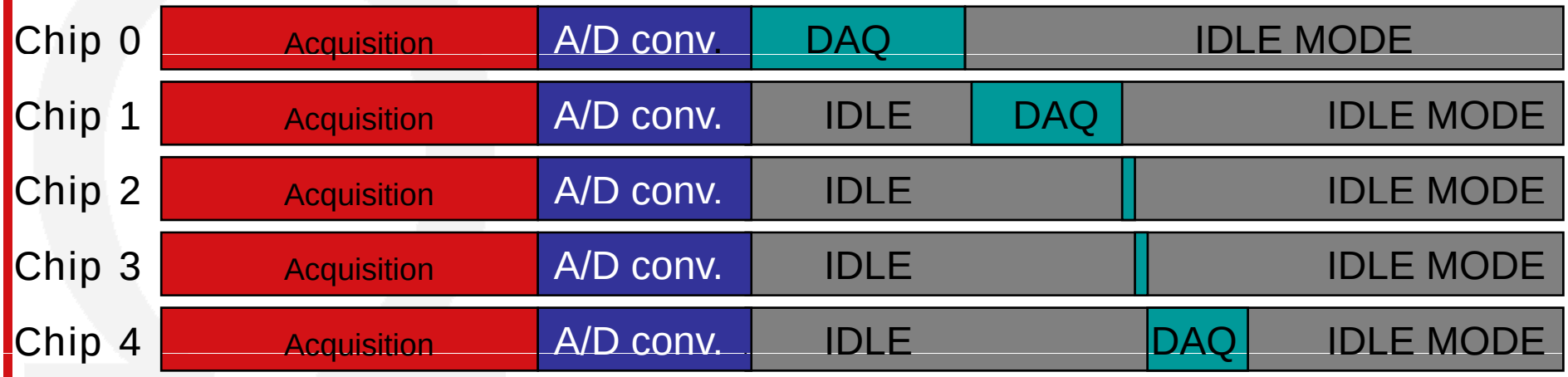
ILC beam structure



Two orders of magnitude saved on the power consumption

Read out : token ring

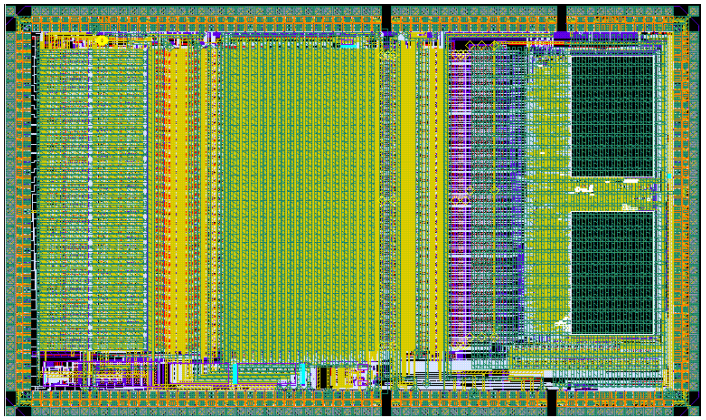


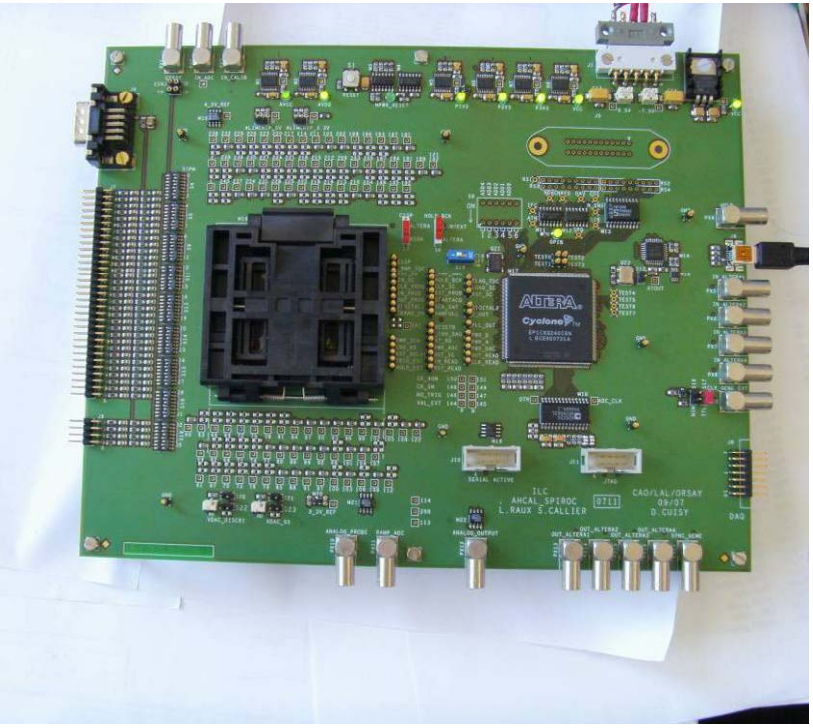


Second generation chip for SiPM

- SPIROC : Silicon Photomul. Integrated Readout Chip
  - 36 channels
  - Charge measurement
  - Time measurement
  - Autotrigger on MIP or spe
  - Sparsified readout compatible with EUDET 2nd generation DAQ
  - Chips daisy-chained
  - Pulsed power -> 25 µW/ch

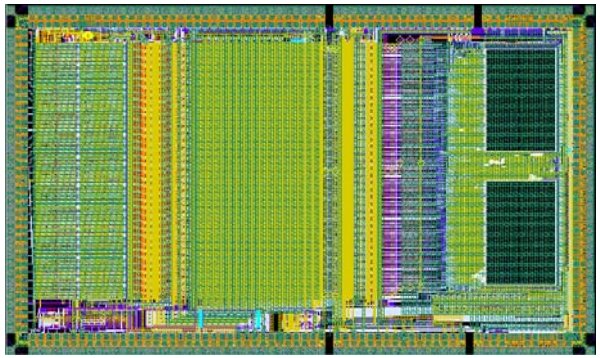
- Fabricated in SiGe AMS 0.35 µm
  - Submitted in june 07
  - Chip area : 30 mm2



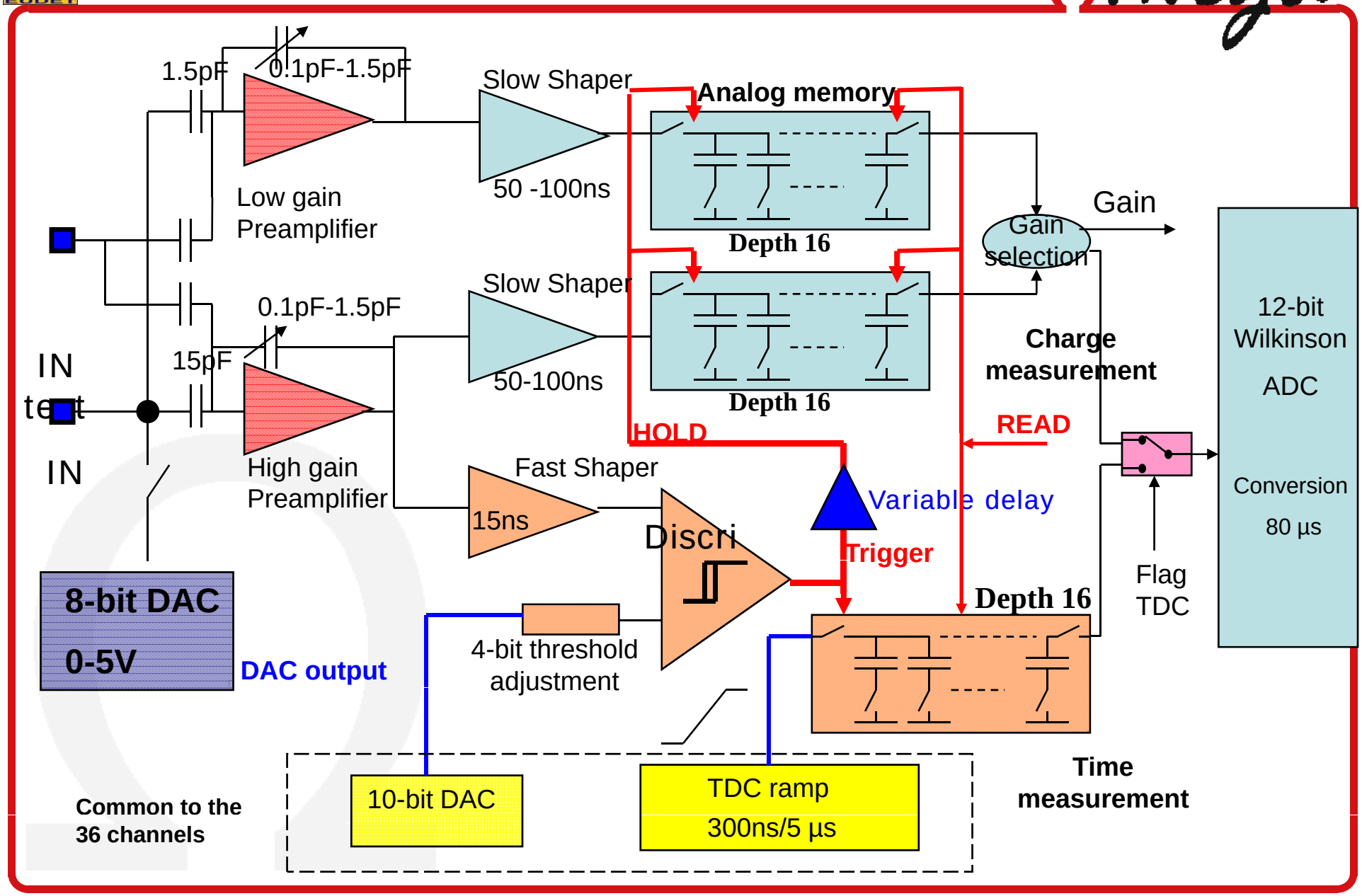


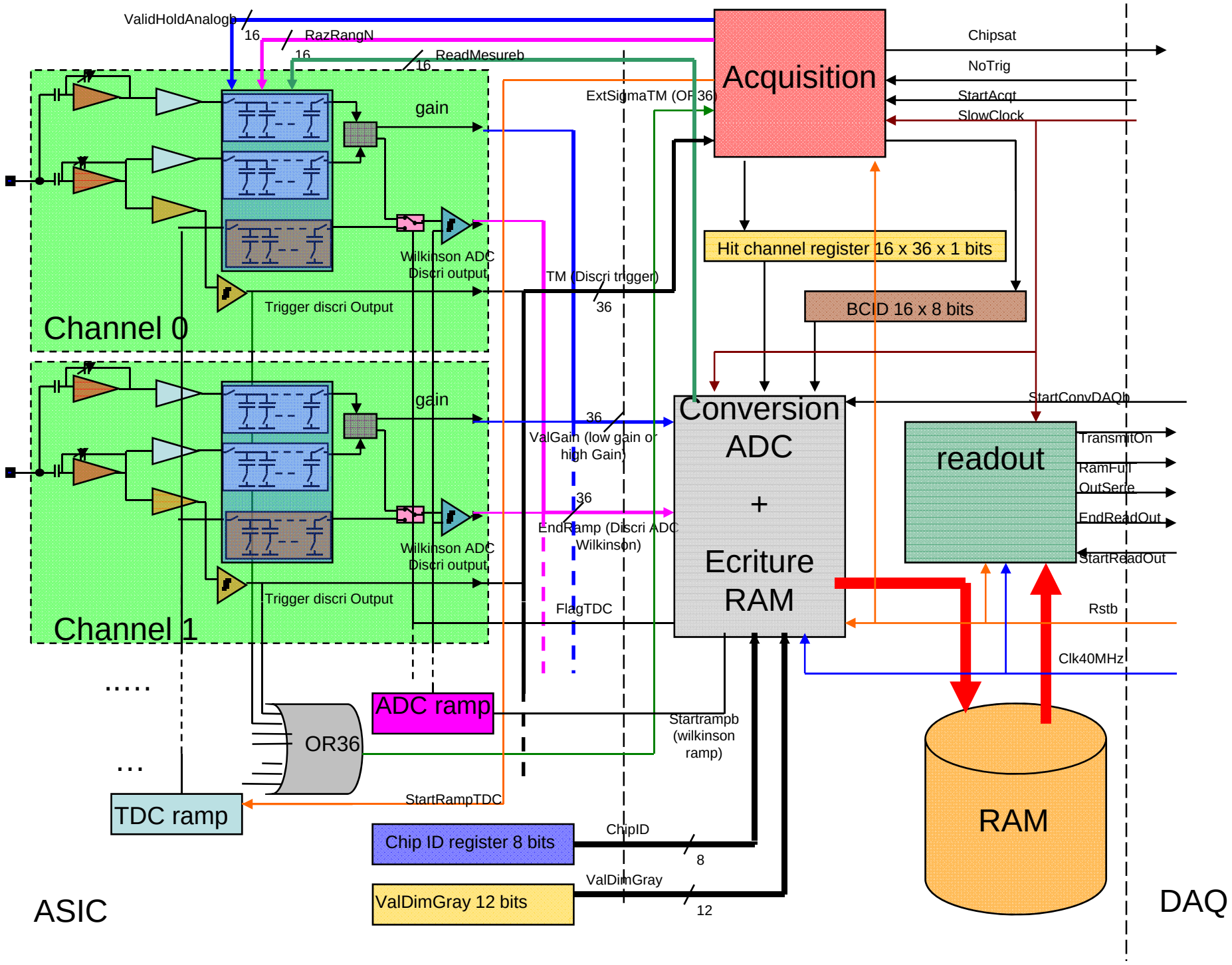
SPIROC main features

- Internal input 8-bit DAC (0-5V) for individual SiPM gain adjustment
- Energy measurement : 14 bits
  - 2 gains (1-10) + 12 bit ADC 1 pe → 2000 pe
  - Variable shaping time from 50ns to 100ns
  - pe/noise ratio : 11
- Auto-trigger on 1/3 pe (50fC)
  - pe/noise ratio on trigger channel : 24
  - Fast shaper : ~10ns
  - Auto-Trigger on ½ pe
- Time measurement :
  - 12-bit Bunch Crossing ID
  - 12 bit TDC step~100 ps
- Analog memory for time and charge measurement : depth = 16
- Low consumption : ~25µW per channel (in power pulsing mode)
- Individually addressable calibration injection capacitance
- Embedded bandgap for voltage references
- Embedded 10 bit DAC for trigger threshold and gain selection
- Multiplexed analog output for physics prototype DAQ
- 4k internal memory and Daisy chain readout

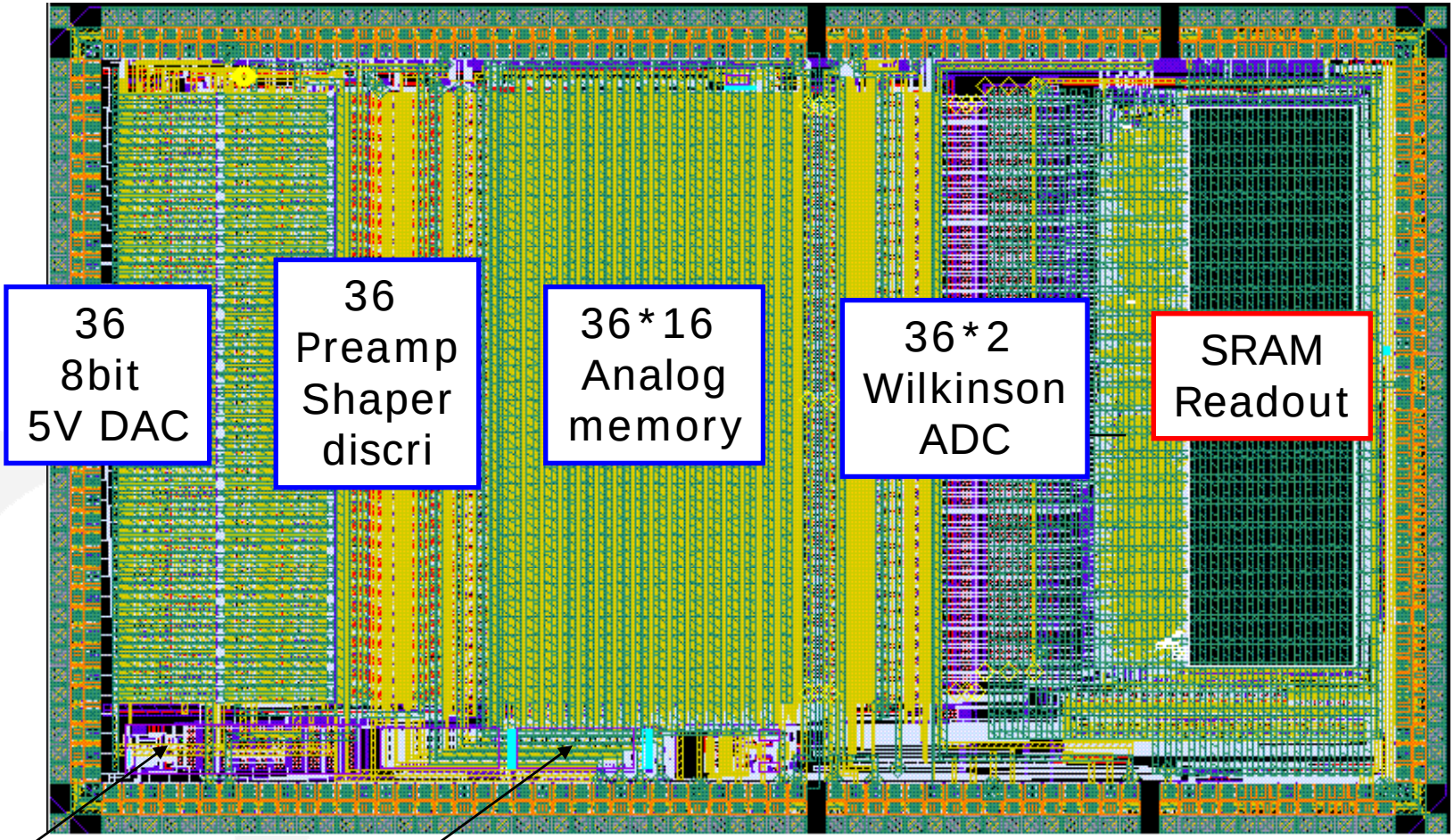


SPIROC : One channel schematic

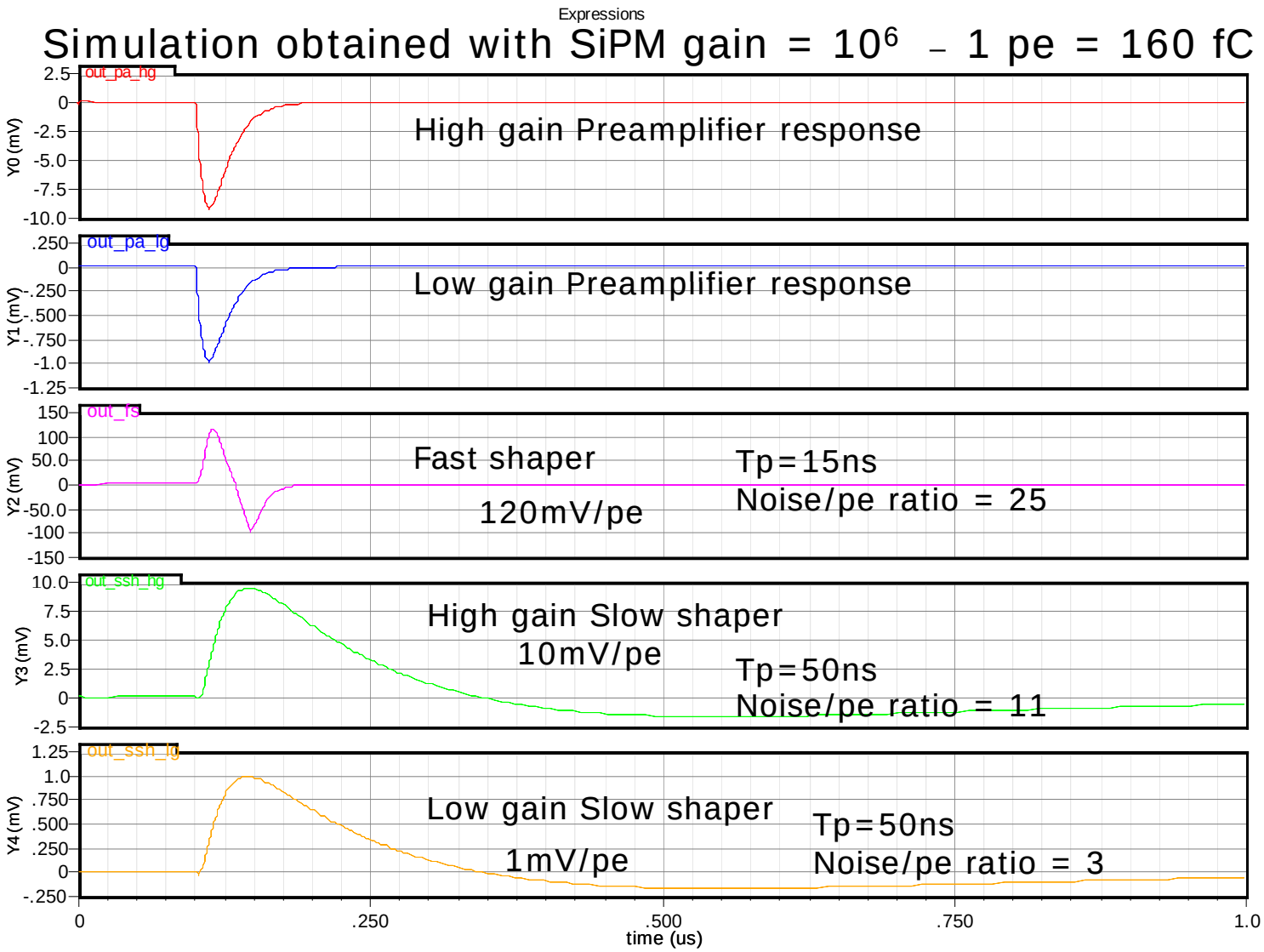



ValidHoldAnalogb
16
RazRangN
16
ReadMesureb
16
Acquisition
Chipsat
NoTrig
StartAcqt
SlowClock
ExtSigmaTM (OR36)
gain
Wilkinson ADC
Discri output
Trigger discri Output
Channel 0
TM (Discri trigger)
36
Hit channel register 16 x 36 x 1 bits
BCID 16 x 8 bits
gain
Wilkinson ADC
Discri output
Trigger discri Output
Channel 1
36
ValGain (low gain or high Gain)
36
EndRamp (Discri ADC Wilkinson)
FlagTDC
Conversion ADC
+
Ecriture RAM
StartConvDAQb
readout
TransmitOn
RamFull
OutSerie
EndReadOut
StartReadOut
Rstb
Clk40MHz
.....
...
OR36
ADC ramp
Startrampb (wilkinson ramp)
TDC ramp
StartRampTDC
Chip ID register 8 bits
ChipID
8
ValDimGray
ValDimGray 12 bits
12
RAM
ASIC
DAQ

SPIROC layout

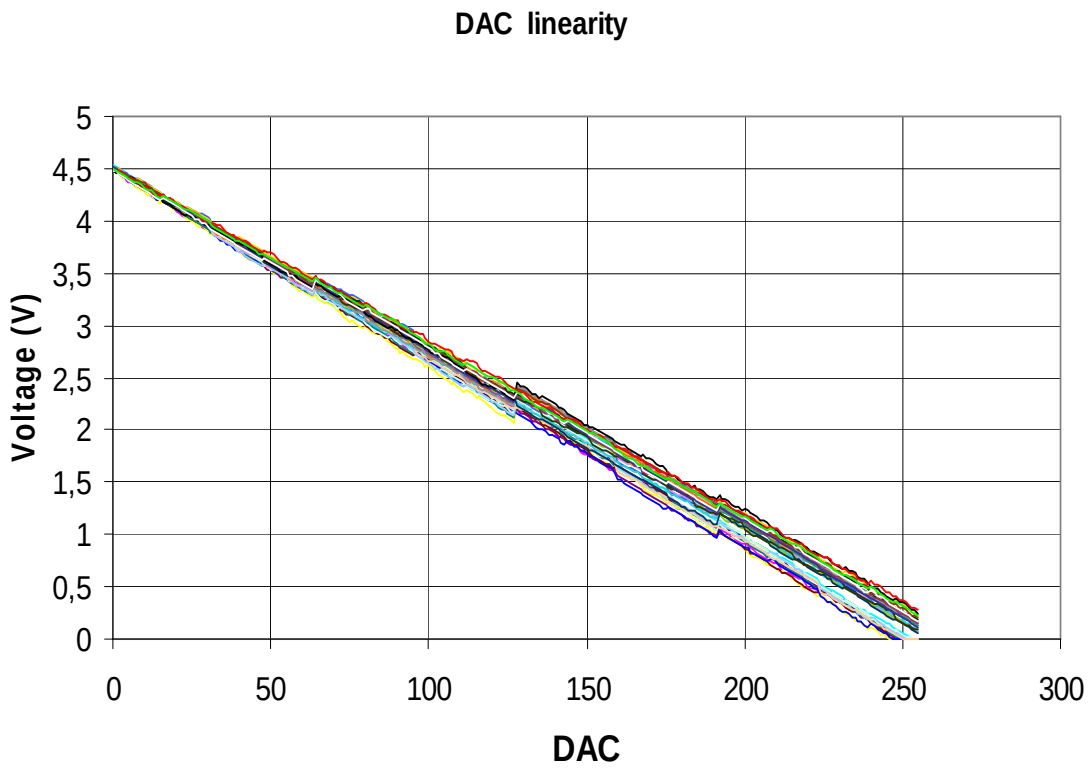


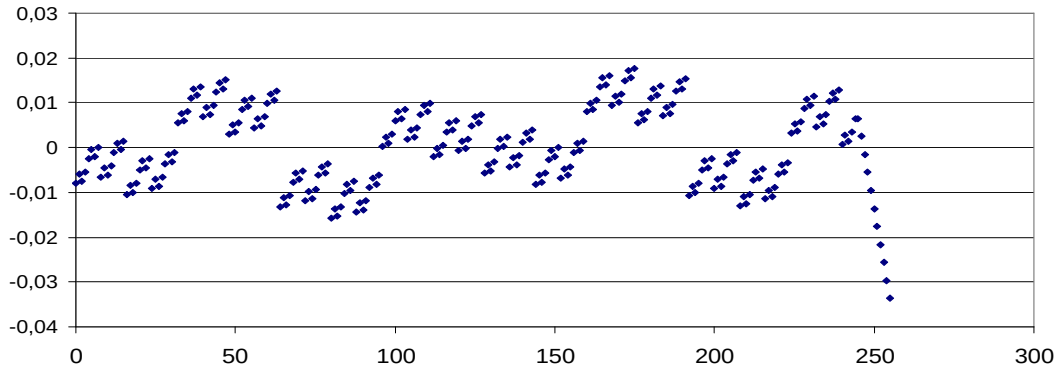
Simulated waveforms



Input DAC

- 8 bit, 5V range
- LSB=20mV
- 36 DACs : one per channel
- Ultra low power (1µW) : no power pulsing
- Can sink 10 µA leakage current
- Linearity : ± 2%

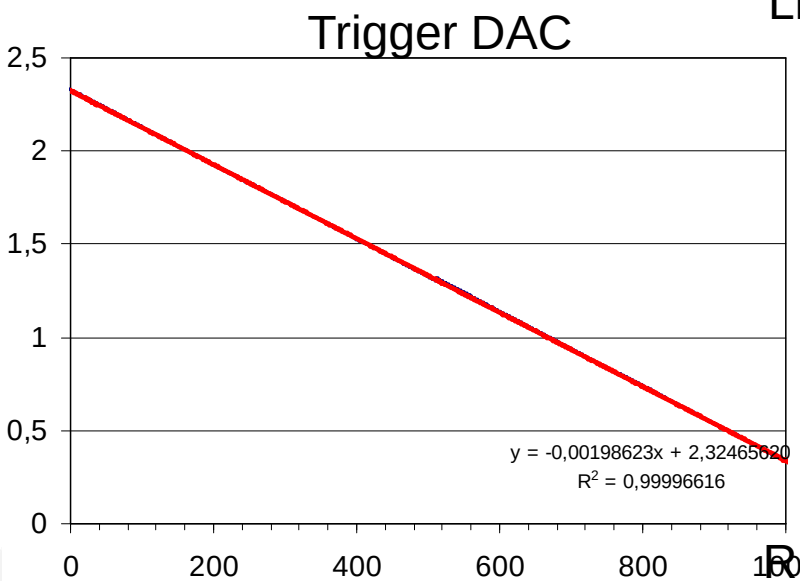


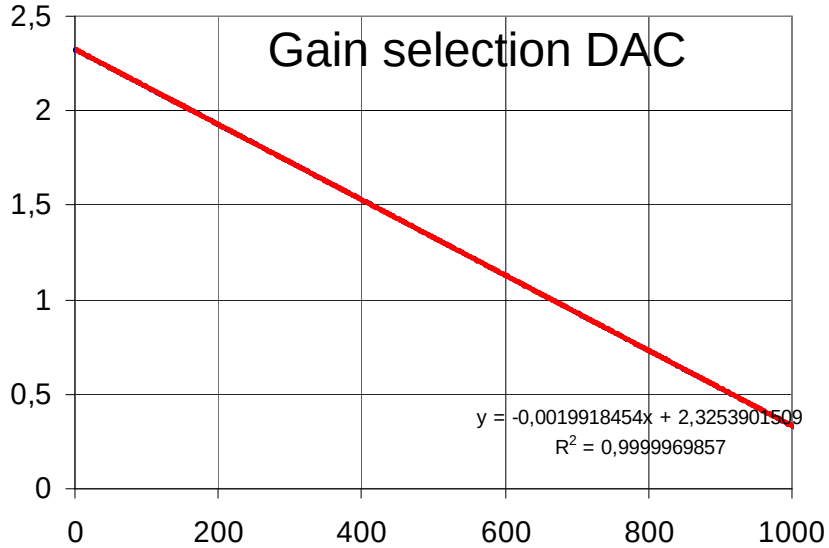


Trigger and gain select DAC meas.

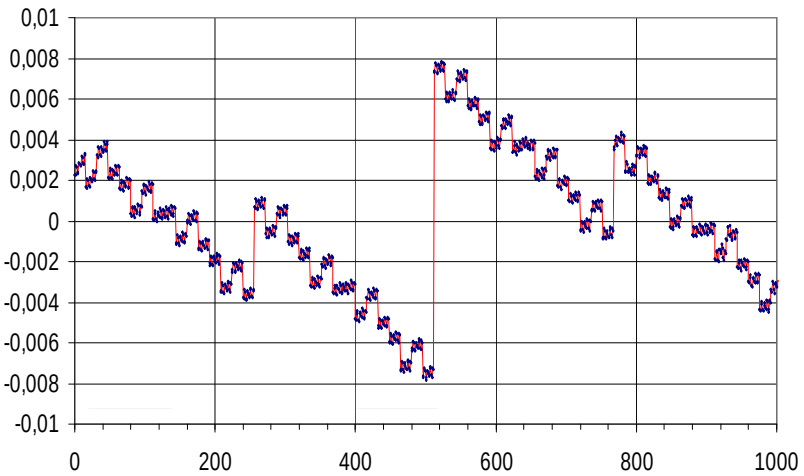
- Linearity : typ ±0.2%

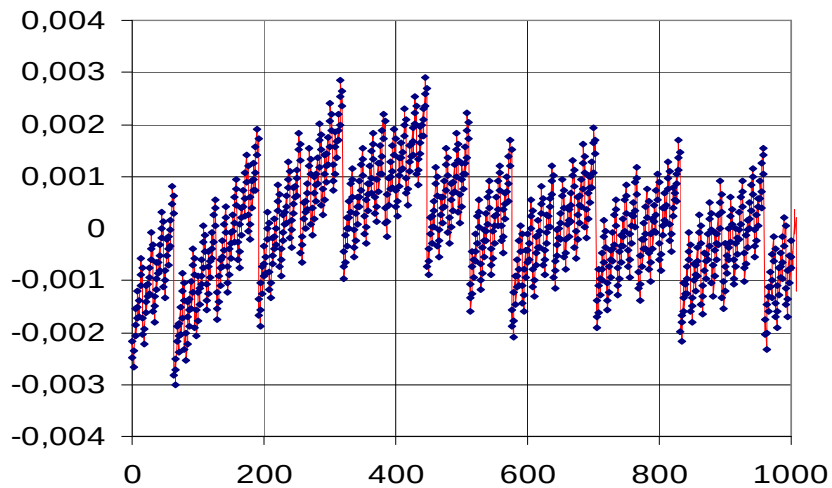
Linearit





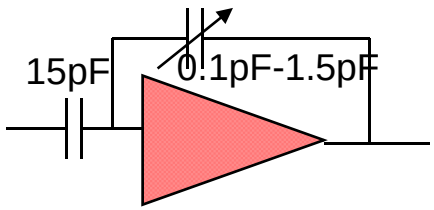
Residua



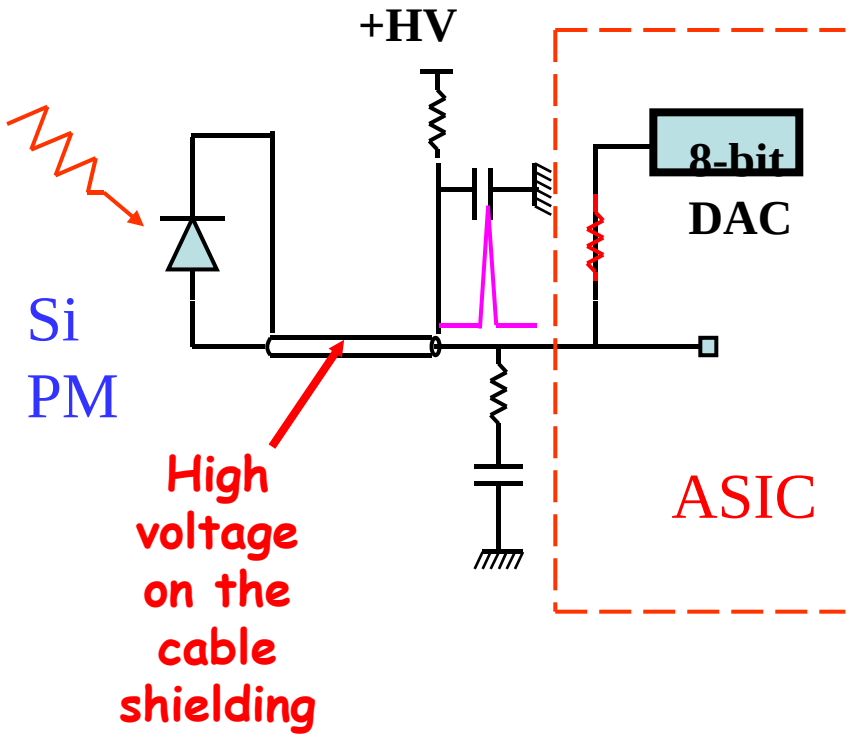


Input preamp

- Bi-gain low noise preamp
  - Reused from SKIROC
  - Low noise charge preamp capacitively coupled = voltage preamp
  - Gain adjustable with 4 bits common to all preamps : Cf=0.2, 0.4, 0.8, 1.6 pF
  - Positive input pulse
  - 8 mV/pe in HI Gain
  - Noise : 1.4 nV/sqrt(Hz)
  - Power : 2 mW (unpulsed)



- Low gain at preamp level
  - 1.5pF coupling capacitor
  - 0.8 mV/pe, MAX : 2000 pe (300pC)



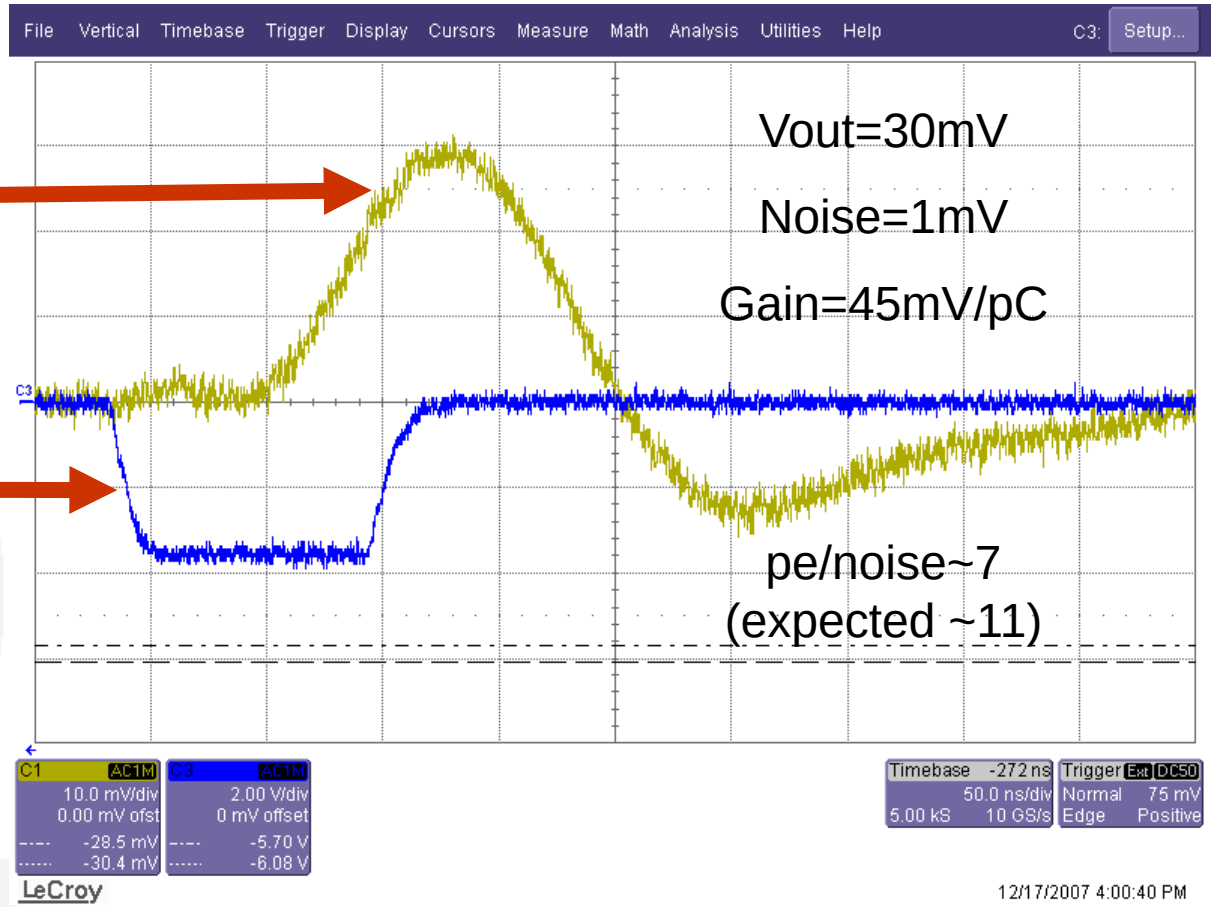
Analog waveforms

High gain channel output

680fC (~4 pe @SiPM gain=$10^{6)}$ in SPIROC

Charge measurement

Auto trigger



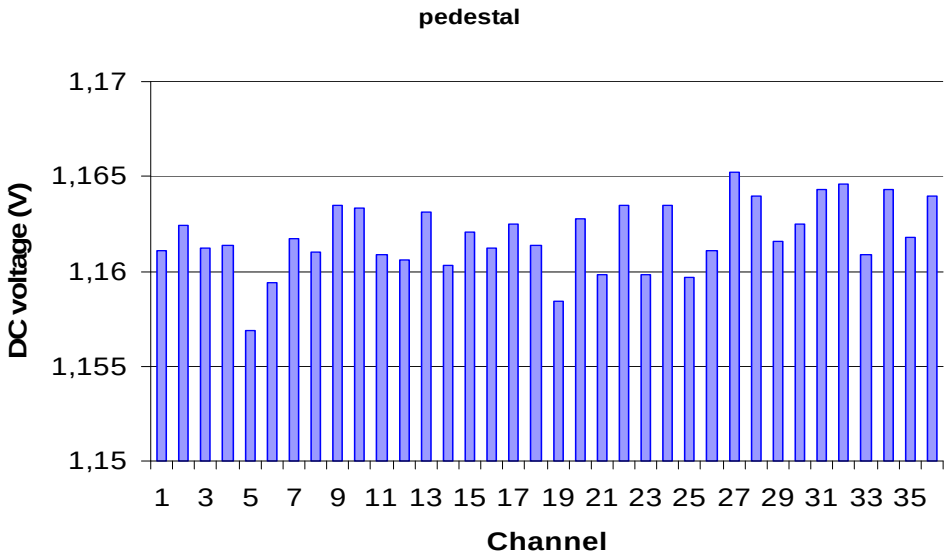
Set up:

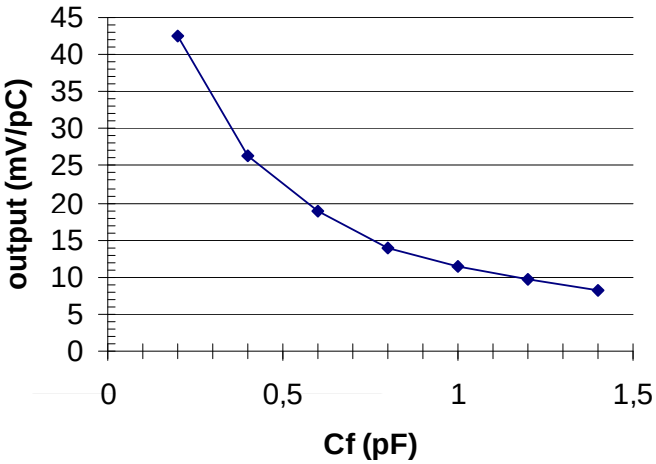
Cf=400fF

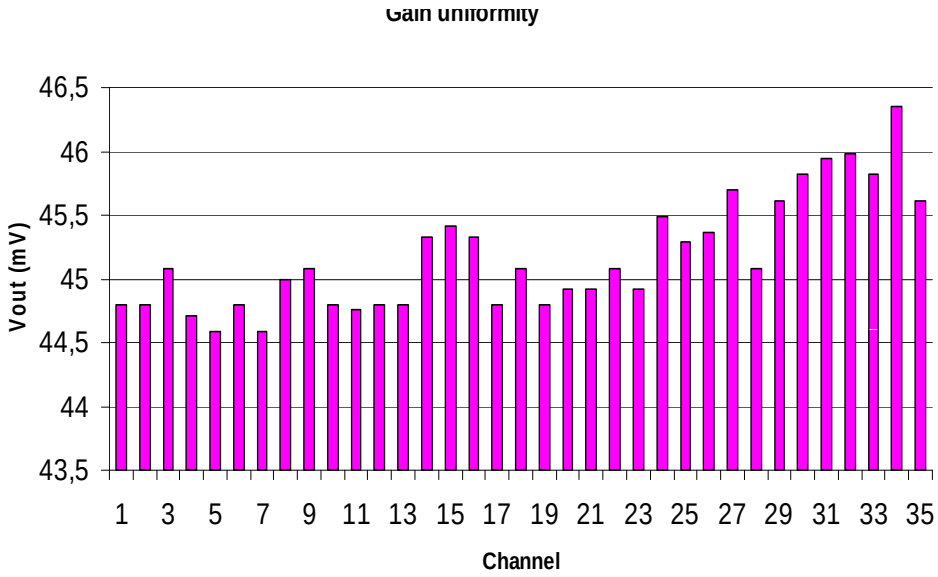
Tau=50ns

Gain uniformity

- Pedestal uniformity
  - Avg = 1.16V
  - Rms = 1.8 mV
- Gain uniformity
  - Rms 1%
  - 45 mV/pC (Cf=0.2pF tau=50ns)
- Noise : ~ 1mV

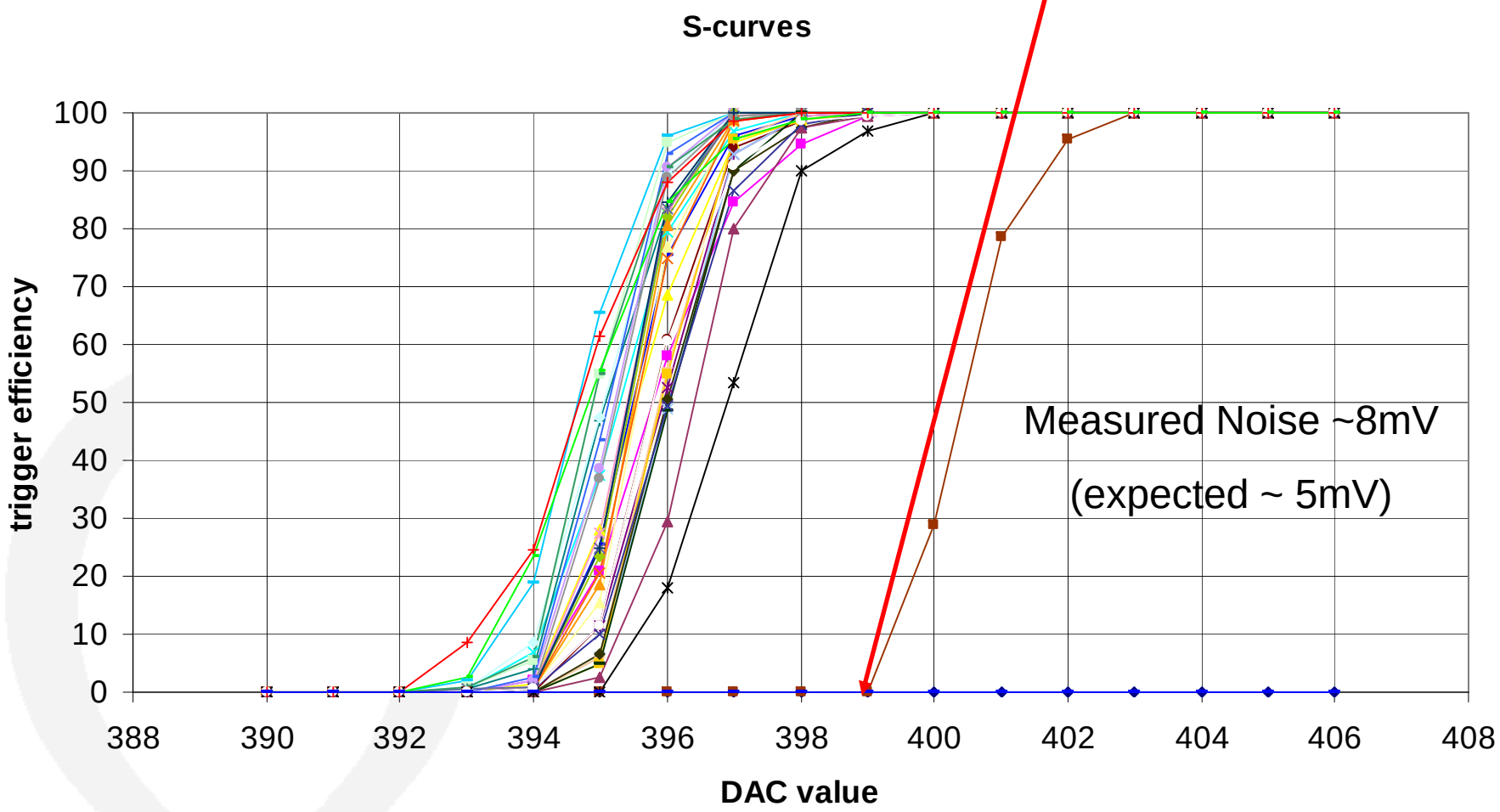




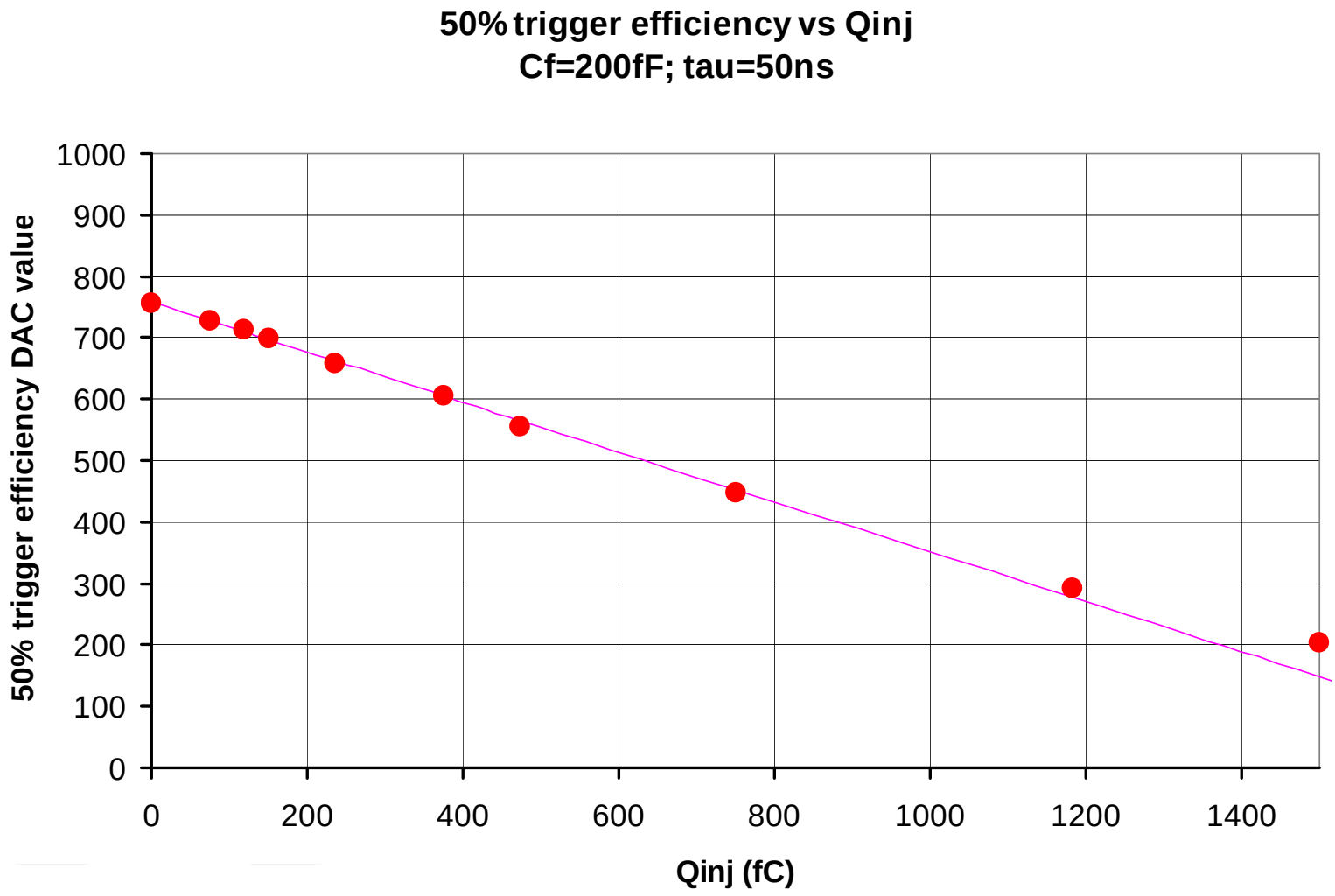


S-curves

- Trigger efficiency versus Threshold (1UDAC=2mV)



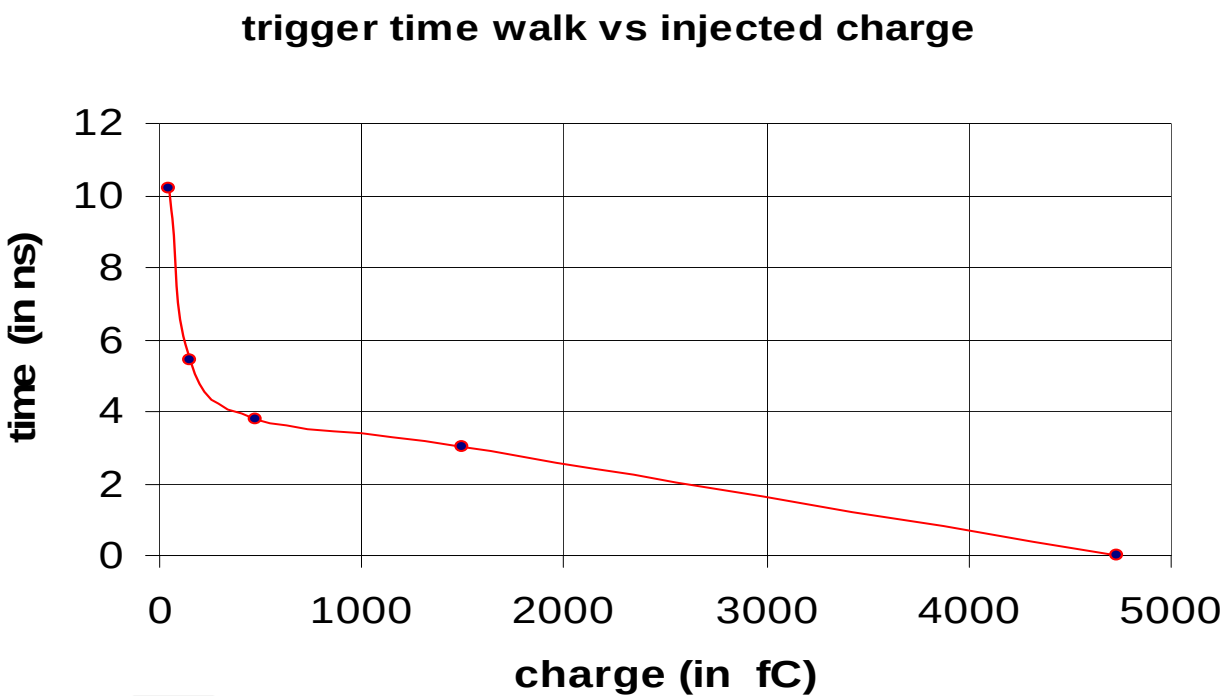
Trigger linearity



Crosstalk and trigger time walk

- Very low Cross-Talk : 0.3% (long distance cross talk due to slow shaper voltage reference: If this voltage decoupled with 100µF, it becomes negligible ~0.04%)

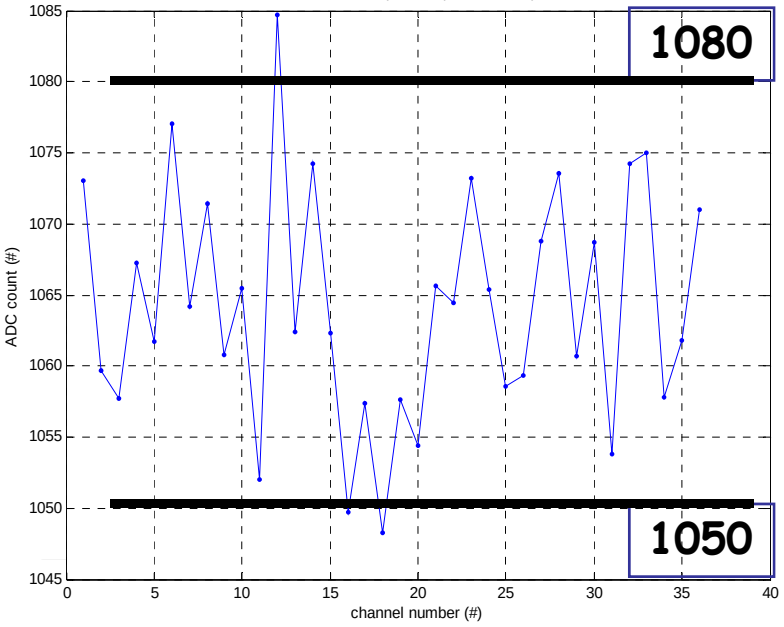
- Trigger time walk: ~10ns



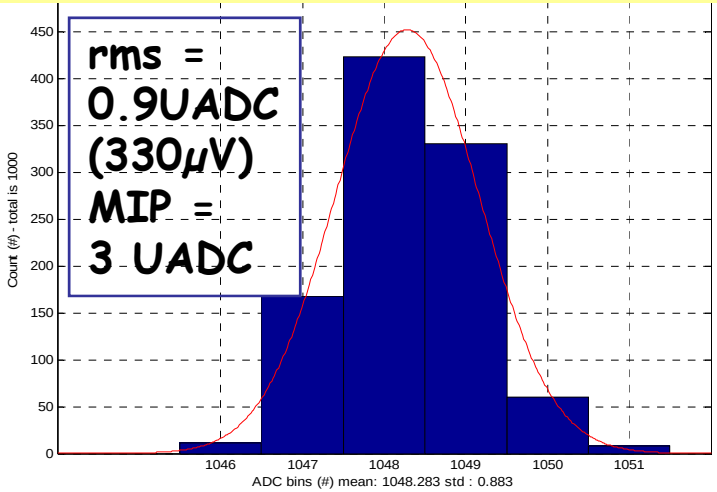
12 bit Wilkinson ADC performance

- (stupid) bug in internal ADC : cannot be tested
- Similar to ADC in sister chip SKIROC
- 1 ADC/channel 12 bits 80µs
- Fixed in SPIROC2

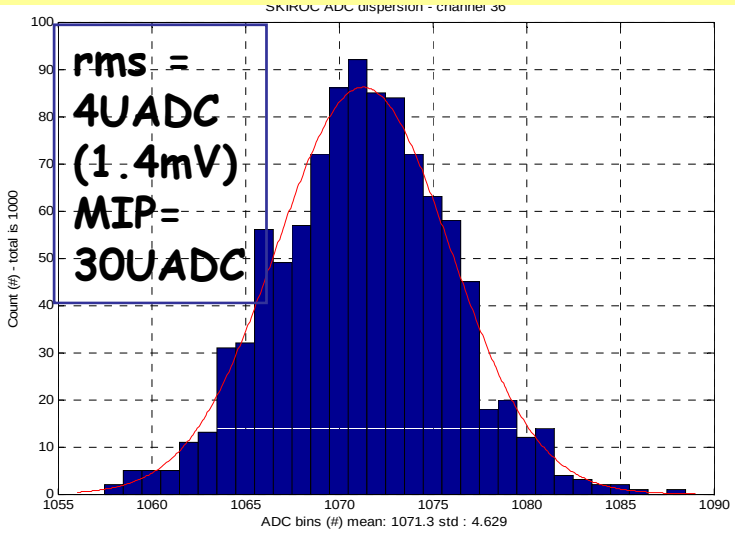
Pedestal value vs Channel number



Noise in low gain shaper

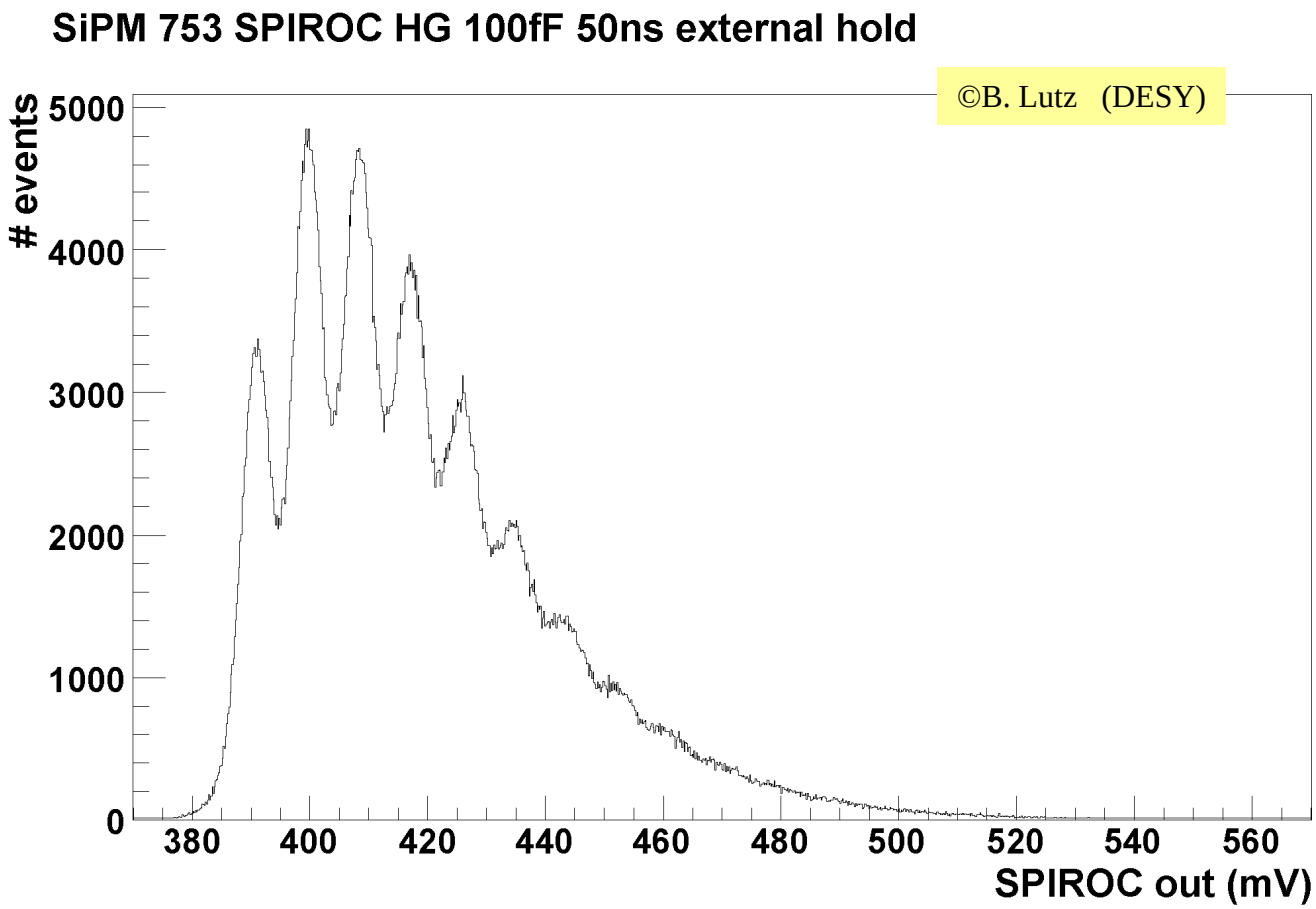


Noise in high gain shaper



Single photoelectron spectrum

- Spiroc1 can already replace FLC_SiPM (multiplexed analog output)



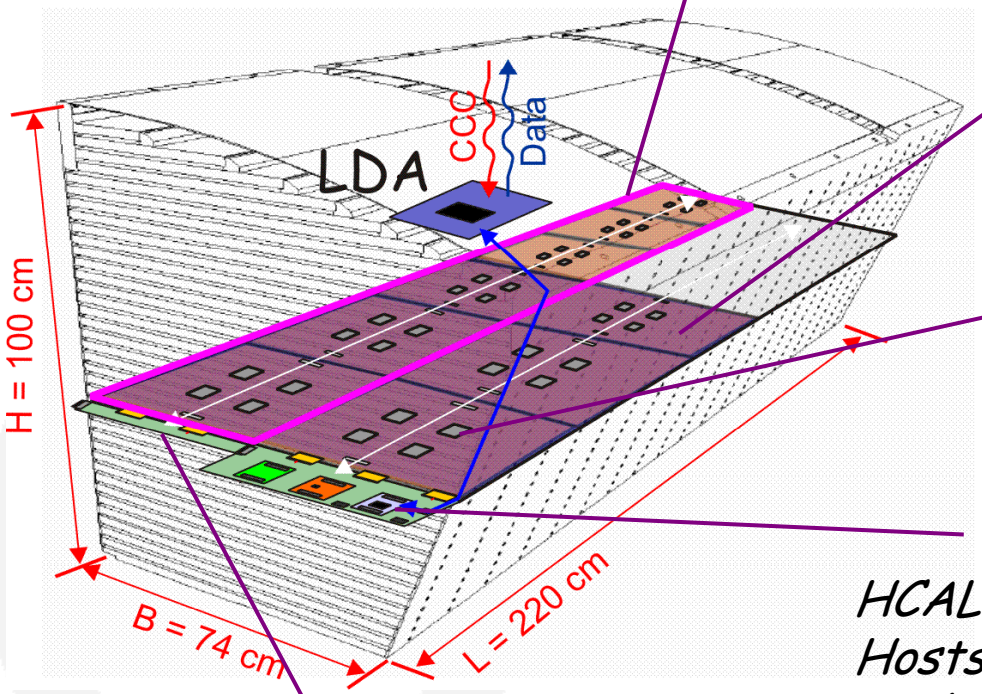
Conclusion

- SPIROC is a versatile readout chip for SiPM photodetectors
- It provides
  - Charge measurement from 1 pe to 2000 pe in two linear scales with a signal to noise ratio of 10
  - Time measurement to better than 1 ns
  - Auto-trigger on ½ pe with internal 10 bit DAC
  - Ultra low power 5V 8bit input DAC for SiPM gain adjustment
  - 25 µW/ch with 1% ILC Power pulsing
  - On chip Wilkinson ADC and RAM for daisy chain readout
- It will be produced in large scale in 2009 for the EUDET AHCAL module
- More information on MAROC, HaRDROC, SPIROC, SKIROC, PARISROC on http://omega.in2p3.fr

Backup slides

Barrel HCAL architecture

1/16 of barrel half



AHCAL Slab
6 HBUs in a row

Front end ASICs embedded
Interfaces accessible

HBU
HCAL Base Unit
12 x 12 tiles

SPIROC
4 on a HBU

HEB
HCAL Endcap Board
Hosts mezzanine modules:
DIF, **CALIB** and **POWER**

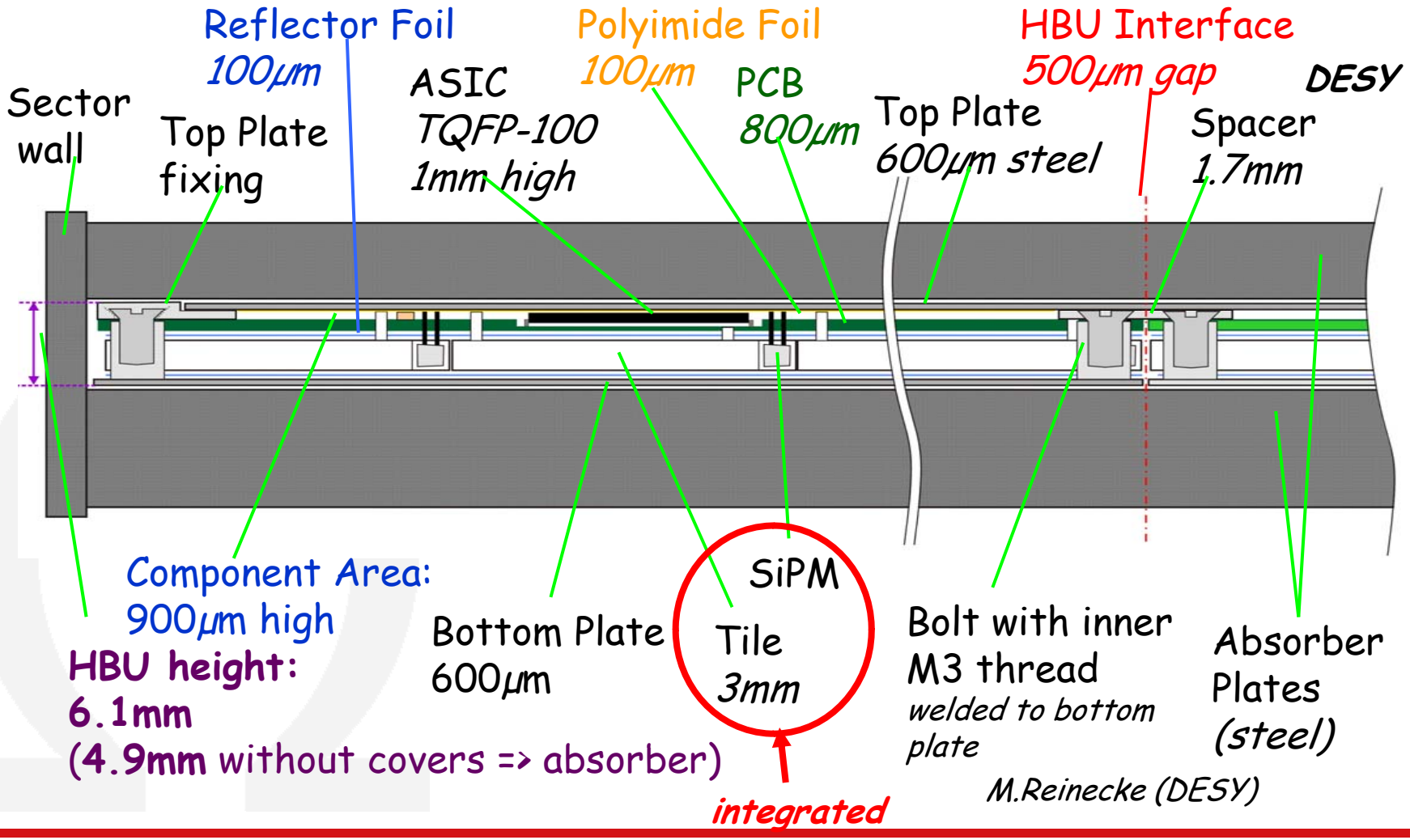
HLD
HCAL Layer Distributor

Power:
40 µW / channel

Heat:
T grad. 0.3K/2m
Time constant: 6 d

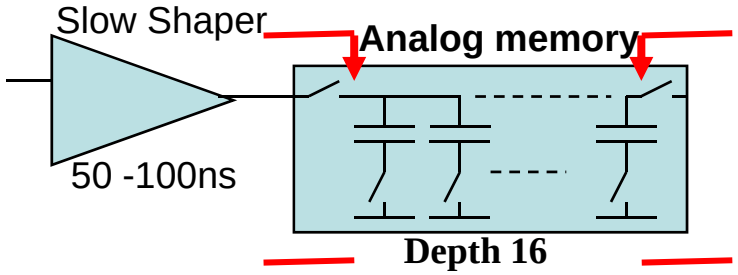
P.Goettlicher (DESY)

Integrated layer design

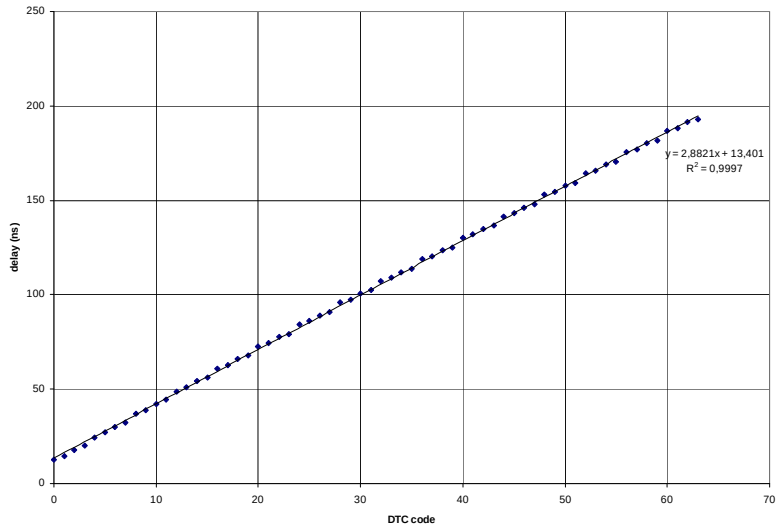


Slow shaper & SCA

- Slow shaper from HaRDROC
  - Variable peaking time : 50-150 ns
  - 3 bits common to all channels
  - High Gain = 10 mV/pe
  - Noise = 900 µV
  - Low gain = 1 mV/pe

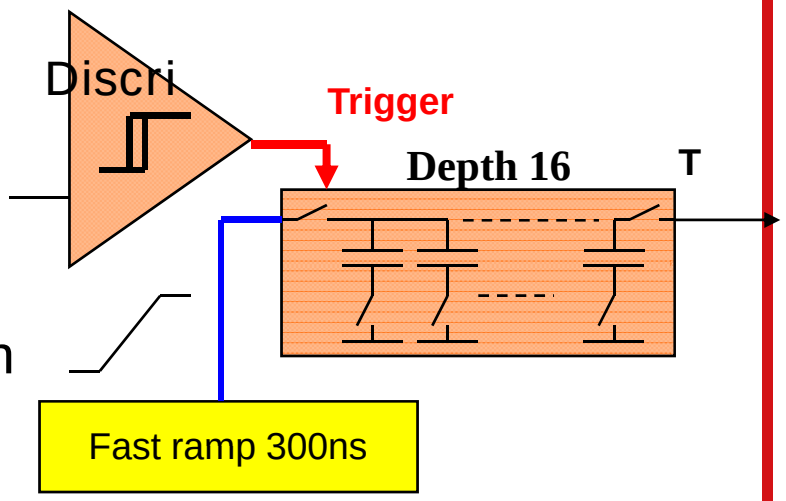


- Backup : analog T&H from HaRDROC
  - Hold capacitor : 2pF -> 0.5 pF
  - Needs external hold signal
  - Multiplexed analog output @ 5MHz
  - Allows readout with DAQ0



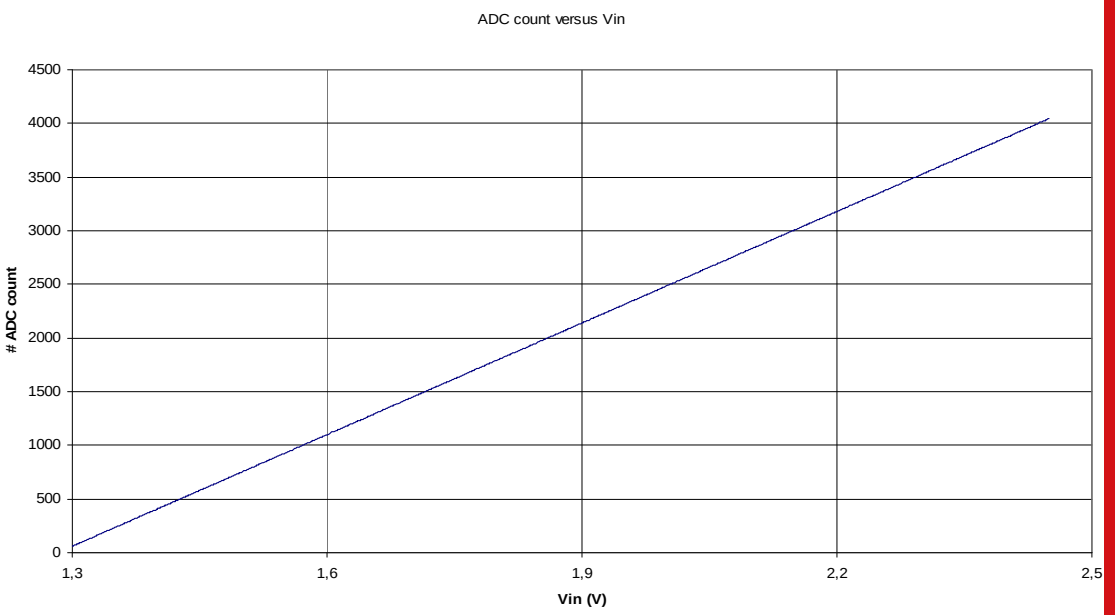
TDC

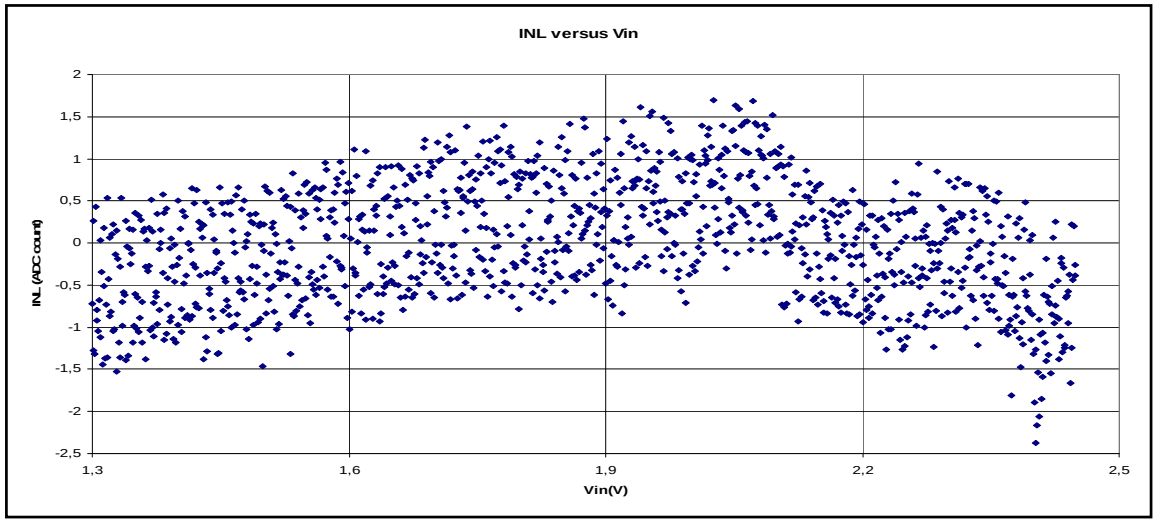
- New block
  - 12 bits
  - 300 ns full scale
  - 100 ps LSB (not accuracy !)
  - « common start » = BC
  - Time stored in SCA together with charge
  - Can also be readout with backup analog

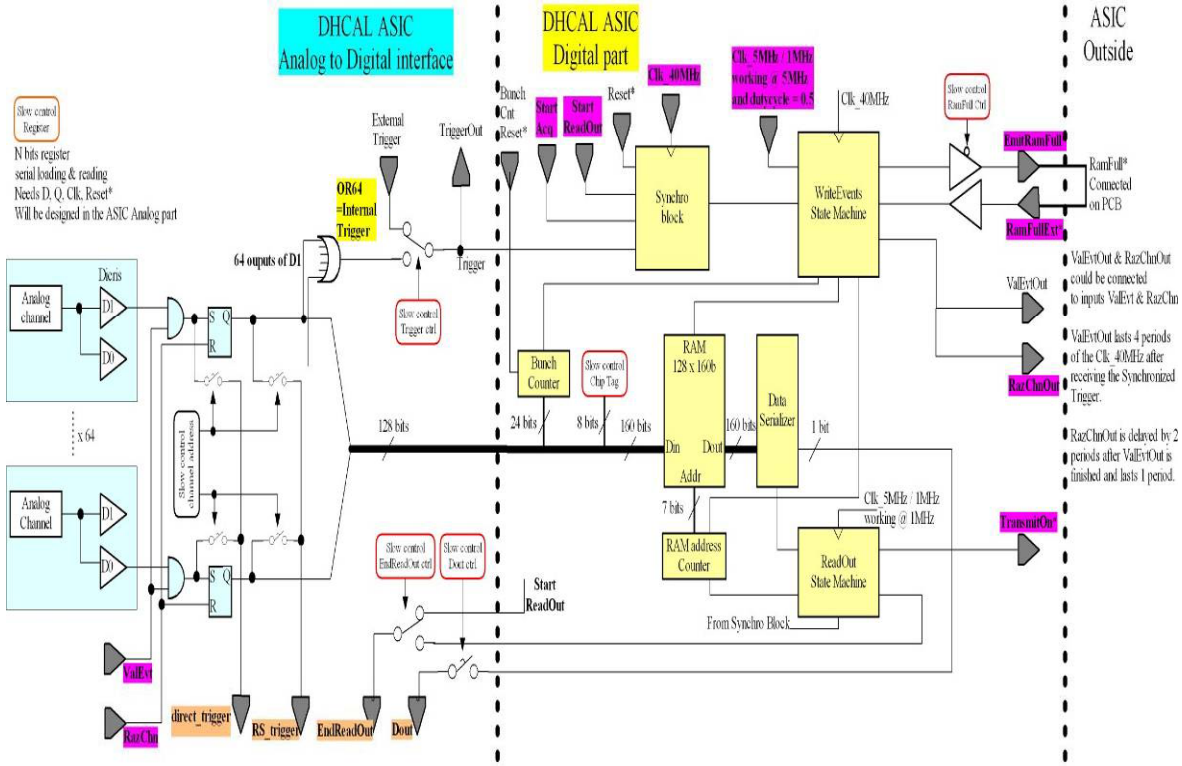


Wilkinson ADC

- Taken from MAROC
  - New : adjustable resolution : 8 - 10 or 12 bits
  - 40 MHz clock
  - 6-100 µs conversion time
  - Power dissipation : 350µW





Digital part

- Inspired from HaRDROC
  - Internal or external Trigger
  - OR36 output
  - Discriminator Validation fast input
  - 4kbyte RAM
  - « Open collector » output signals
  - LVDS clocks
  - Start conversion
  - Start/end readout