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Digital Part of PARISROC: a Photomultiplier Array ReadOut Chip

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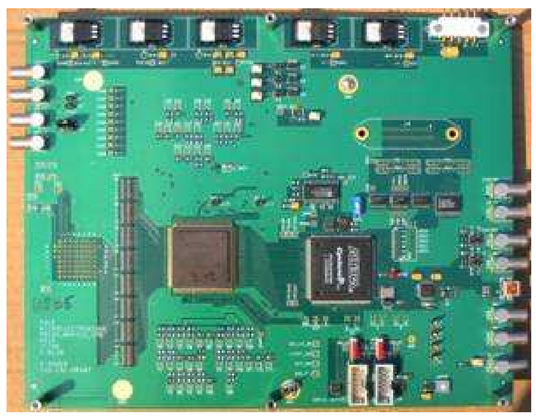
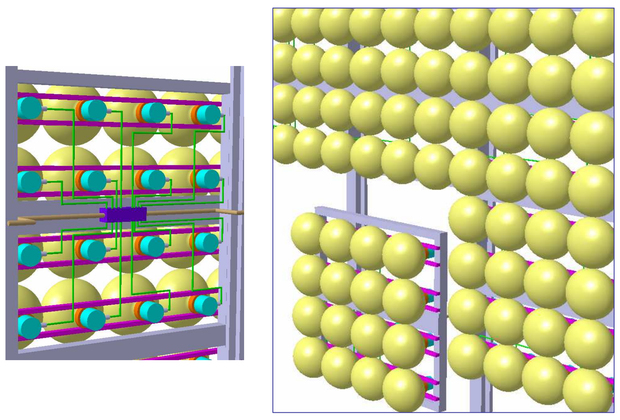
PARISROC Test Board



- 16 PMT inputs can be read by 1 PARISROC chip
- SCA depth of 2 for charge and fine time measurements
- FIFO management of SCA
- Triggerless and independent channels
- 24 bits timestamp counter @ 10 MHz (1.67s)
- 40 MHz clock for ADC and SCA management
- 10 MHz clock for Timestamp + Readout
- AMS 0.35µm-3B standard digital cells

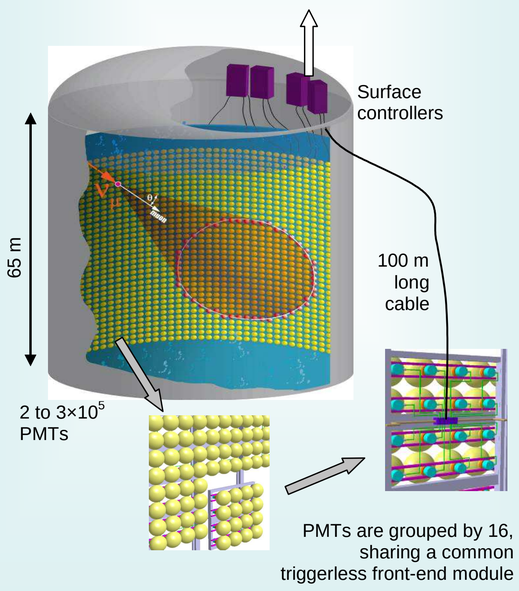
Module of 16 PMTs



Principle of megaton scale Cerenkov water tank

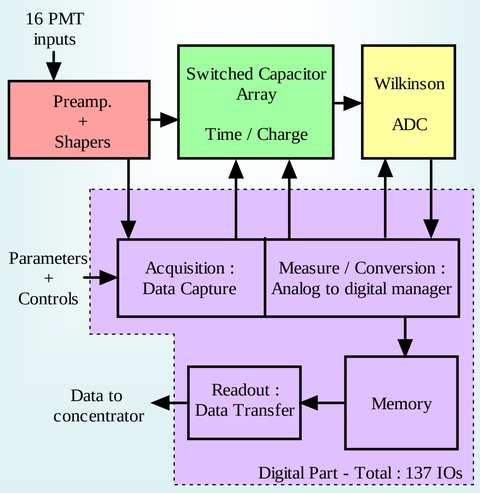
Offline processing (on the surface):

- Coincidence
- Noise rejection
- Trajectory reconstruction



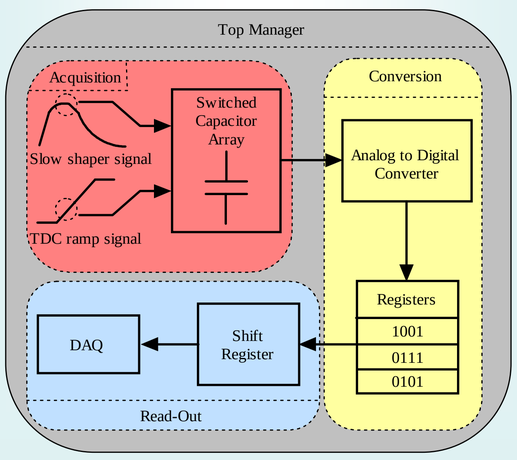
Block Diagram of PARISROC

PARISROC (Photomultiplier ARray Integrated in Sige ReadOut Chip) is the front end ASIC designed for the PMM2 R&D project dedicated to neutrino experiments. Next generation of neutrino experiments that will take place in megaton size water tanks will require very large surface of photodetection and volume of data. For the funded project, this large surface of photodetection is segmented in macro pixels made of 16 Photomultiplier tubes (PMT) connected to an autonomous front end ASIC: PARISROC.



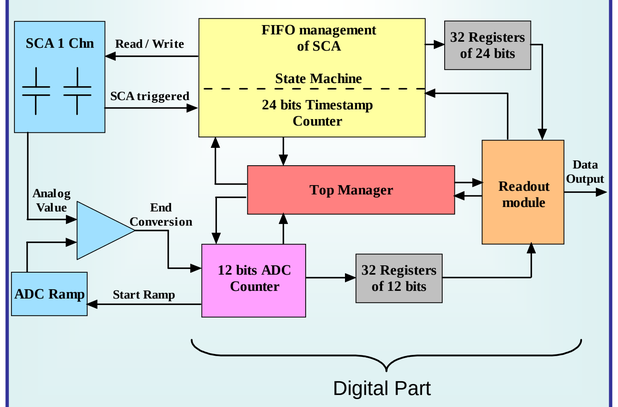
High level working

The digital part of PARISROC is built around 4 modules which are acquisition, conversion, readout and top manager. Actually, PARISROC is based on 2 memories: during acquisition, discriminated analog signals are stored into an analog memory (the SCA: switched capacitor array). The analog to digital conversion module converts analog charges and times from SCA into digital values. These digital values are saved into registers (RAM). At the end of the cycle, the RAM is readout to an external system.



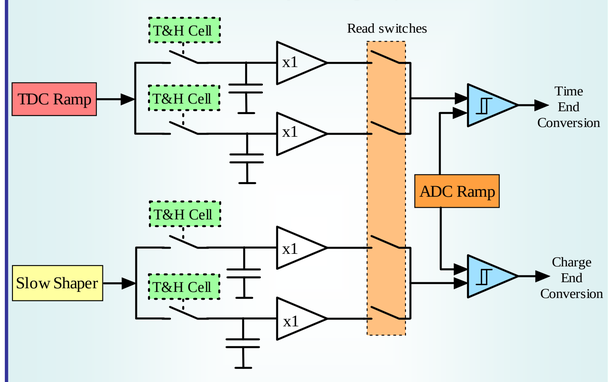
Low level working / block diagram

As the 16 channels of PARISROC are managed independently, 2 state machines are dedicated to handle 1 channel: 1 for write pointer and 1 for read pointer. This implies 32 registers of 24 bits to save coarse time for each depth of SCA. At a high level point of view, SCA of 1 channel is controlled as an analog FIFO.
Conversion is common for all channels and needs 32 registers of 12 bits to store converted data: 16 for charges and 16 for fine time measures.
As the readout will only treat hit channels, this module will tag each frame with its channel number.

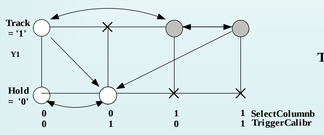


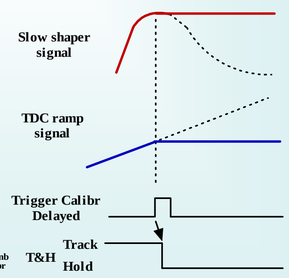
Detail of a SCA channel

The chip has 16 channels. Each channel has a depth of 2 for charge and 2 for fine time storage. The SCA column is selected, read and erased by the digital part.



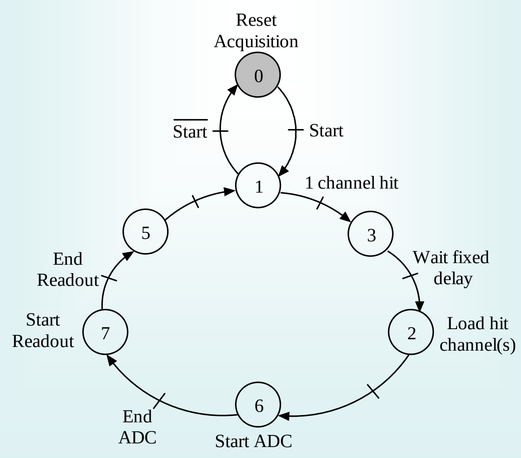
"Track & Hold Cell" allows to lock the capacitor value only when a calibrated trigger occurs within the selected column.





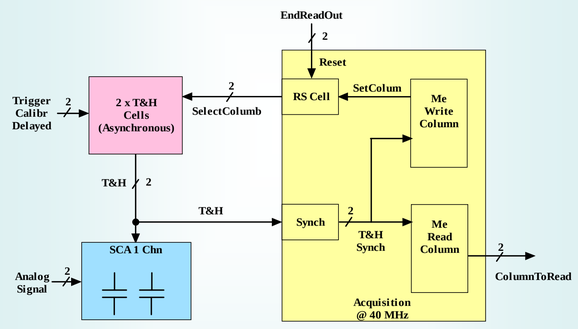
Detail of Top Manager

The top manager module controls the 3 others ones. It allows to start and to stop them to realize the right sequence for an autonomous working.
When 1 channel is hit, the top manager waits for a constant time to allow triggers on others channels. Then, it launches ADC conversion and readout of digitized data. The maximum cycle length is about 200µs when all channels are hit.
During conversion and readout, acquisition is never stopped. That's mean that discriminated analog signals can be stored in the SCA at any time of the sequence if SCA is not full.

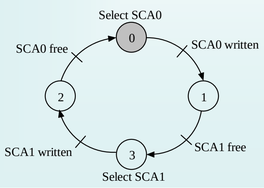


Detail of Acquisition

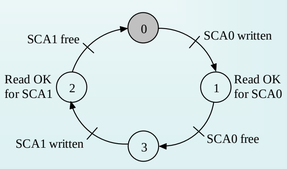
This module is dedicated to charge and time measurements. It manages the SCA where charge and fine time are stored as a voltage. It also integrates the coarse time measure thanks to a 24 bits gray counter with a resolution of 100 ns.
Each channel has a depth of 2 for the SCA and they are managed individually. Besides, SCA is treated like a FIFO memory: analog voltage can be written, read and erased from the memory.



Write/Select State Machine

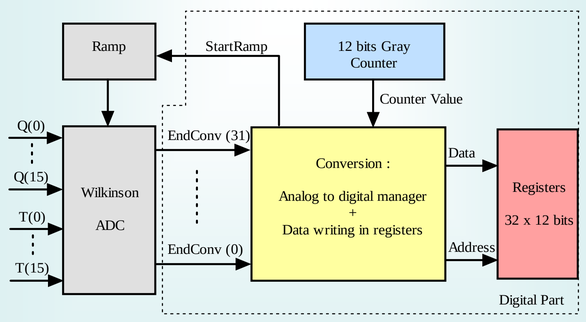


Read State Machine



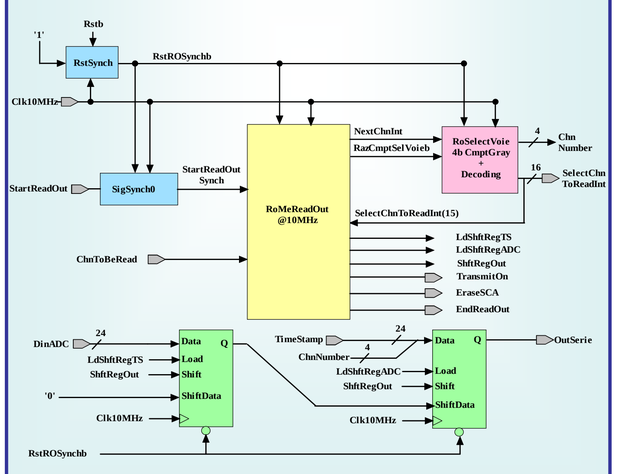
Detail of Conversion

The main purpose of this module is to convert analog values stored in the SCA in digital ones thanks to a 12 bits Wilkinson ADC. The ADC clock frequency is 40 MHz, it implies a maximum ADC conversion time of 103 µs.
Each ADC run converts the fine time and the charge of each channel even if it was not hit: 32 conversions in 1 run. Only the data of hit channel will be treated by the readout module.

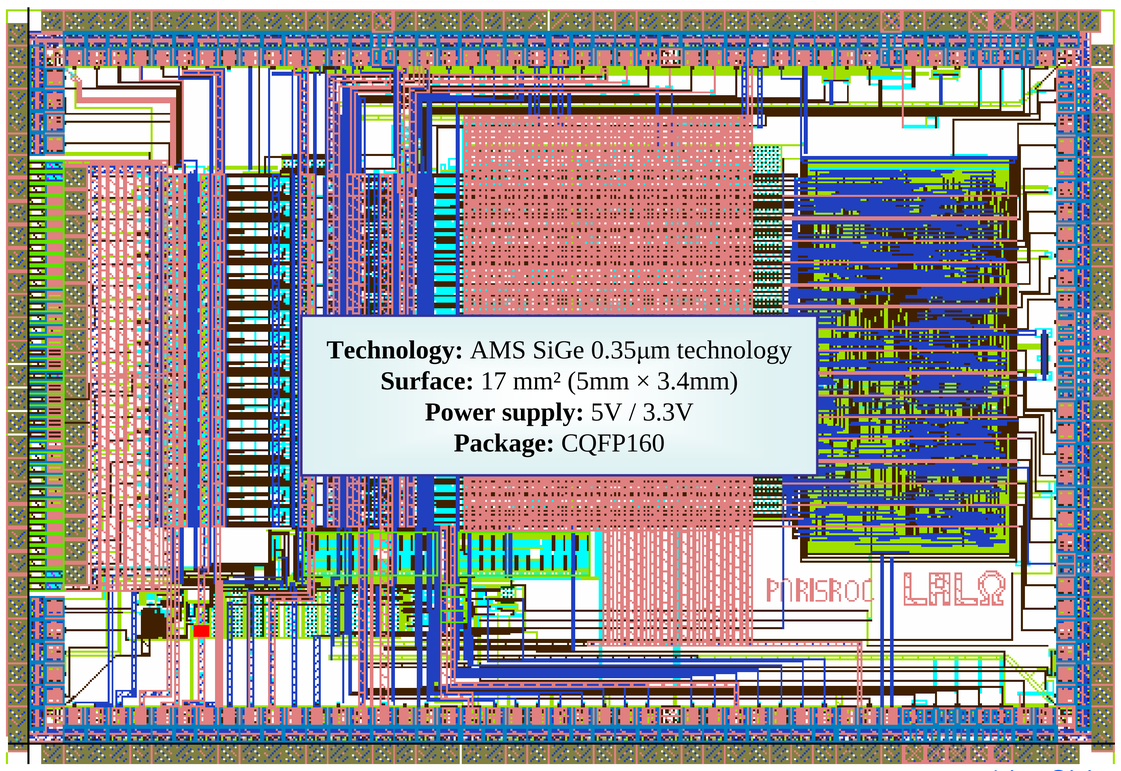


Detail of Read-Out

The Readout module permits to empty the registers. It works as a selective readout: only hit channels are transferred. In the case of all channels hit, about 832 bits of data are transferred to the concentrator with a 10 MHz clock.
The pattern used is composed of 4 data: channel number, coarse time, charge and fine time. Each data is coded in gray and the total number of bit for one frame is 52 bits. When all channels are hit, the readout takes about 100 µs (time between 2 frames is about 1 µs).



PARISROC Chip layout

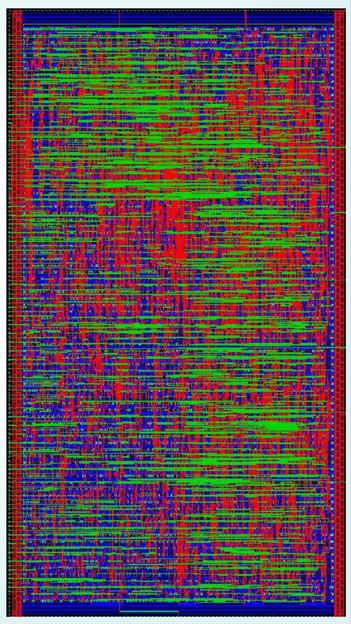


Digital part Layout

The layout of the digital part was realized in 0.35 µm technology from Austria Micro System (AMS) and designed with Soc Encounter from CADENCE.

The layout is on 3 metals (blue, red and green) and its size is 1800 µm by 1000 µm.

The layout is composed by 10K standard cells (equivalent to 71K transistors).
It integrates 1152 memory registers and have a total net length of 1 meter.



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