Effect of cable on pulse shape

- Already studied (in 1998?) for present electronics
- The formulas in the time domain (modification to step pulse) are well known (for example in 1964 <u>http://lss.fnal.gov/archive/other/lbl-cc-2-1b.pdf</u>)
- A step pulse becomes as function of time
 [1. erf(0.6745*sqrt(t₀/2t)] therefore the cable effect depends on
 a single parameter t₀
- An estimate for the parameter t_0 is $t_0=4.56 \times 10^{-3} \times A^2 \times l^2/f$ where A is the cable attenuation in db/m, l is the cable length in m at a frequency f in MHz and t_0 in ns. This formula is not perfect since A^2/f is not constant for the cable we use KX3B.
- In 1998(?) t0 obtained by fitting a step pulse + 12.8 m of our cable measured with a scope => t₀=1.024ns



Some Mathematica plots(I) (fortran to old to get plots!)

effect on step function



Cable[x_] = 1 - Erf[0.6745 * (Sqrt[(0.5 * 1.024 / x)])]

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(II)



effect on delta function => differentiate step function and its transformed shape after the cable





Correction with filter

• Again old story! (196?) use a pole zero filter rC +R



- r/(R+r) = frac = attenuation of low frequency
- $rc \approx time \ constant$
- A delta function becomes δ (Frac/rc)*e^{-(t/rc)} optimum values are frac=0.16 rc=16ns



Integrated results for delta function after cable and correction

Time after δ integrated (δ +cable) integrated(δ +cable +cor) Δ of last col

1ns	0.494	0.492	
10 ns	0.829	0.732	
25 ns	0.891	0.779	
50 ns	0.923	0.777	-0.002
75 ns	0.937	0.781	+0.004
100 ns	0.946	0.786	+0.005
1000 ns	0.983	0.815	+0.029/40



Impact

- Two main consequences
 - Contribution to following samples
 - Modification of flat top over +-2ns (quantitative value? This should be calculated using measured pulse + calculated filter +integral) Calculation on this is the main priority in my opinion!



Pro and Con of possible corrections(I)

- Subtraction of following pulse in FPGA and improvement of flat top with R on integrator
 - Pro simplest for hardware
 - Con: mixes pedestal subtraction and 2-integrator calibration with cable correction
 - Con: Heavy in firmware
- Filter using an added stage before the integrator in ASIC
 - Pro: probably the cleanest method
 - Con: added work and complication for ASIC
 - Con: Asic becomes set-up specific :depends on cable (Is this a real problem???)



Pro and Con (II)

- Put the compensation filter on the PCB (needs 4 components to conserve 50 ohms adaptation)
- A possible solution is r=8 ohms C =2nanofarad (2.2?)
- R= 50 ohms of the Asic in// with (a resistance of 262 ohms + an inductance of 5microHenry in series)
- This allows to have an input impedance of 50 ohms at all frequencies (until the inductance stops working= max frequency=150MHz in radiospare)
 - Pro: rather flexible and optimised at PCB time (later than ASIC)
 - Con: 4X32 components per cards including 32 5-microH inductances
 - Con: could impact the noise? (to be calculated or tested)



Conclusion

- Need to define time scale (time for final decision)
- In my opinion a least a test of the PCB solution should be done and tested to insure the existence of the solution at least as backup

