3D activities @ CEA-LETI

D. Henry / CEA-Leti-Minatec

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Outline

- **Introduction**
- **Medipix 3 project status**
- **3D Technological toolbox @ LETI**
  - **Available technologies / short term projects**
  - **Technological modules developments / Mid & long term projects**
  - **Products examples**
- **Conclusions / prospects**

CEA - Leti at a Glance

Commissariat à l'Énergie Atomique et aux Énergies Alternatives

is one of the largest research organizations in Europe, focused on energy, health, information technologies, and national defense

16,037 **People** (10% PhD and Post Doc)

10 **Research centers**

CEO Dr. Laurent Malier

Founded in 1967 as part of CEA

1,700 researchers

190 PhD students + 34 post PhD
with 70 foreign students (30%)

Over 1,700 patents

265 generated in 2010
40% under license

210 M€ budget

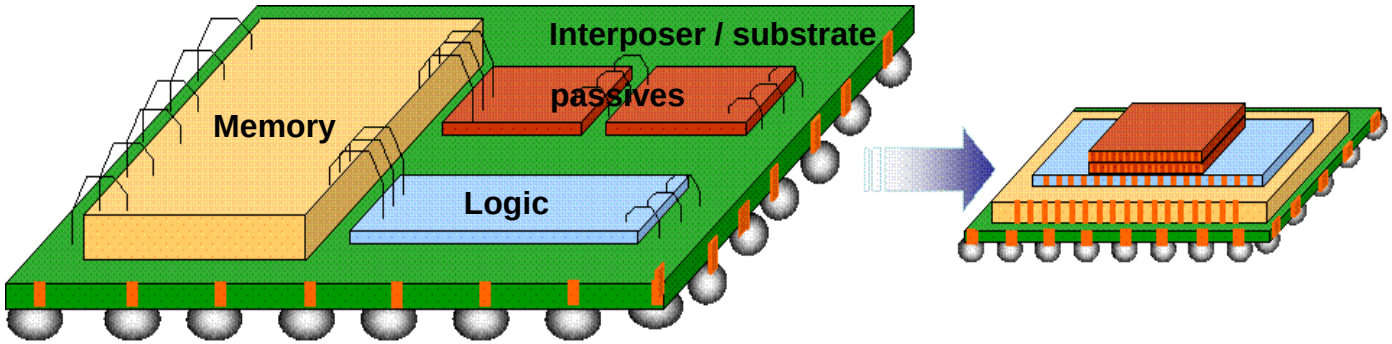
~ 40M€ CapEx

40 start-ups & 265 industrial partners

Introduction : What is 3D Integration ?

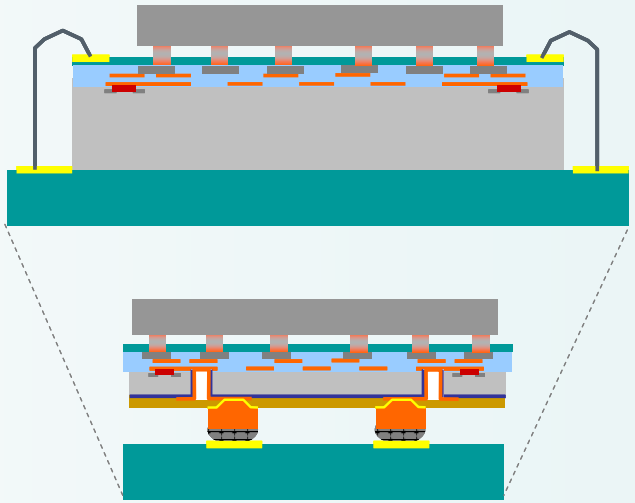
- In electronics, a 3D integrated circuit is a chip in which two or more layers of active electronic components are integrated vertically into a single circuit, component or system.

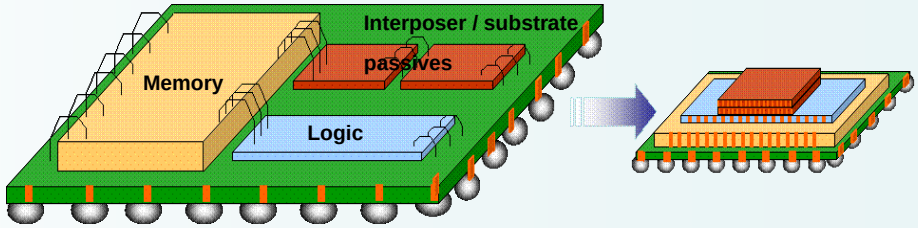
- 3D Integration key drivers :
  - Form factor decrease
  - Performances improvement
  - Heterogeneous integration
  - Cost decrease



Introduction : Why do we need 3D Integration ?

- To solve the following issues :
  - Form factor decrease :
    - X & Y axis
    - Z axis
  - Performances improvement
    - Decrease R, C, signal delay
    - Increase device bandwidth
    - Decrease power consumption
  - Heterogeneous integration
    - Integration of heterogeneous components in the same system
  - Cost decrese
    - Si surface decrease
    - Reuse of existing Packaging, BEOL & FEOL lines



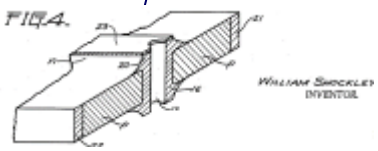


3D Integration electronic components (brief) history

- First products in the middle of the 90's
  - From MCM 2D to MCM 3D

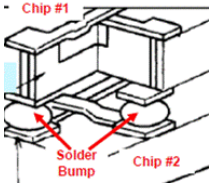
- Two phases :
  - From 80's to 2003 : start-up phase
  - Until 2005 / 2006 : Prototype phase

1962



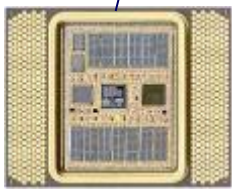
TSV Invention
Nobel Prize W. Shockley – Bell Labs

1986



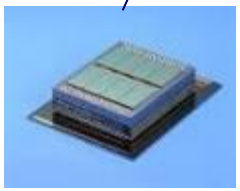
3D IC first concept
Y Akasaka

1990



MCM 2D for radar applications - Astrium

1997



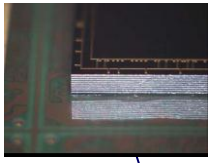
Vertical 3D Stacking -LETI

1999

MCM 3D - LETI

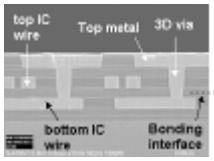
6 Memories stack with WB Samsung

2003



10 Memories chips stacked with TSV Hitachi - Renesas

2005

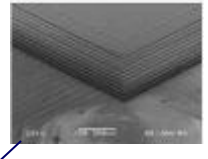


3D IC CEA LETI

2006

Heterogeneous stack Irvine sensors

2007



10 chips stacked NEC

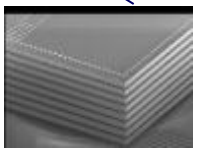
2008

Memories stack 3D Plus

2009

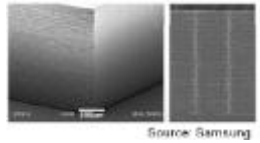
Memories stacked with TSV on Logic Intel

2010



8 Memories chips stacked with TSV Elpida - NEC

32 chips stacked Samsung



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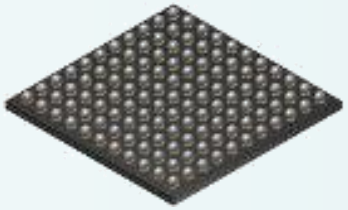
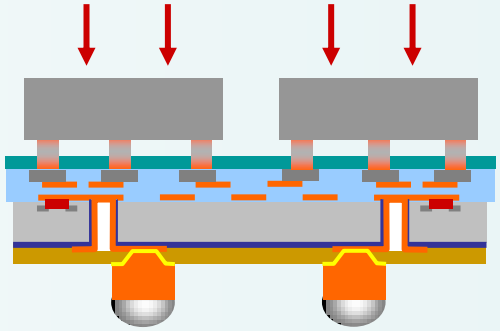
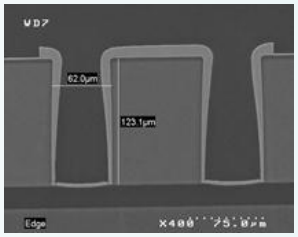
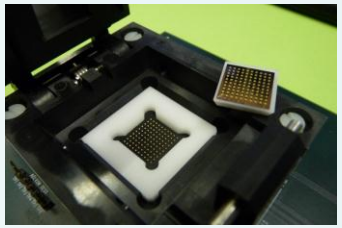
Medipix 3 project status (summary)

- **Customer:** CERN
- **Project start up:**
  - June 2011
- **Objectives :**
  - Fabrication of a read-out chip with TSV
  - Assembly of a particle detector on top of it
  - Proof of concept
- **Project status**
  - 1st lot: µS6688P (2 wafers)
  - 2nd lot: µS6924P (3 wafers)
  - 3rd lot: µS7394P (3 wafers)
- First lot delivered on January 2012 ➔ not in specification
- Third lot delivered on June 2012 ➔ OK
- Dicing & pick out issues @ LETI & VTT
- Dicing solution in october 2012
- CERN electrical tests :
  - Preliminary (14 chips) ➔ OK
  - Complete tests + detectors assy on going



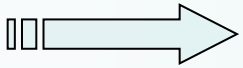


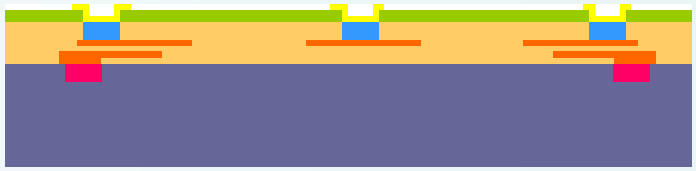




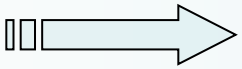
Medipix 3 process flow

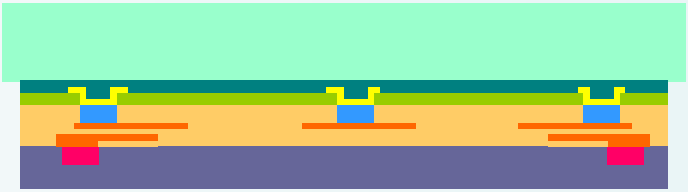
- **Front Side UBM**
  - UBM
    - TiNiAu Deposition
    - Litho UBM JSR335
    - UBM etch



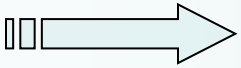


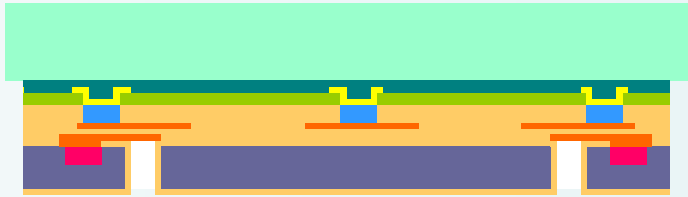
- **Bonding / Thinning**
  - Bonding HT1010
  - Grinding/edge dicing
  - CMP Si

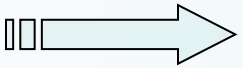


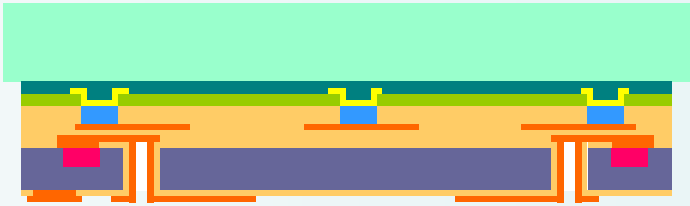


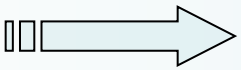
- **Back Side: TSV Last + RDL + Passivation + UBM**
  - TSV
    - Litho TSV JSR335
    - TSV AR2 etch
    - SiON conf deposition
    - Etch back
    - SEED TiCu
  - RDL
    - Litho RDL
    - ECD Cu 10µm
    - Litho PASSIV ALX 7µm
  - UBM
    - TiNiAu deposition
    - Litho UBM JSR335
    - UBM etch
    - Debonding

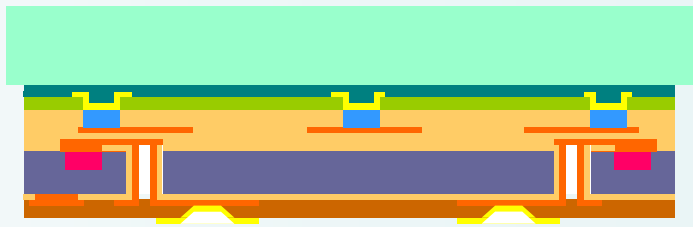






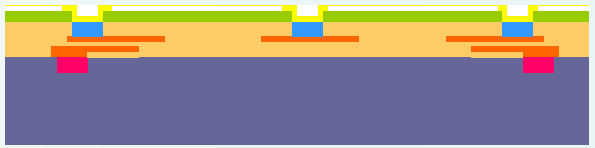


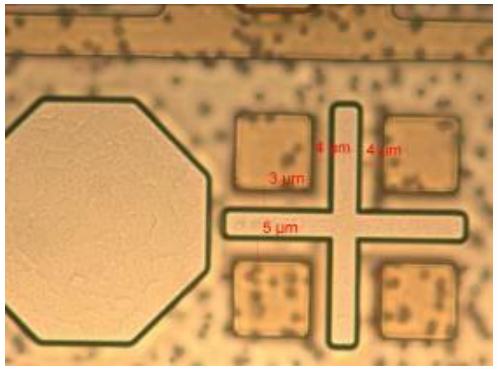




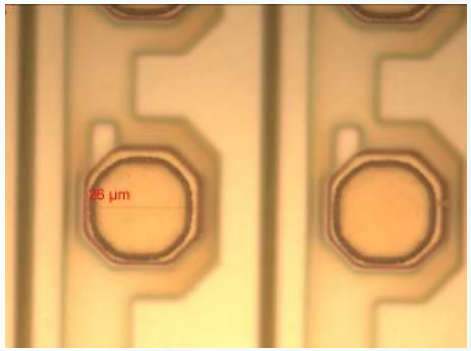
Medipix 3 project results

- **Front Side**
  - Front Side topology = 4µm
  - Alu/UBM contact resistance: Preclean + Ti / Ni / Au deposition
  - UBM litho: positive photo resist
  - Alignment on Top metal (Specs +/-1µm):

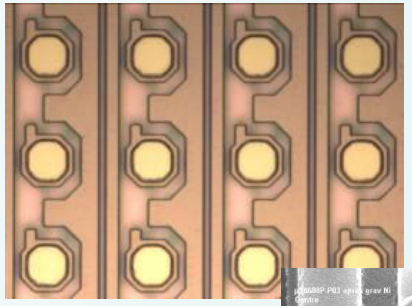


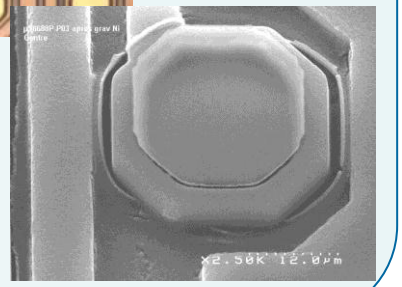


Alignment marks UBM/Final metal



Pixels after litho

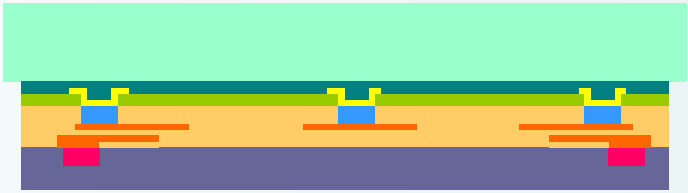




Pixels after etch

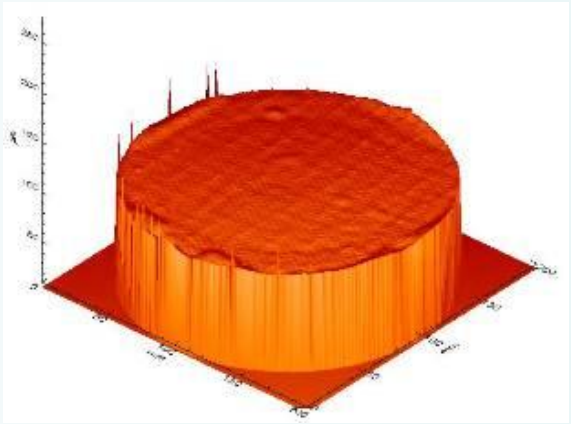
Medipix 3 project results

- **Bonding on a temporary glass carrier**
  - HT1010 (BSI product)
  - Bonding on EVG520
  - Accoustic microscope inspection



- **Silicon thinning to 120µm**
  - Coarse grinding until 200µm
  - Edge timming until 1.5mm
  - Coarse + Fine grinding until 125µm
  - Silicon CMP (2µm) until 120µm + scrubber

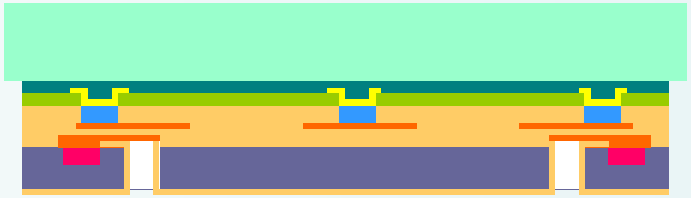
P01-SONOSCAN inspection



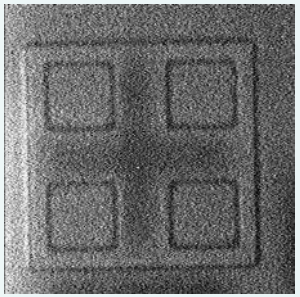
P01-3D mapping-Si thickness post grinding

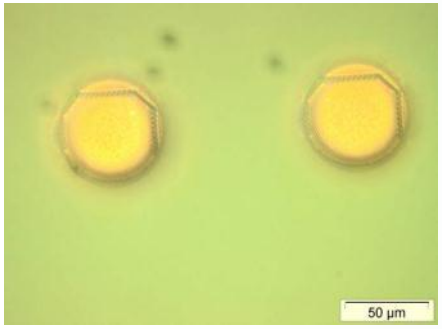
Medipix 3 project results

- **TSV patterning**
  - Hard mask deposition:
  - TSV :
    - Photo resist
    - Alignment BS (TSV) / FS (UBM)
    - CD=60µm (AR 2:1)
    - TSV etch process ➔ Multi step
      - HM etch
      - Si etch : Bosch process
    - TSV insulation :
      - LT dielectric deposition
      - Bottom etch to contact M1

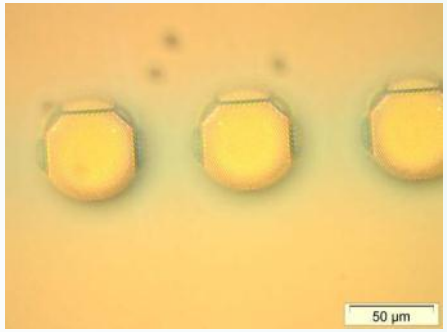


Alignment marks BS/FS

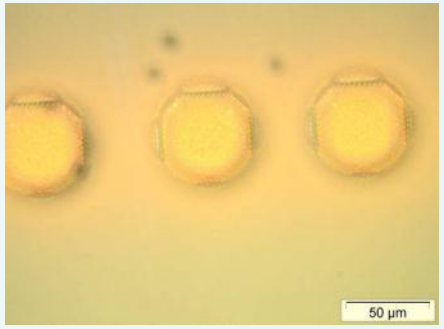




edge



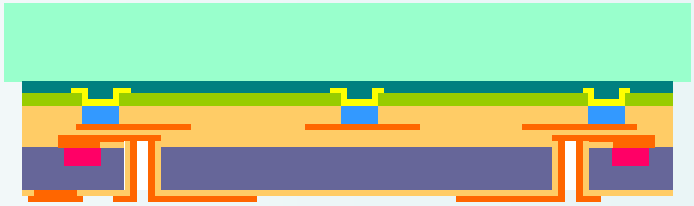
mid-radius

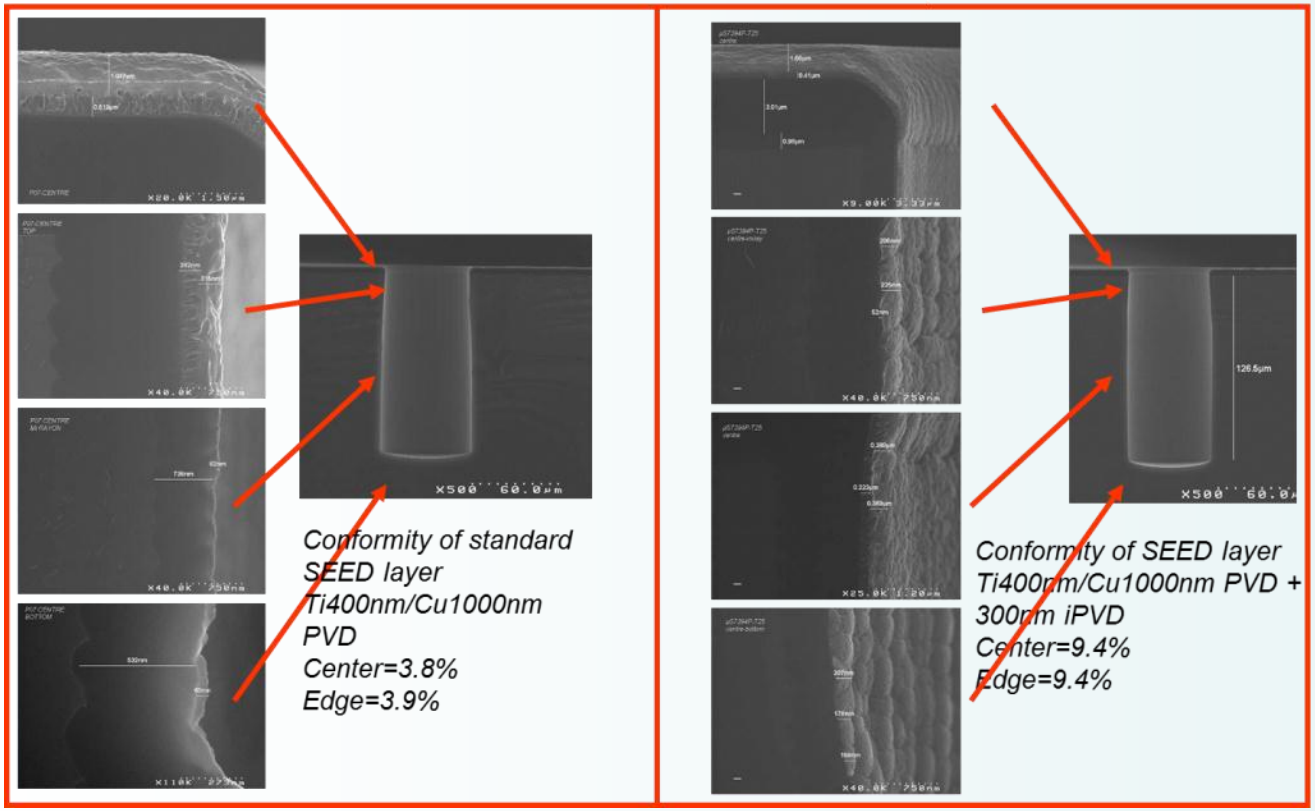


center

Medipix 3 project results

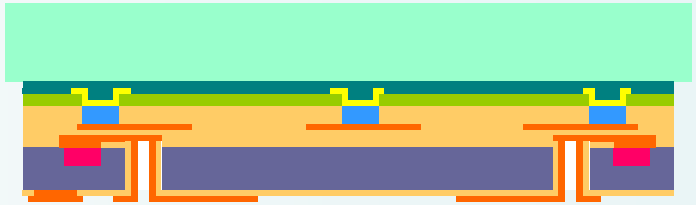
- **TSV Metalization + RDL**
  - P01 and P03: Seed layer deposition Ti 400nm / Cu 1000nm (PVD)
  - P02: Ti 400nm/ Cu 1000nm (PVD) + Cu 300nm (IPVD)

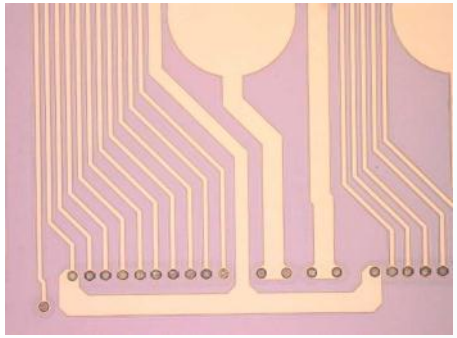




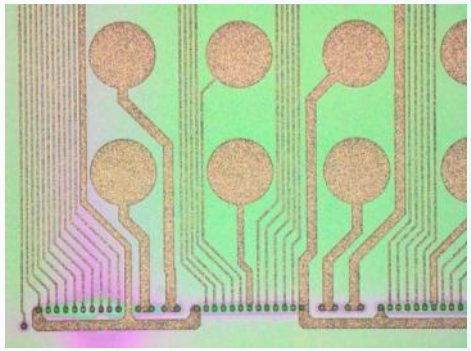
Medipix 3 project results

- **TSV Metalization + RDL**
  - RDL litho : Dry film 15 µm
  - ECD Cu 9µm
  - Stripping
  - Seed layer Cu + Ti etch
  - RDL line thickness control

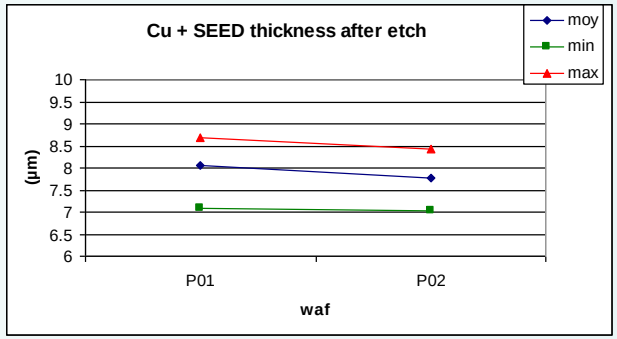




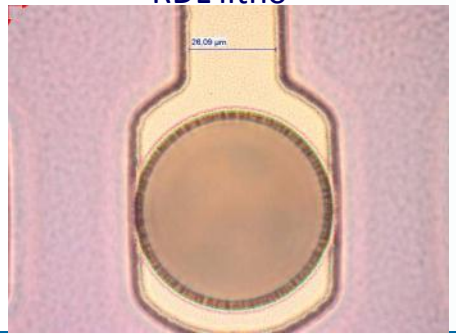
RDL litho

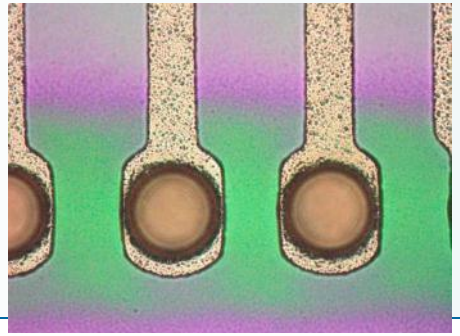


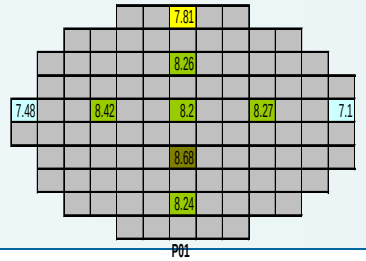
RDL Cu line on TSVs



RDL Cu line thickness control (graph + map)

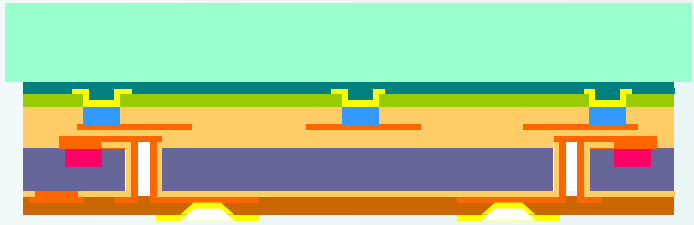


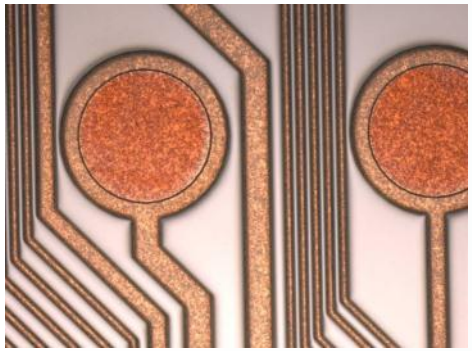




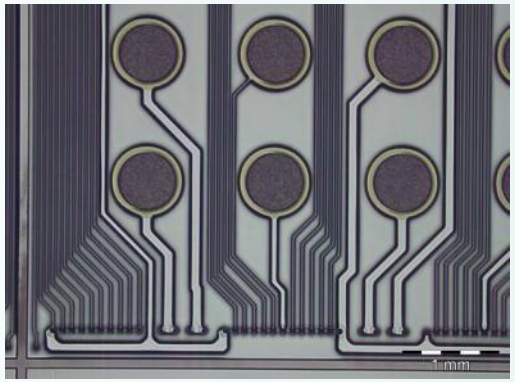
Medipix 3 project results

- **Passivation + backside UBM**
  - Litho process
  - Photosensitive polymer
  - UBM deposition (TiNiAu)
  - UBM litho
  - UBM etch, stop on polymer



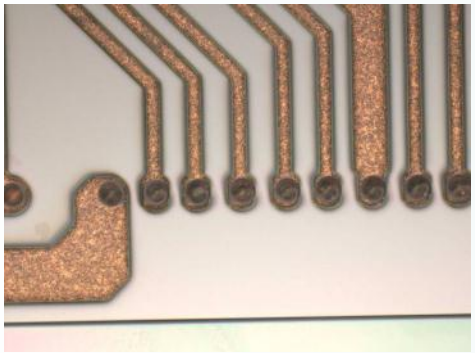


BGA matrix

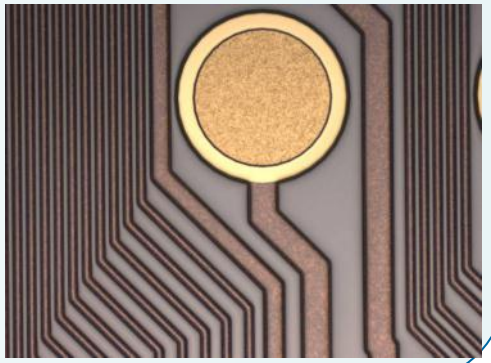


Functional die after litho UBM

Polymer covering the TSV

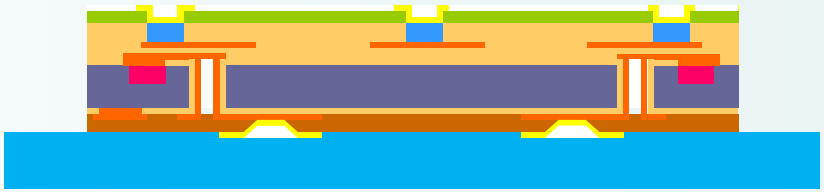


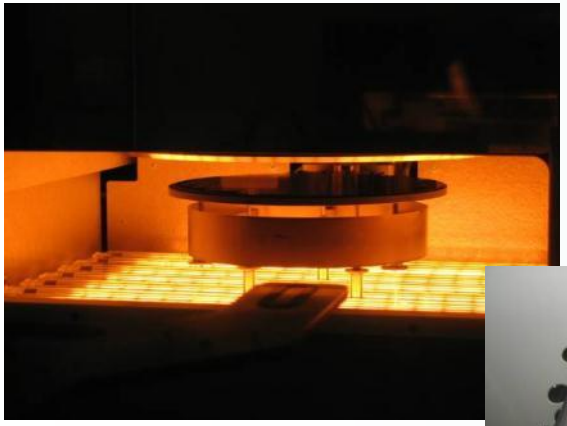
Functional die after UBM etch



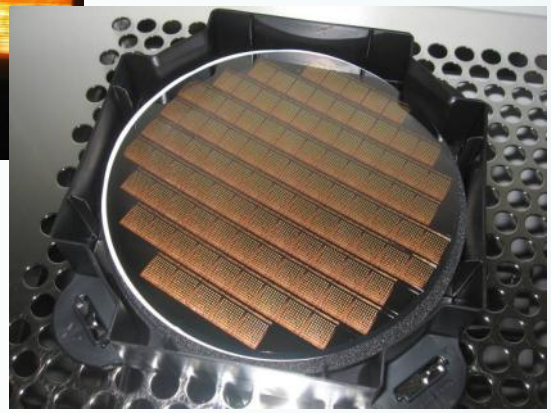
Medipix 3 project results

- **Debonding / Cleaning**
  - Debonding (slide-off)
  - Cleaning with Wafer Bond remover
  - Delivery for dicing

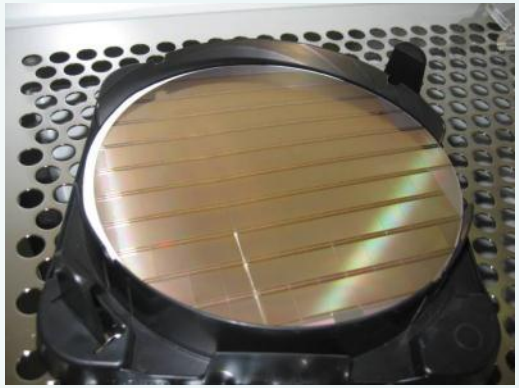




Slide off debonding



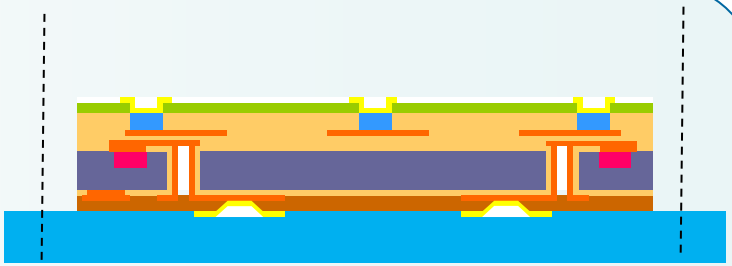
P02- After debonding

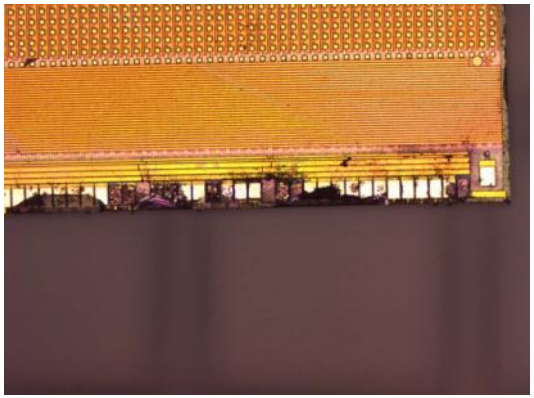


P01- After debonding

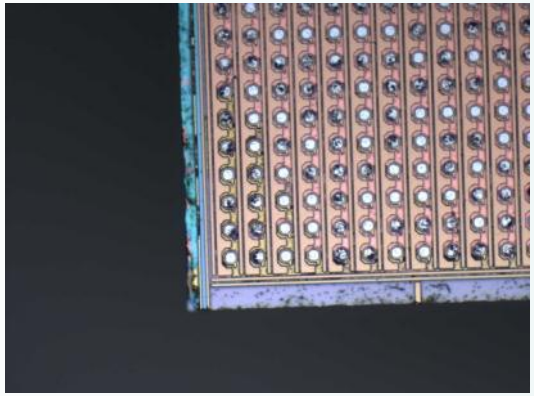
Medipix 3 project results

- **Chips Dicing & boxes packaging**
  - First delivered wafers :
    - Metal delaminations on front side
    - High chipping on the edges
    - Chips breaking during pick out process
    - Tape residues on pixel side

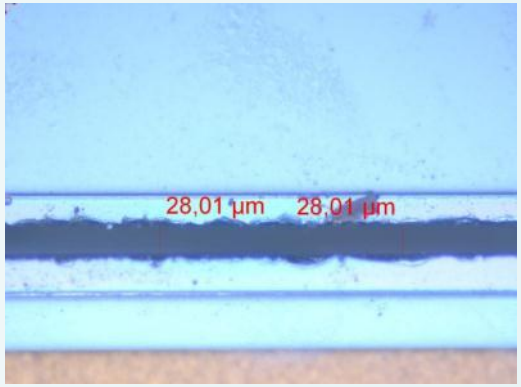




High chipping + pad delamination



Tape residues

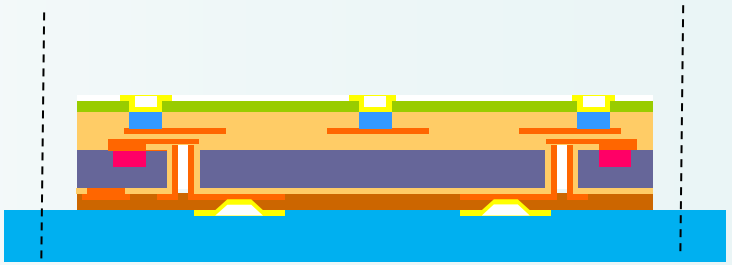


Backside chipping

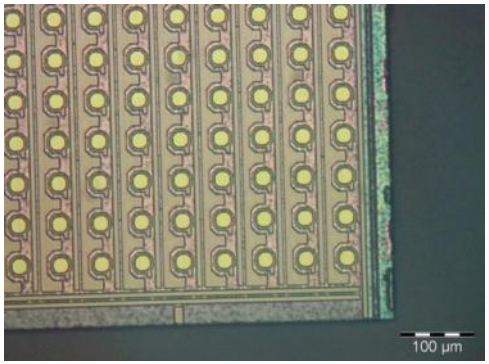
- **Need to develop an optimized dicing process :**
  - DISCO collaboration

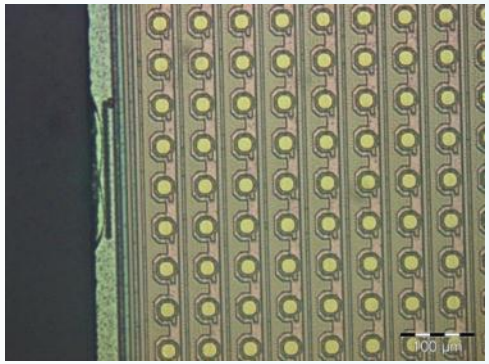
Medipix 3 project results

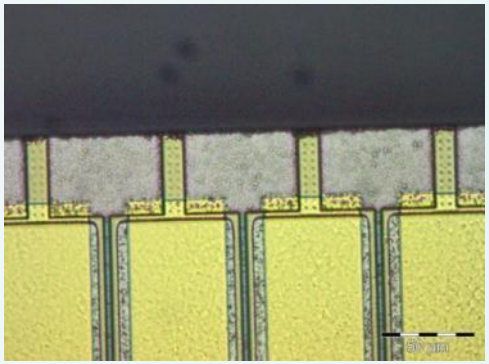
- **Dicing trials on DISCO plant (Munchen)**
  - Taping of BGA side on the tape
  - UV tape
  - Fine blade
  - High Blade rotation
  - Low Blade speed



- **Pixel side observations**
  - Chip I4



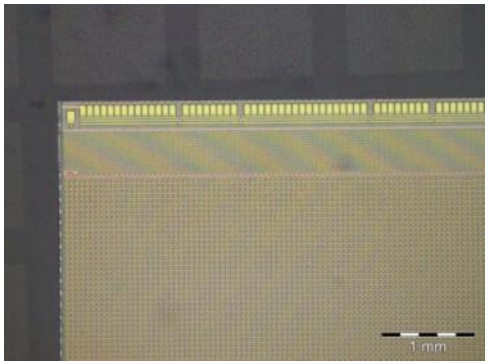


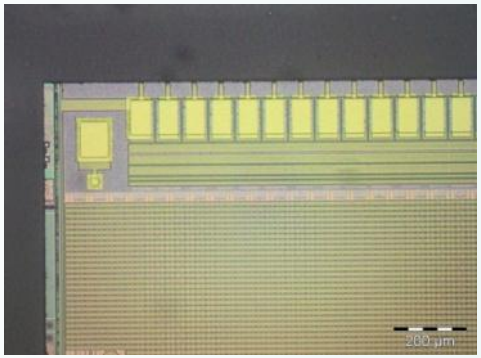


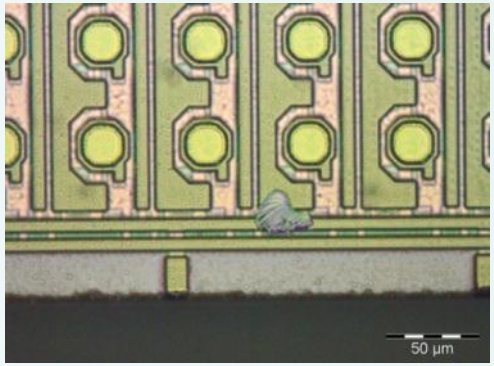
  - Lower chipping compare to previous dicing
  - Every defects localized on dicing streets

Medipix 3 project results

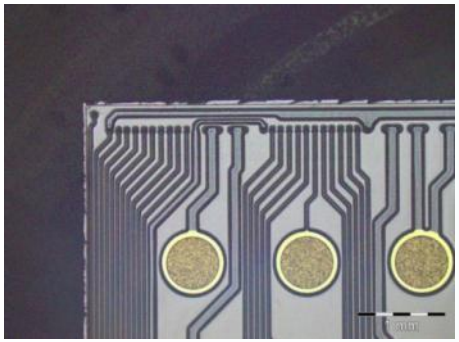
- **Pixel side observations**
  - Chip I4

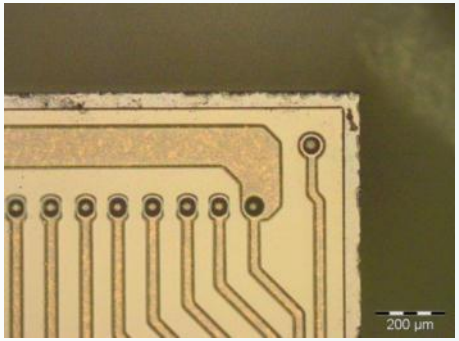


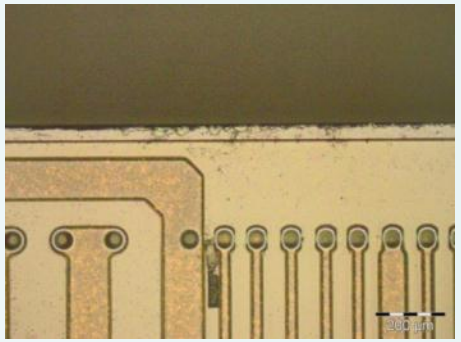




- **BGA side observations**



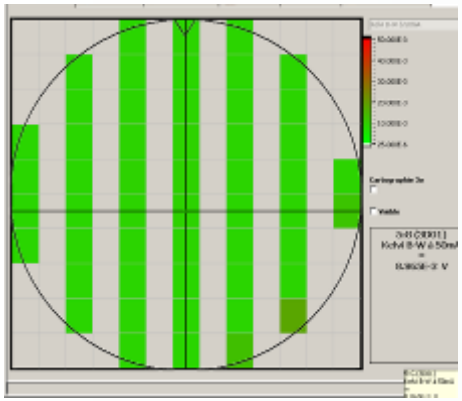




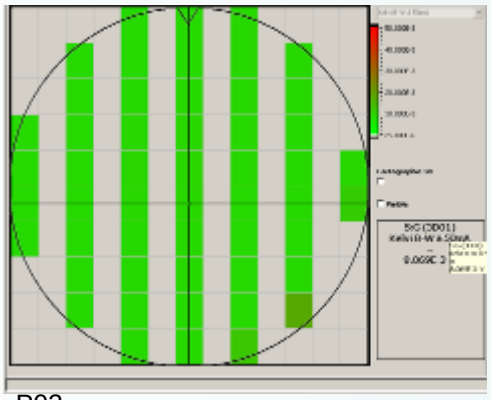
  - Higher chipping than on the pixel side ➔ contact with tape
  - All defects localized on the dicing streets ➔ polymer seal ring effect

Medipix 3 project results / electrical tests (non exhaustive)

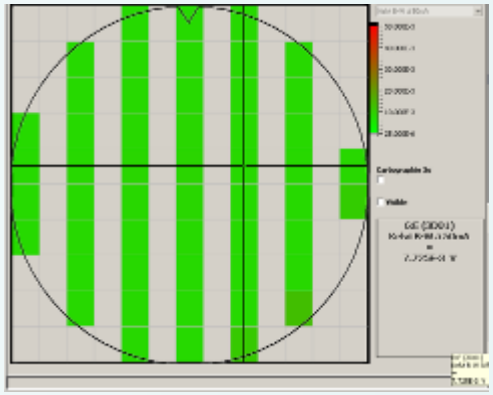
- **UBM/ Al contact resistance**



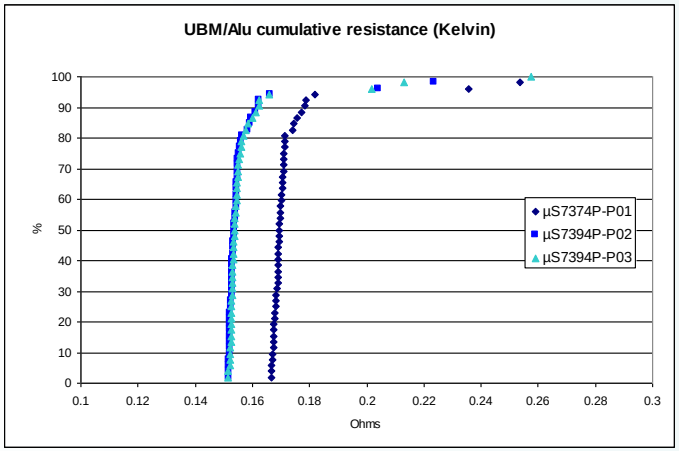
P01



P02



P03

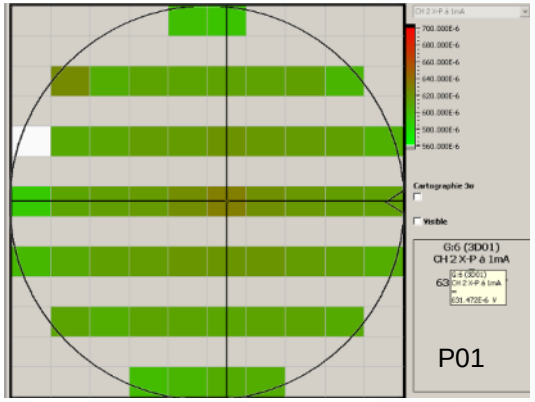


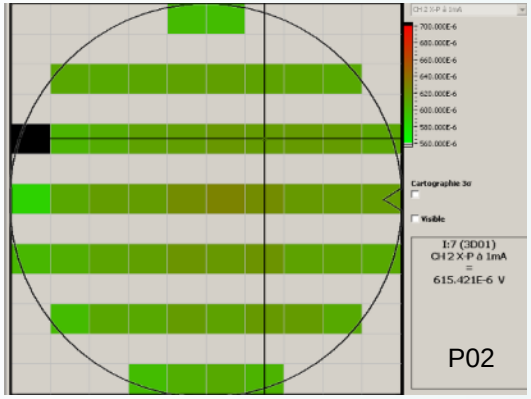
Cumulative resistance UBM/Alu
Mean value : ~ 150 mohms

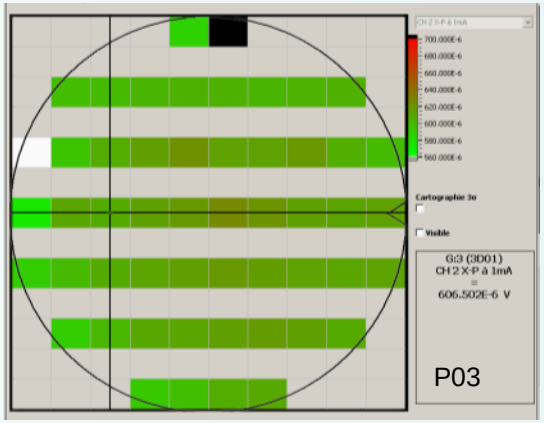
- **Conclusions:**
  - ☺ Isolation between UBM lines OK
  - ☺ Alu/UBM contact resistance is OK

Medipix 3 project results / electrical tests (non exhaustive)

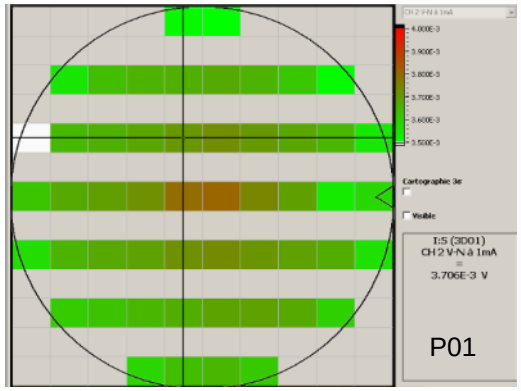
- **2 TSV chain resistance (by Vdd)** **1.23 Ω ± 3.6 % (1σ)**

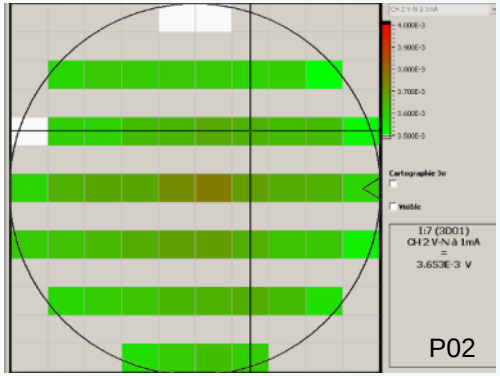


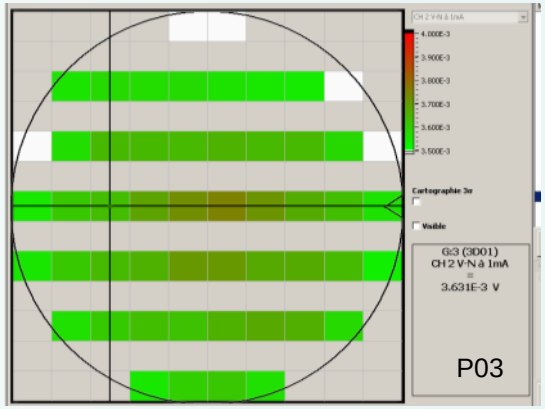




- **2 TSV chain resistance (by Vss)** **3.60 Ω ± 1.9 % (1σ)**







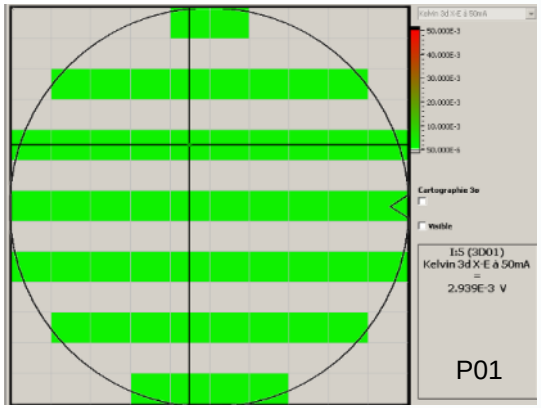
- **Conclusions:**

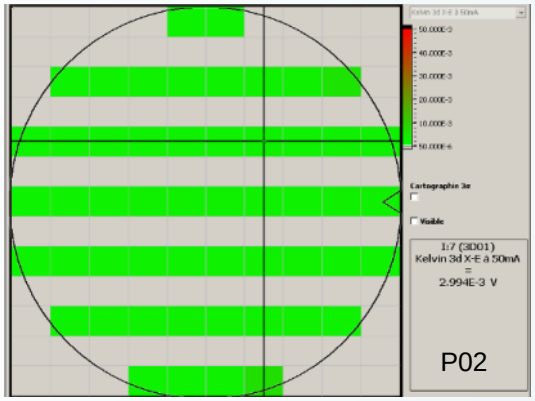
☺ Uniform distribution of values ➔ no comparizon with reference value possible

Medipix 3 project results / electrical tests (non exhaustive)

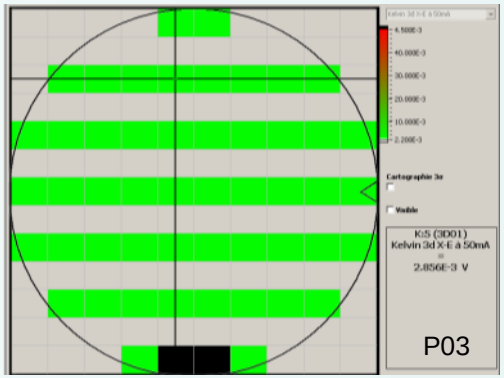
- **Kelvin TSV ➔ Mean value**

50 mΩ ± 14 % (1σ)



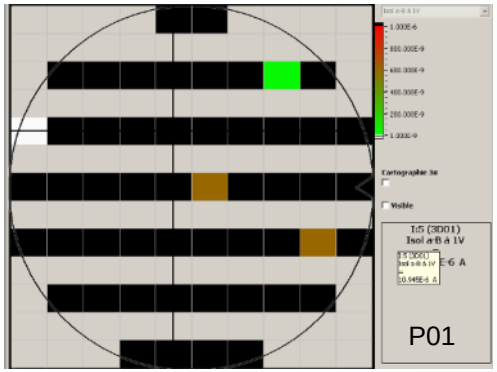


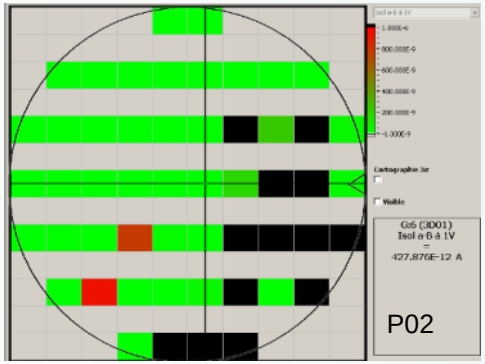
Kelvin3D (Specs < 1 Ohm/TSV) / Yield: 100%

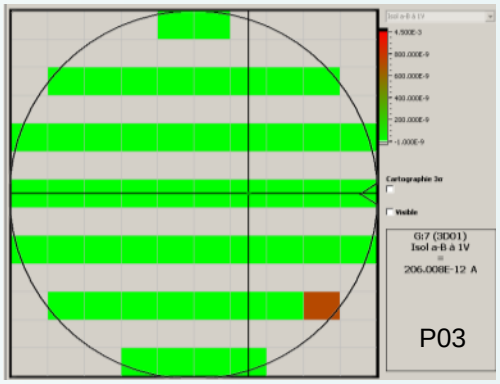


Kelvin3D (Specs < 1 Ohm/TSV) / Yield: 96%

- **Insulation between 2 TSV (1 connected TSV to M1 & 1 non connected) – Applied voltage : 1V**







- **Conclusions:**

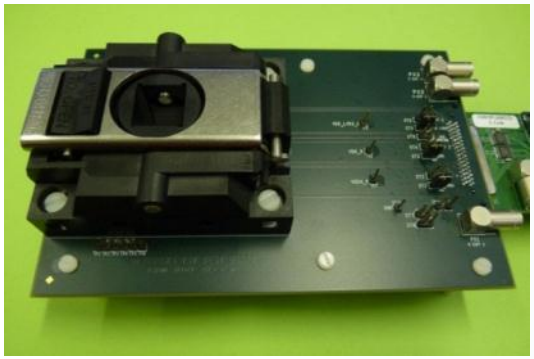
  Insulation issue on P01 & P02 / Root cause identified

  Correction on P03

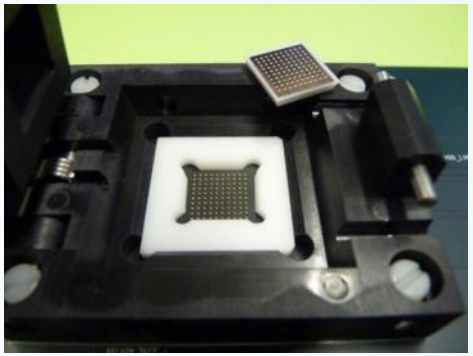
I_{leak} < 1 E^{-06}A

Medipix 3 project results – CERN electrical results

- Test set-up :
  - Test board realize the interface between Medipix3 chip and readout interface
  - Test socket is embedded on test board to establish contact to the bga pads of the chip
  - We are using a custom readout interface (USB) common to most of MEDIPIX chip family



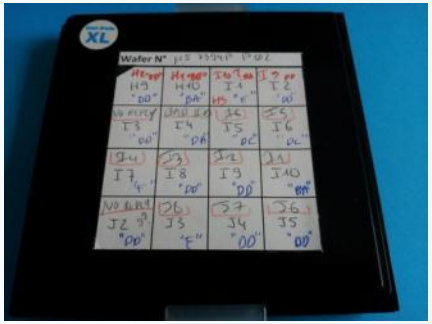
Test board



Test socket

Readout interface

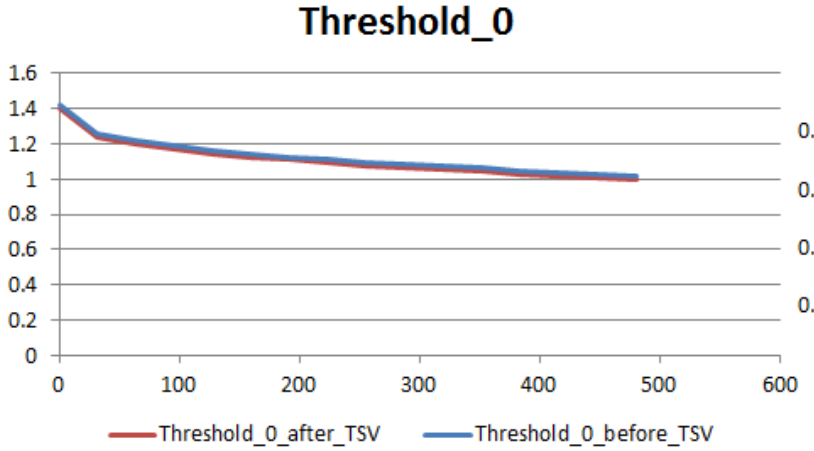
- Test samples
  - LETI sent a complete GELPAK of 16 diced chips. (DISCO dicing)
  - Parts are from IBM wafer # AZNW5VH, at CERN it was identified as Wafer # 24

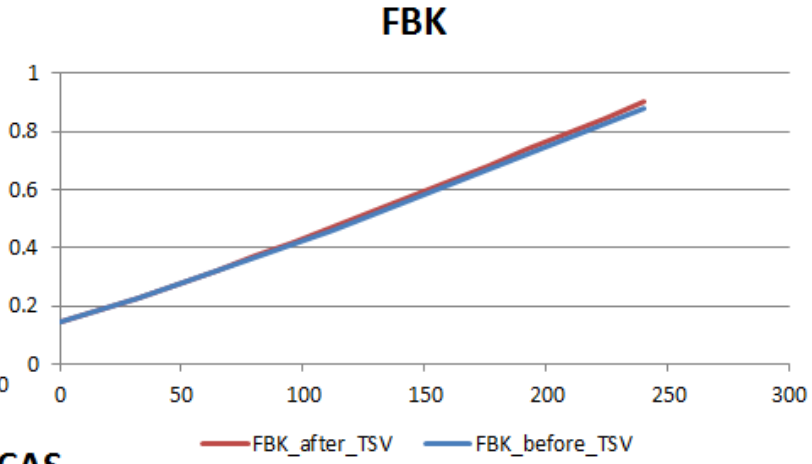


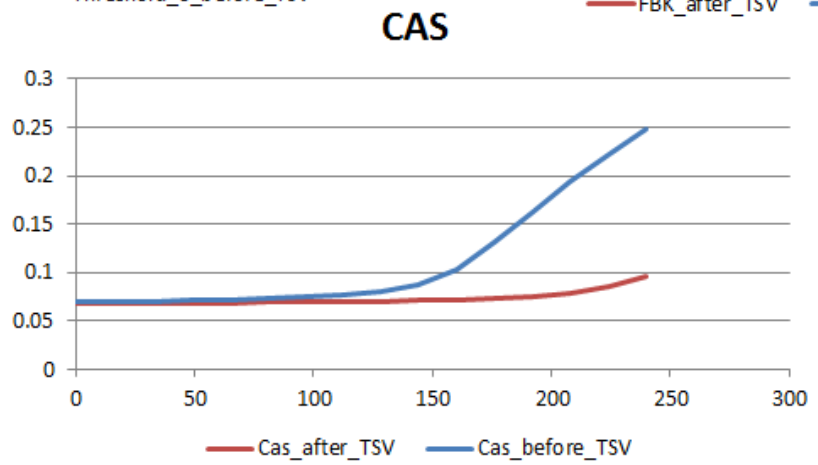
(Courtesy of Jerome ALOZY / CERN)

Medipix 3 project results – CERN electrical results

- W24-H2 DAC dependency





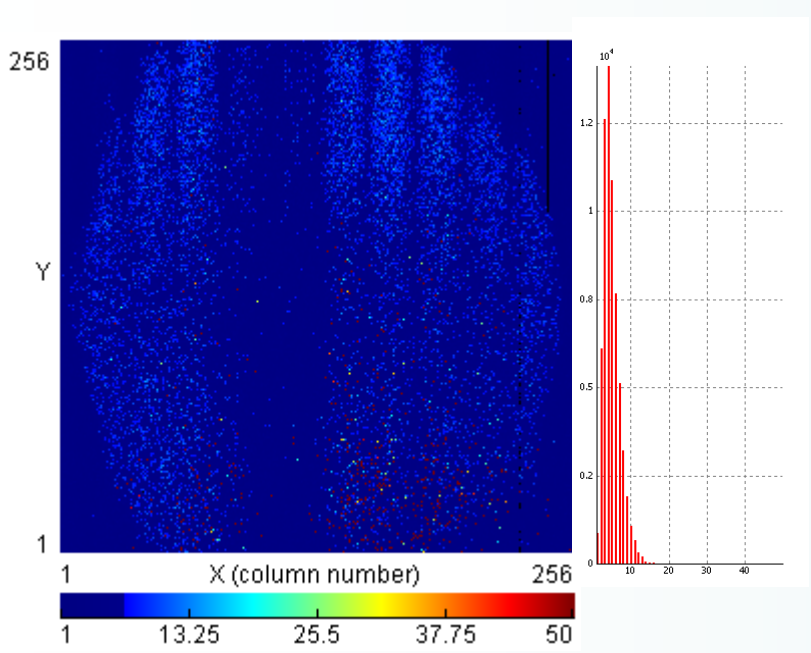


(Courtesy of Jerome ALOZY / CERN)

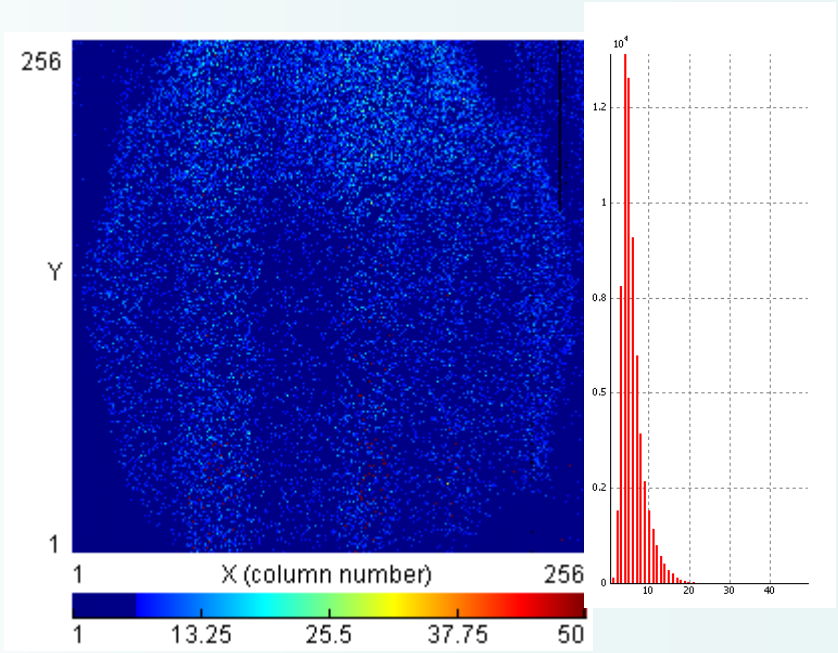
Chip H2 behaves as expected, only a small drift with DAC CAS is noticeable.

Medipix 3 project results – CERN electrical results

- W21-H2 Noise floor comparison
  - View of the complete matrix behaviour



Before TSV



After TSV

  - We could notice only a slight difference

(Courtesy of Jerome ALOZY / CERN)

Medipix 3 project results – CERN electrical results

- Conclusion on preliminary tests @ CERN (16 chips)
  - Result are really encouraging, again we have a limited number of samples to have good statistic and selected samples were not the one expected (for instance one class F was selected for electrical test). For me 10 device on 14 selected samples are functional and behave well.

			For stat.	OK
H2	OK		1	1
H1	OK		1	1
I10	BAD	to be checked visually	1	0
I9	OK but a bit noisy	to be investigated	1	1
I8?	BAD	to be checked visually	1	0
I7?	BAD	wronlgy seleceted class F sample	0	
I6	OK		1	1
I5	OK		1	1
I4	BAD	already bad during wafer probing	0	
I3	BAD	to be checked visually	1	0
I2	OK		1	1
I1	OK		1	1
J9?	BAD	to be checked visually	1	0
J8	OK		1	1
J7	OK		1	1
J6	OK		1	1
			14	10

(Courtesy of Jerome ALOZY / CERN)

Medipix 3 project perspectives

- Tests of 84 new chips coming from wafer 02 ➔ On going @ CERN
- Assembly of detectors on ROIC @ VTT ➔ on going
- Dicing process implementation @ LETI
- One wafer stored @ LETI ➔ optimized wafer for detector assy

- Dissemination aspects :
  - 3 common papers (CERN / LETI) in 2012 : Minapad / ISCDG / ESTC
  - 1 abstract accepted to ECTC 2013

- Project starting with new design (Medipix RX ?)

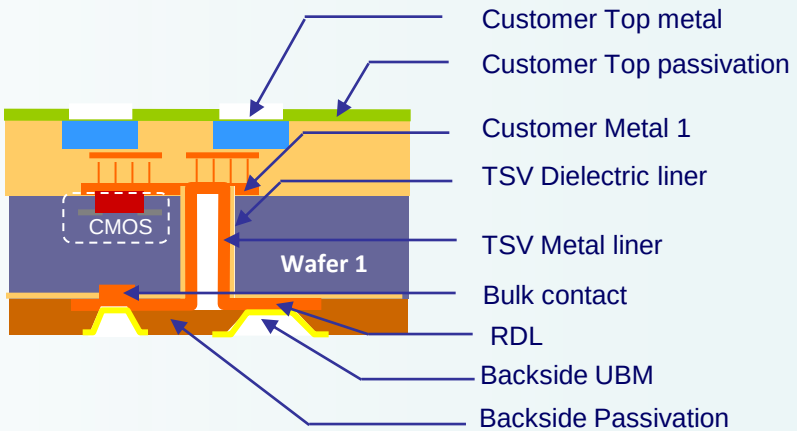
Outline

- Introduction
- Medipix 3 project status
- **3D Technological toolbox @ LETI**
  - **Available technologies / short term projects**
  - Technological modules developments / Mid & long term projects
  - Products examples
- Conclusions / prospects

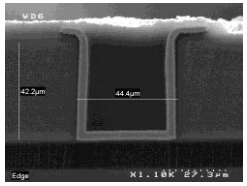
Available technologies : TSV + RDL

TSV & RDL DRM & schematic

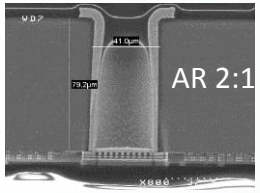
- Wafer size : **200 & 300 mm**
- TSV type : **via last / Cu liner**
- Minimum pitch : **60 µm**
- TSV diameter : **30 to 100 µm**
- Aspect Ratio (AR) : **from 1:1 to 3:1**
- RDL material : **Cu / protective layer possible**
- RDL thickness : **1-10 µm**
- RDL minimun width : **20 µm**
- RDL minimun space : **20 µm**



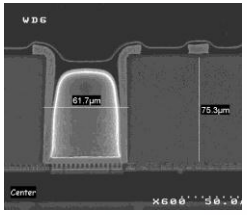
TSV & RDL morphological results

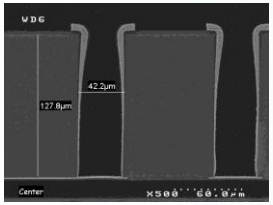


AR 1:1

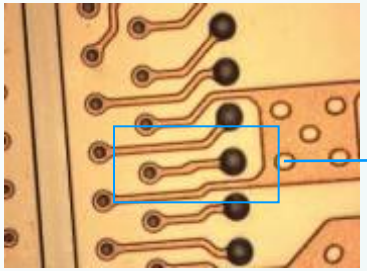


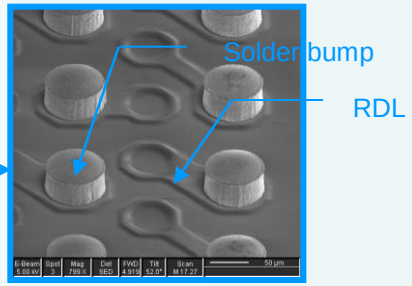
AR 3:1





Cu RDL integration : pillars on RDL + passivation

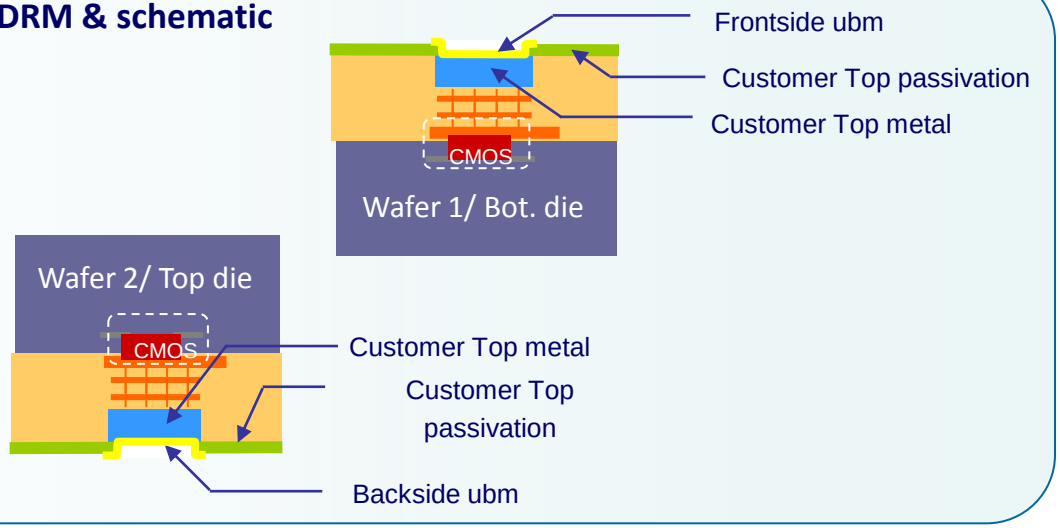




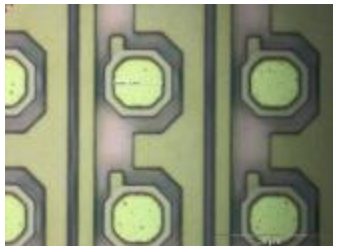
Available technologies : Under bump metallurgy (UBM)

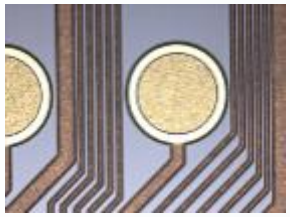
UBM DRM & schematic

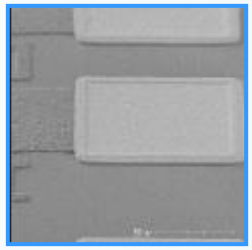
- Wafer size : **200 & 300 mm**
- UBM material : **TiNiAu**
- Possible on frontside and / or backside of the components
- UBM thickness : **0.5 – 1.5 µm**
- UBM width : **20 – 800 µm**
- UBM minimun pitch : **40 µm**



UBM results

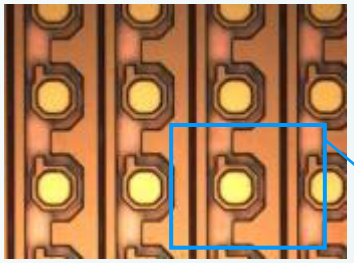






Available technology :

- Metal sputtering / thickness range : 0.5 – 1.5 µm



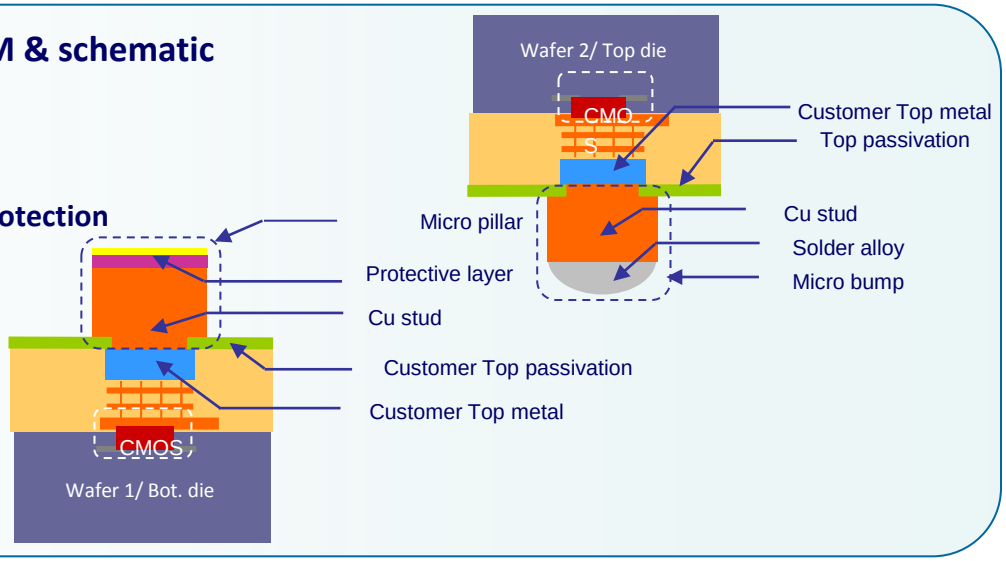
Different shape possible :

- Square
- Polygons
- Circle

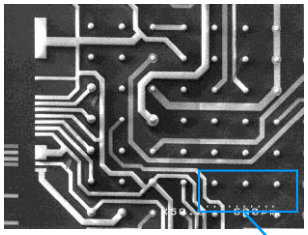
Available technologies : Micro bumps & micro pillars

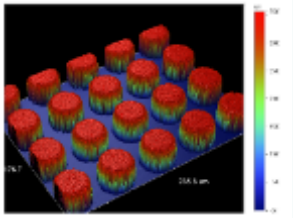
Micro bumps & micro pillars DRM & schematic

- Wafer size : **200 & 300 mm**
- Micro-bumps material : **Cu post / (Ni) / SnAg solder**
- Micro pillar material : **Cu post / Ni / Au or SnAg protection**
- Minimum pitch : **50 µm**
- Micro-bumps diameter : **25 µm**
- Micro pillars diameter : **25 µm**
- Micro-bumps thickness : **20 – 35 µm**
- Micro pillars thickness **:** **8 – 15 µm**

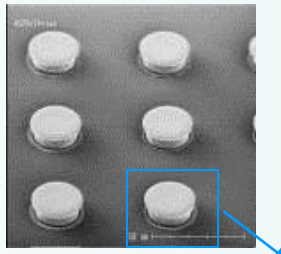


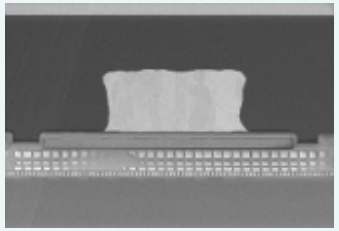
Micro bumps & micro pillars morphological results



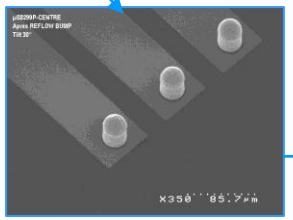


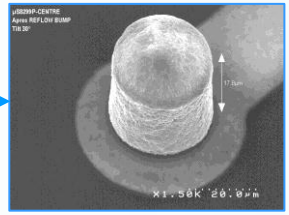
Micro-bumps characterization



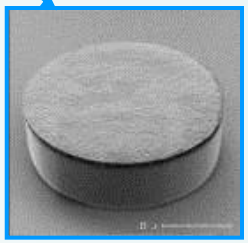


Micro-bumps after reflow





Micro pillars with protective layer

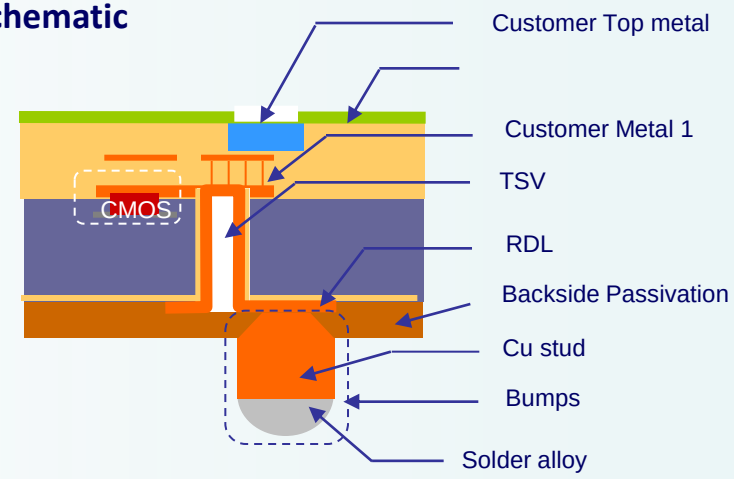


Micro pillars on top metal

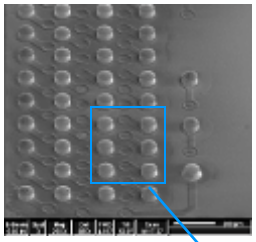
Available technologies : bumps & pillars

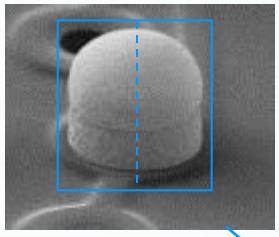
Bumps & pillars DRM & schematic

- Wafer size : **200 & 300 mm**
- Pillars material : **Cu stud / (Ni) / SnAg solder**
- Minimum pitch : **100 µm**
- Pillars diameter : **50 – 100 µm**
- Pillars thickness : **50 – 80 µm**



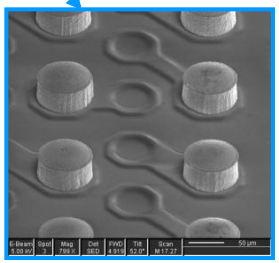
Bumps & pillars morphological results

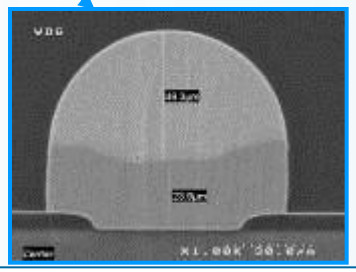


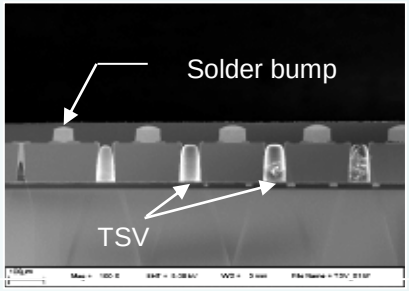


Bumps cross section

Bumps





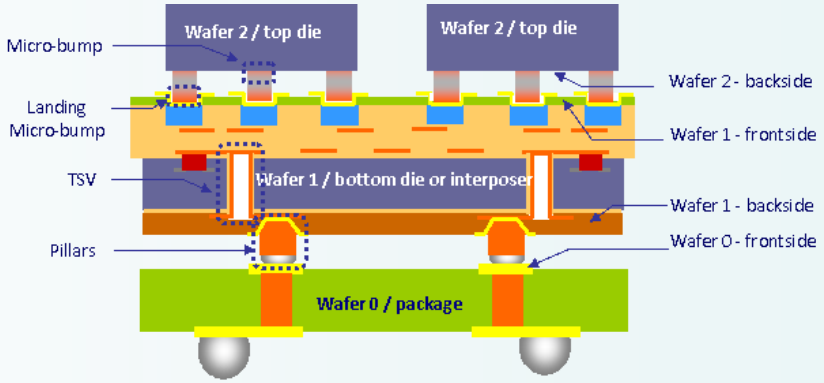


Pillars integration with TSV

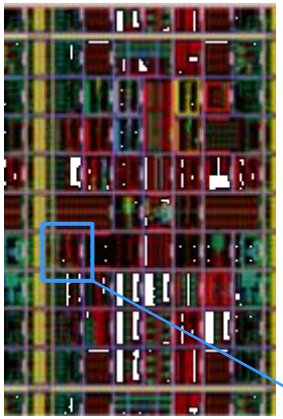
Available technologies : 3D electrical tests / reliability

Electrical test approach

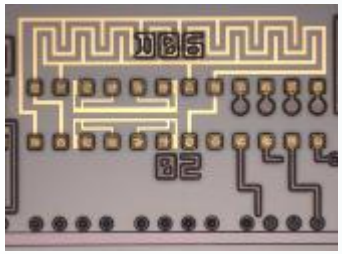
- Electrical tests at each level
- Specific structures for 3D technologies
- Non invasive structures into dicing lines
- Using of Standard probe cards
- Data exploitation tool

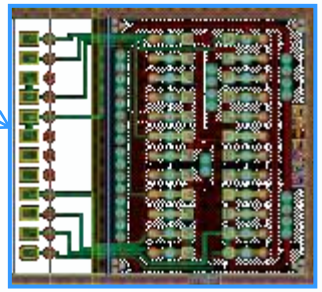


Electrical test results & tools

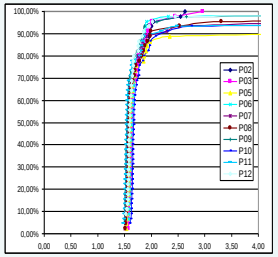


3D tests structures

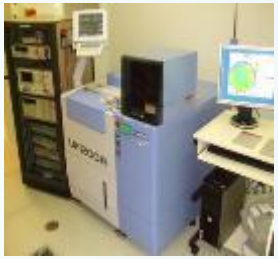




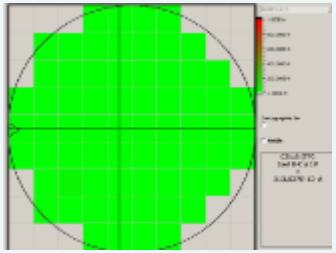
Probe card



Electrical test results



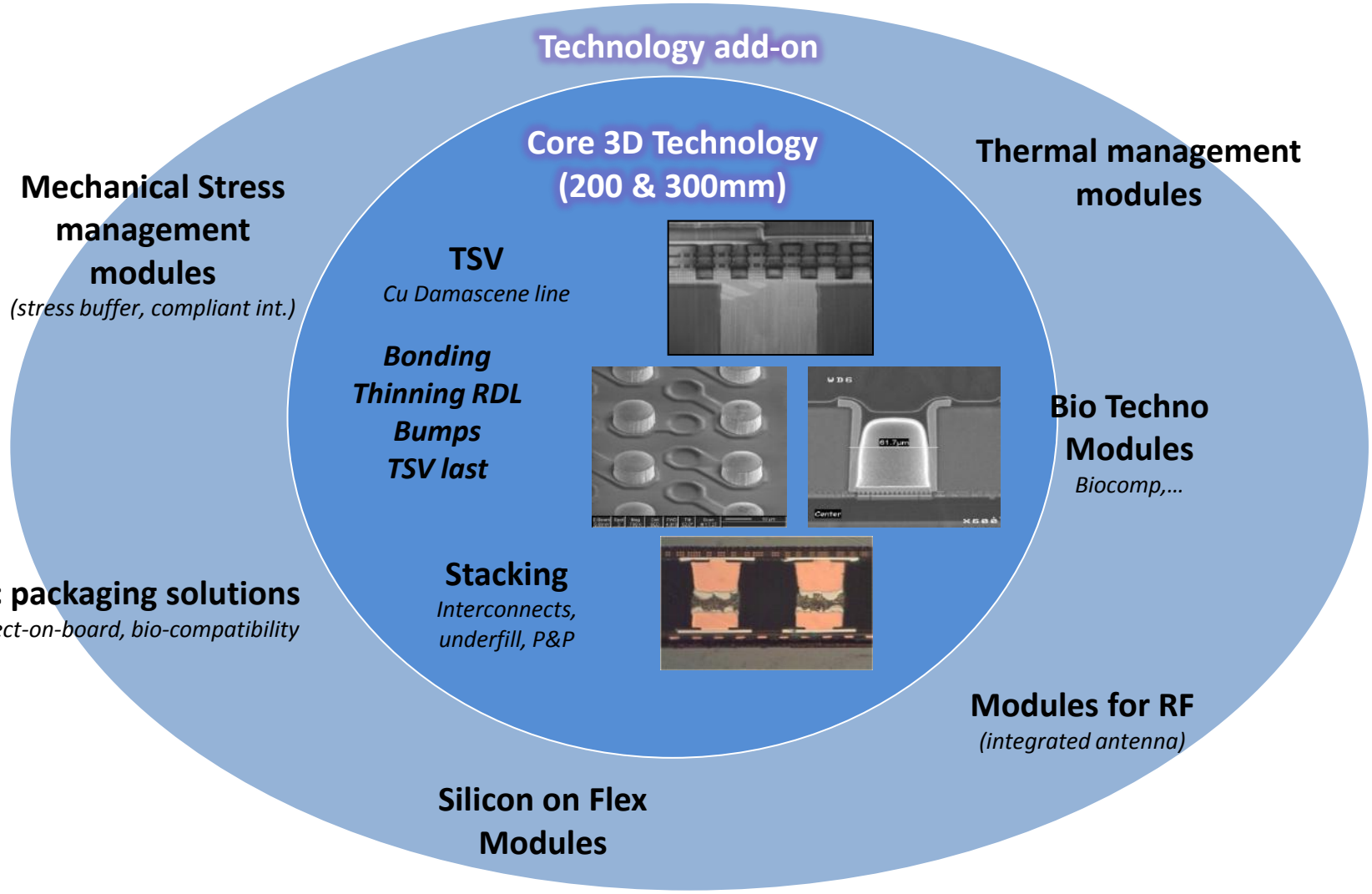
Electrical test tool



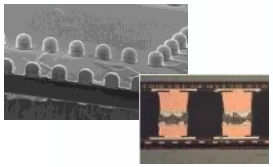
Outline

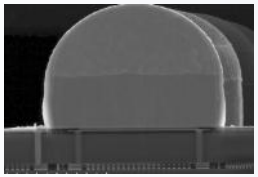
- Introduction
- Medipix 3 project status
- **3D Technological toolbox @ LETI**
  - Available technologies / short term projects
  - **Technological modules developments / Mid & long term projects**
  - Products examples
- Conclusions / prospects

Technological developements

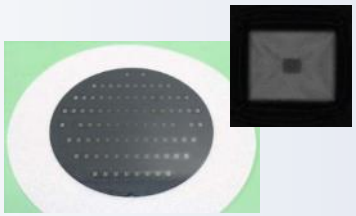


Technological developements

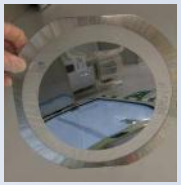


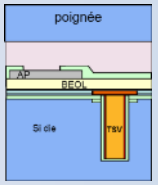


µ-bumps and SAC copper pillars

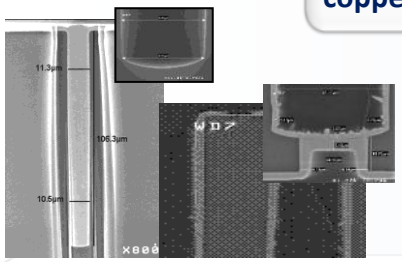


Molding & underfilling





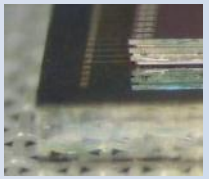
Temporary bonding on 100 µm thk 200mm wafer including small or large copper pillars



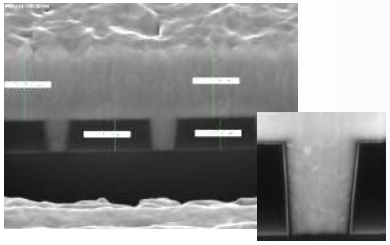
Through Silicon Via (TSV). Cu filled. AR3-10

3D

INTEGRATION



F2F and B2F Thin die stacking (30um thk). Conformal routing

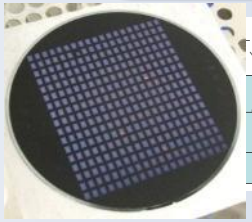


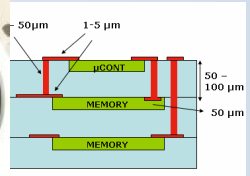
2 to 4 layers routing Damascene thick Copper Routing on organic

Thinning 80 – 100 µm

Internal stress monitoring

Warp management





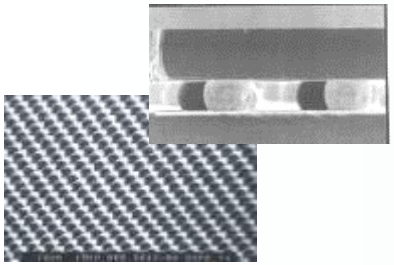
Organic/silicon rebuilt wafer

Routing and via (TPV)

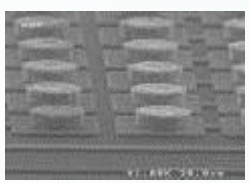
Strata stacking and connecting

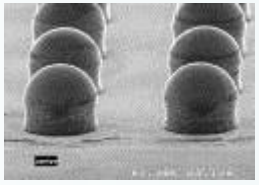
Tech.dev. : die to die interconnects

From solder balls to Cu-Cu bonding → A wide range of interconnections

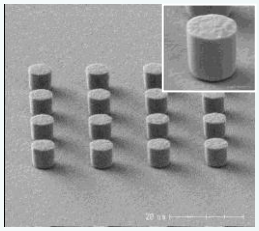


Classic Flip chip (Ball or stud bump)

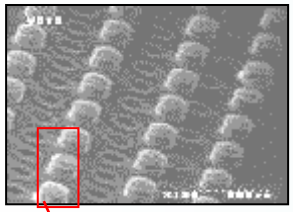


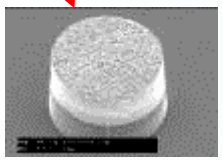


µbumps / µpillars SLID / TLP

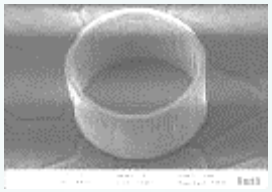


Solder-free µinserts

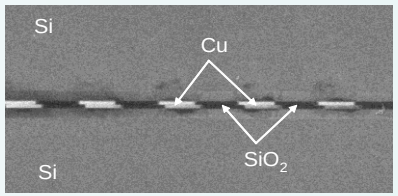




> 100 µm C2S pillars



µtubes in SAC



Cu-Cu Direct bonding

100-30 µm range

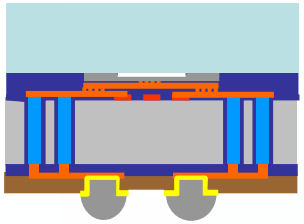
30-10 µm range

Down to 5 µm

Pitch reduction

Tech.dev. : TSV families

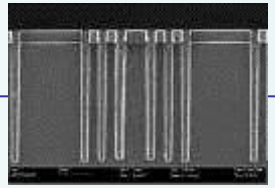
TSV First (Polysilicon filled)



Polysilicon filled

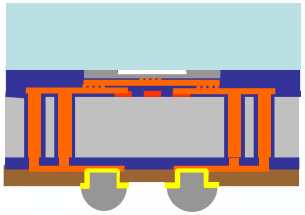
TSV first for medical applications

SOI substrate, High voltage



Trench AR 20, 5x100µm

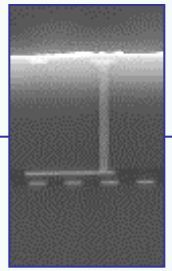
TSV Middle (Copper or W filled)



Cu filled

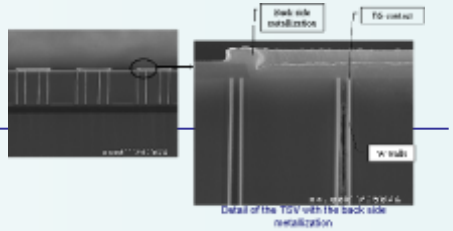
Best flexibility in layout and design

Higher density of I/Os



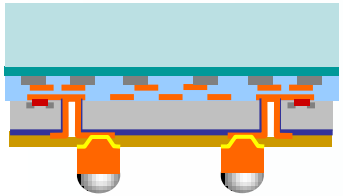
AR 7 , 2 x 15µm

AR 10, 10x100µm



W filled

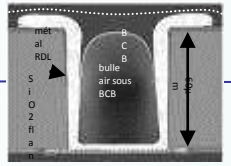
TSV Last (Copper liner or filled)



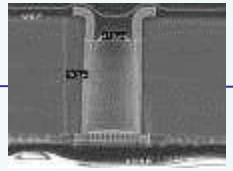
High density (<10⁴/mm²), Cu filled

Mid density (<200/mm²), Cu lined

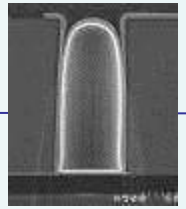
Minimal impact on circuit layout



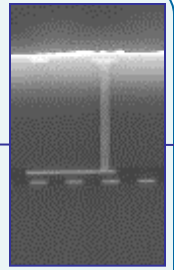
AR 1 80x80µm



AR 2, 60x120µm



AR 3, 40x120µm

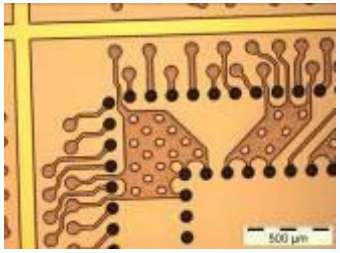
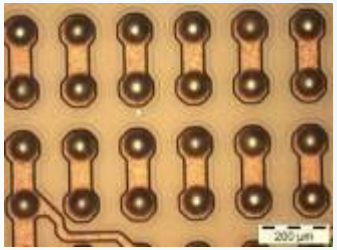
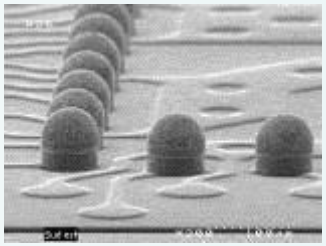


AR 7 , 2 x 15µm

Tech.dev. : RDL & Board connections

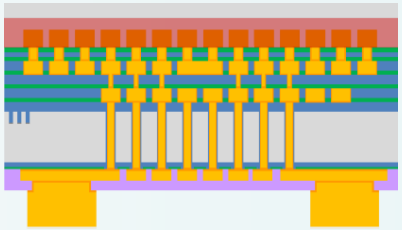
Two families of RDL with different targets and application fields

Cu RDL with organic passivation layer

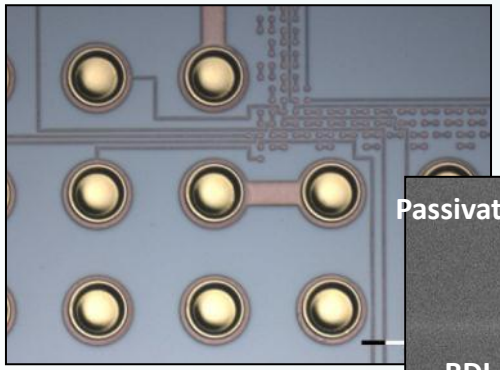
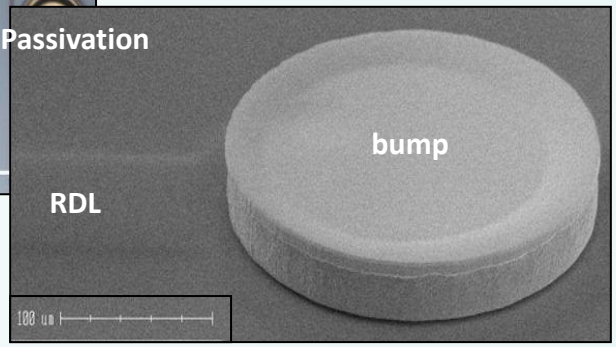





Few µm's of Cu (1 – 10 µm), Polymers for IDL

Cu RDL (Damascene) with inorganic passivation layer



- RDL
  - **L/S=10µm**
  - Organic passivation by spin coating
- Large bumps
  - **Ø250µm and 500µm pitch pillars**
  - Cu/Ni/Au electroplating
  - Stripping, seed layer wet etch
  - Total thickness 70µm

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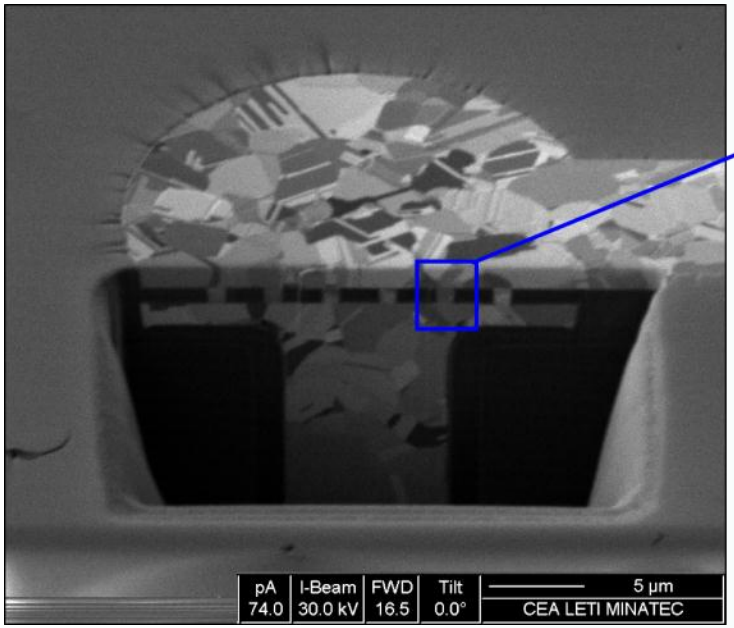
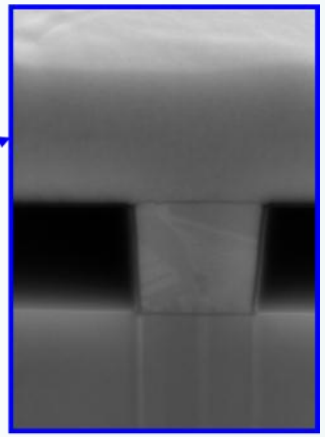
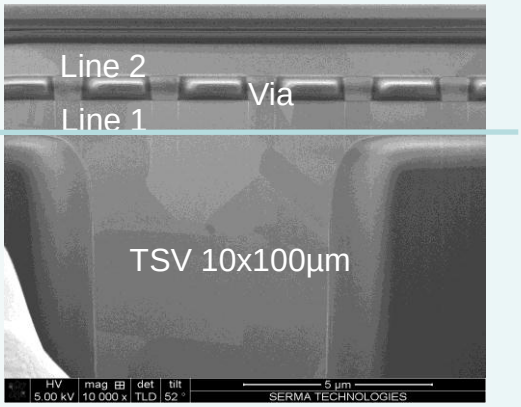
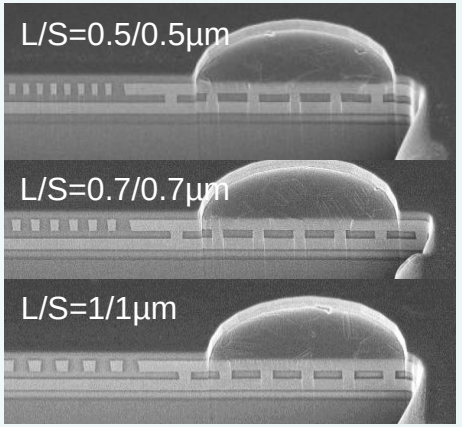
Tech.dev. : Front side routing

- Dense routing 0.5/0.5µm
- Cross section after Line 2 copper Chemical Mechanical Polishing
- TSV integration with thick (>1µm) Line 1 – Via – Line 2 damascene levels
- Full integrity of via: no extrusion









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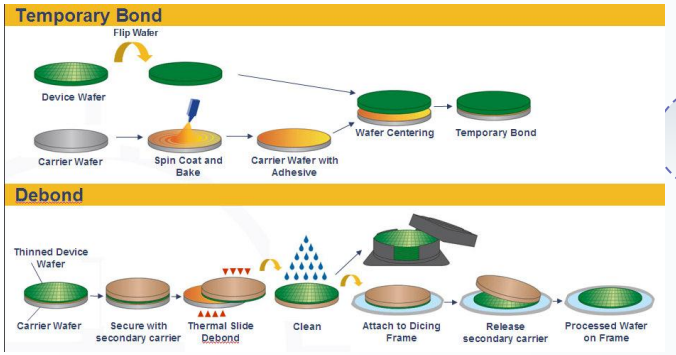
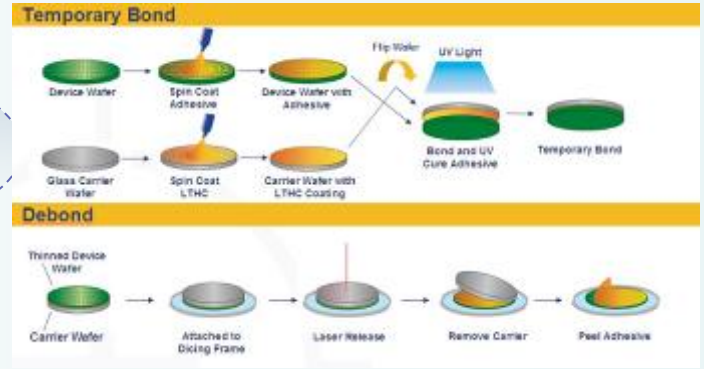
Tech.dev. : temporary bonding

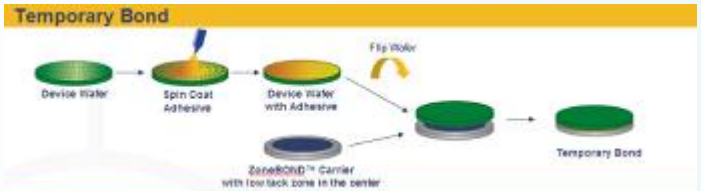
- **Temporary bonding main challenges**
  - High temperature compatibility
  - Low temperature debonding
  - Wet processes compatibility
  - Mechanical resistance : grinding & polishing



Possible approaches



Slide off



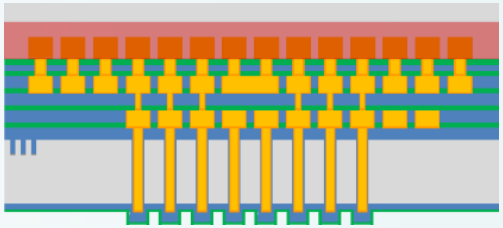
UV release

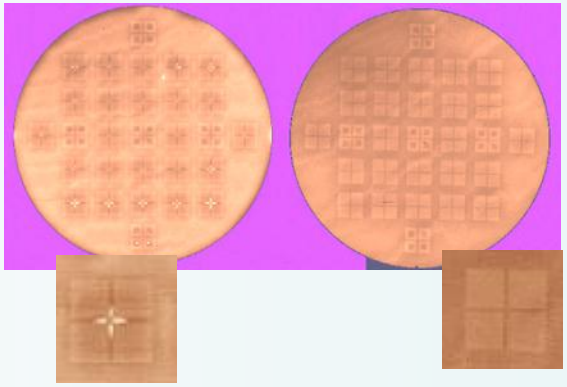
Zone bond

Source : M. Gabriel / Suss Microtec / EPTC 2010

Tech.dev. : temporary bonding & thinning

- **Temporary Bonding / slide off technique**
  - HT10.10 glue / 19µm thick
  - Scanning acoustic microscopy (SAM)
- Mechanical grinding
  - Thinning to 100µm
  - Edge trimming
- Silicon CMP





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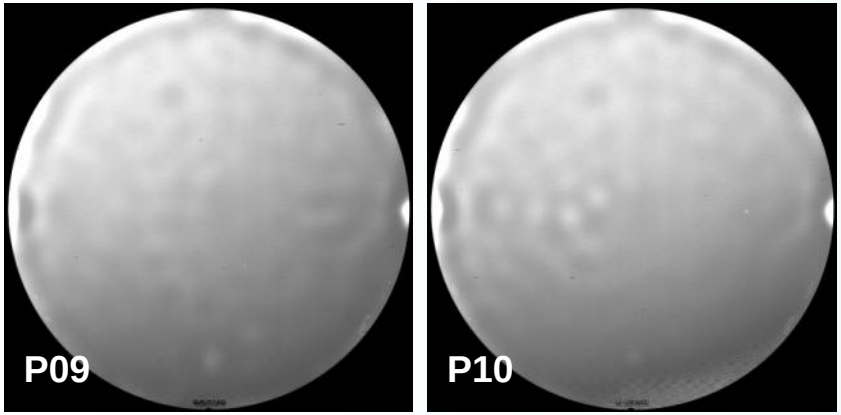
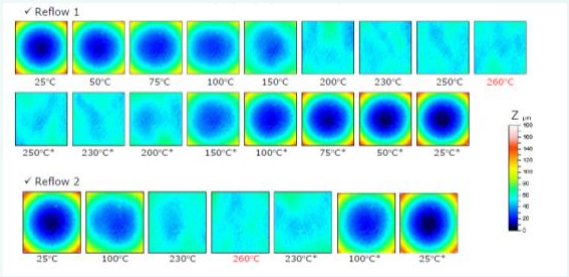
- **Temporary Bonding / ZB & UV techniques under developments**

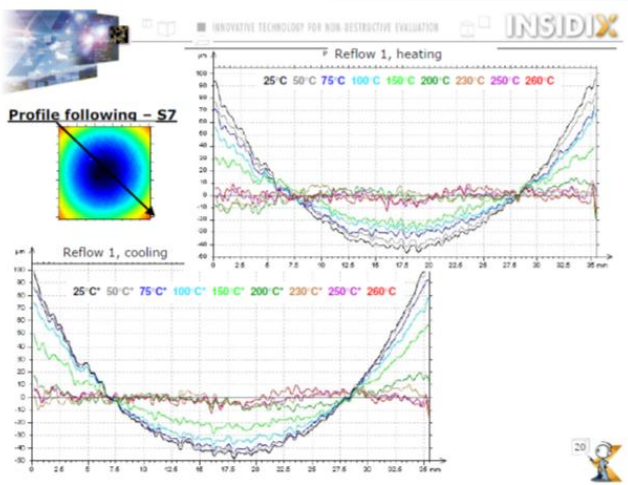


ZB bonding / SAM inspection on full wafers

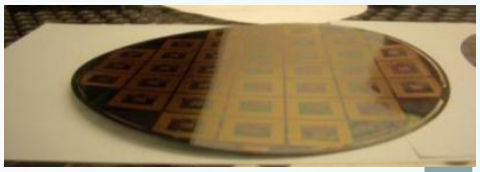
Tech.dev. : Stress management

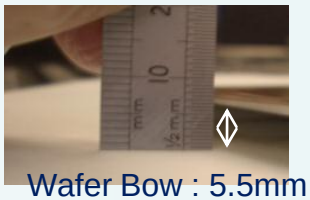
- **Objectives : to compensate the stress of the chip in order to be able to :**
  - Thin the chips until “ultimate” thickness (< 50 µm)
  - Assembly the chips on another chip without connections defectivity ➔ bending effect
  - Identification of the characterization method
- **Preliminary trials on going :**
  - TDM method ➔ Topography & deformation measurement under thermo mechanical load
  - Full field technique / Optical deformation measurements
  - Resolution : +/- 3µm
  - Temperature scanning
  - First experiment with stress compensation layers

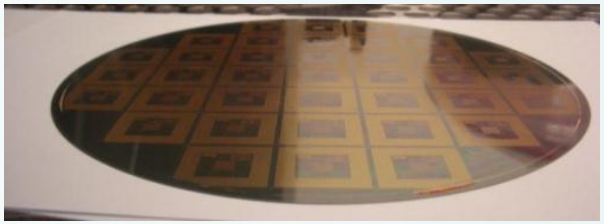




Standard process



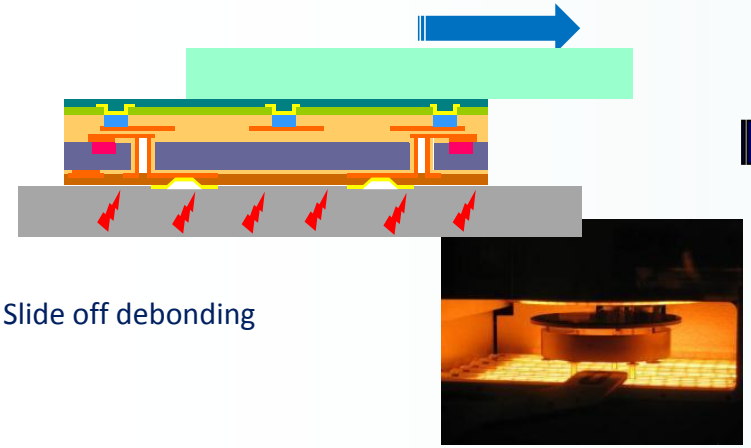




Compensation stress layers process

Tech.dev. : Debonding

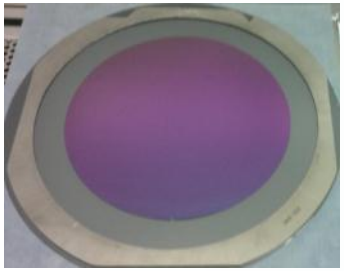
- **Debonding / slide off technique**
  - High temperature (200°C) + slide off



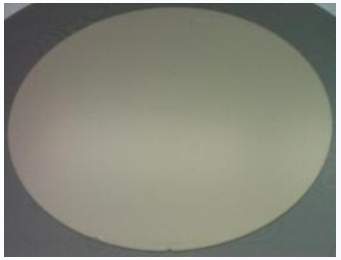
Slide off debonding

Cleannig + taping

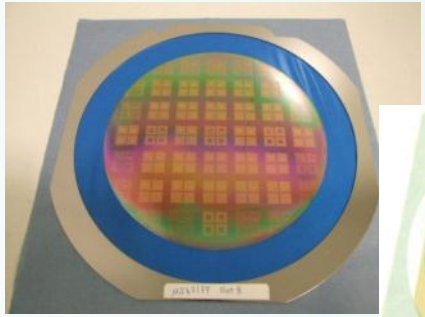
- **Debonding / ZB technique**
  - Glue chemical dissolution + pull in



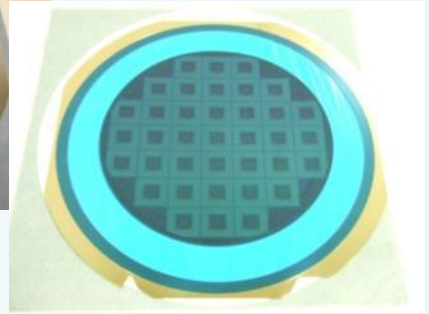
Device on tape



Carrier (reusable)



Front side



Back side

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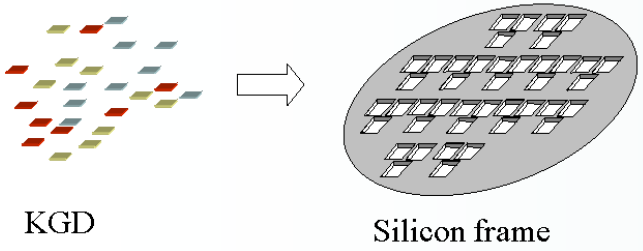
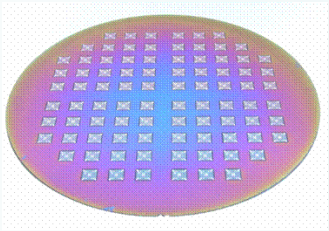
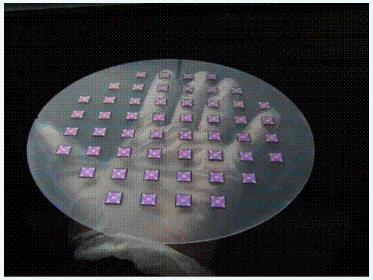
Tech.dev. : Rebuilt wafers

Embedded chips in silicon

- Rebuilt wafers: CIWIS approach (Chip In Wafer for Integrated System)
- Deformation minimized (Low warpage) : high litho resolution
- Wafer fully compatible with classical silicon processes
- Higher temperature compatibility
- Process compatible with Si & glass frame

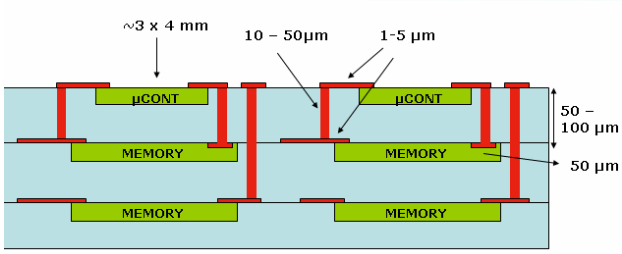


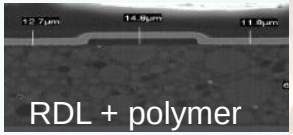

Chip in Silicon Wafer

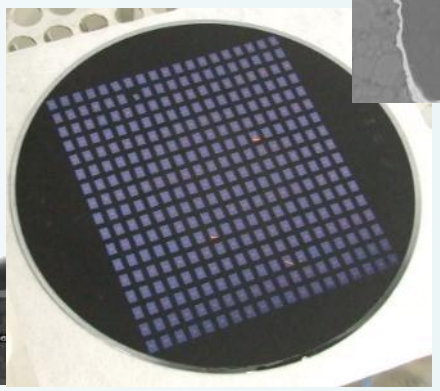

Chip in Glass Wafer

Embedded chips in polymer

- multi-die embedded in organic wafer with via and routing
- die attach on tape + carrier / molding
- Through Polymer Via connecting (TPV) / routing
- hybrid wafer warp monitoring / control
- Waferlevel multi-strata stacking

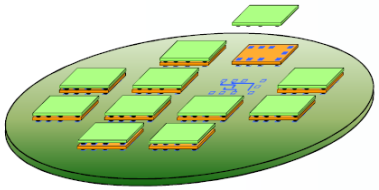


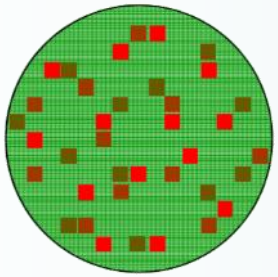


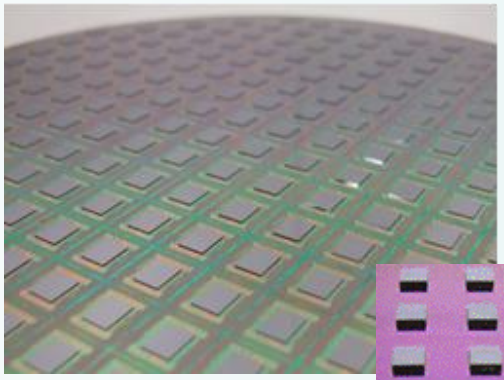


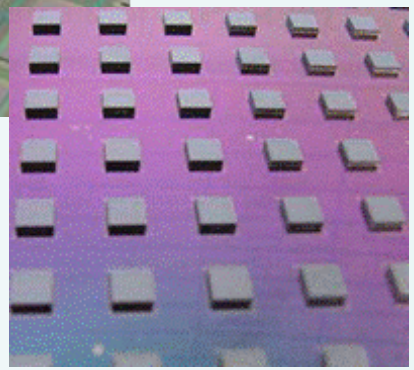
Tech.dev. : Chips stacking

- **Two approaches for components stacking**
  - Chip to wafer
    - High speed / low accuracy (+/- 3µm)
    - Low speed / high accuracy (+/- 0.5 µm)
  - Wafer to wafer









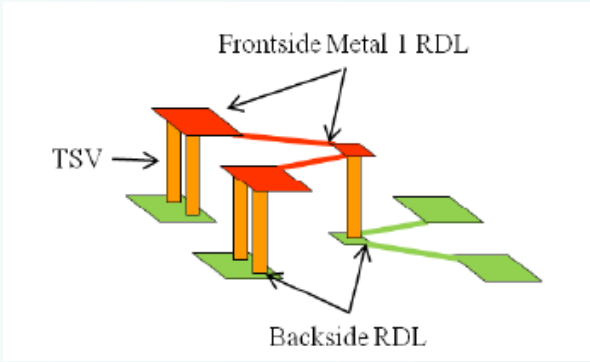
SET FC 300

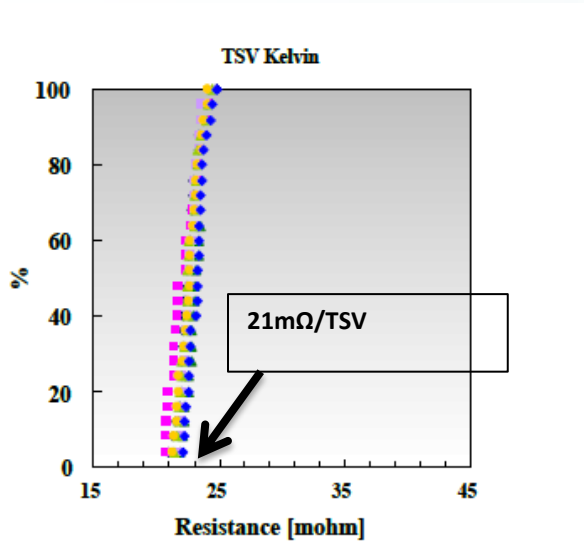
Datacon

Source : Panasonic

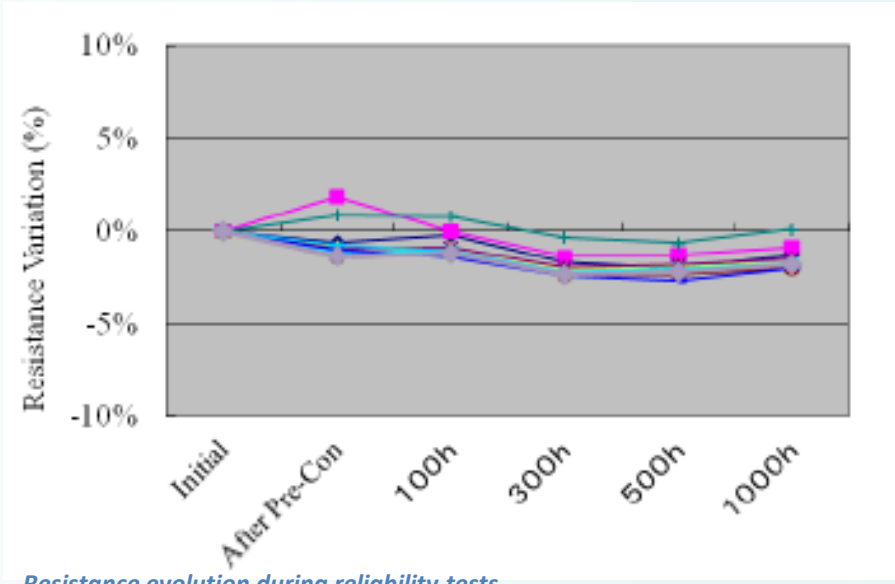
Tech.dev. : electrical tests & reliability

- Specific patterns developments for electrical tests
- Reliability :
  - Environmental tests ➔ TCT / HTS / HAST
  - Electro-migration





Reliability Test	Condition
Pre Conditioning	bake 125C, 24hrs, MSL-3 30C, 60%, 192hrs, Rreflow 260C x 3times
Temp. Cycle (TC)	-55C-125C, 1000cycle
High Temp. Storage	125C, 1500hrs
HAST	110C, 85%, 3V, 1000cycles



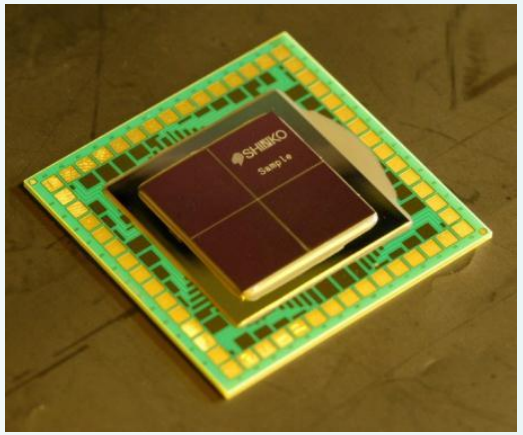
Resistance evolution during reliability tests

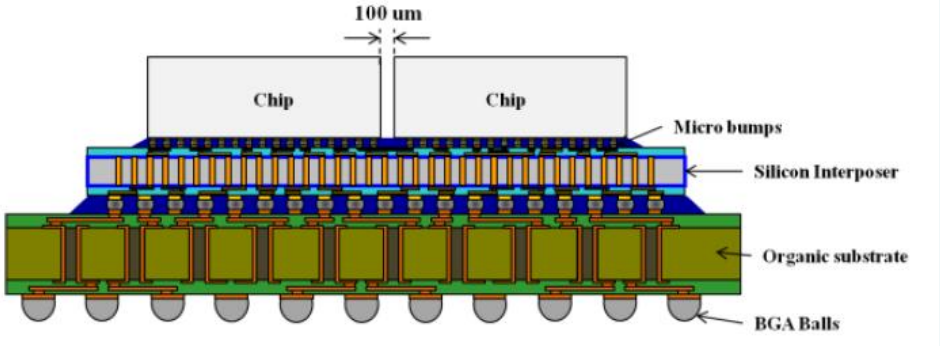
Outline

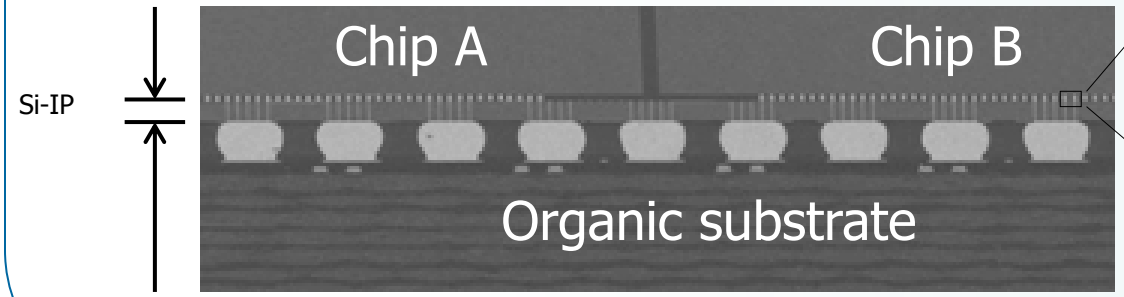
- Introduction
- Medipix 3 project status
- **3D Technological toolbox @ LETI**
  - Available technologies / short term projects
  - Technological modules developments / Mid & long term projects
  - **Products examples**
- Conclusions / prospects

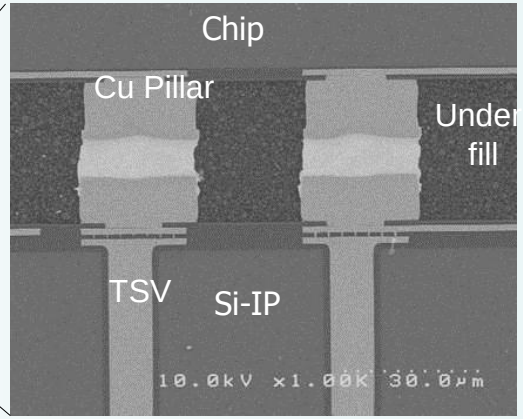
Product example : Passive interposer

- Features
  - Cu TSV, AR10
  - 2 to 4 layers routing, Damascene thick copper, L/W 0.5/0.5 x 1.4µm
  - Temporary bonding
  - Thinning, Stress Monitoring, Warp Management



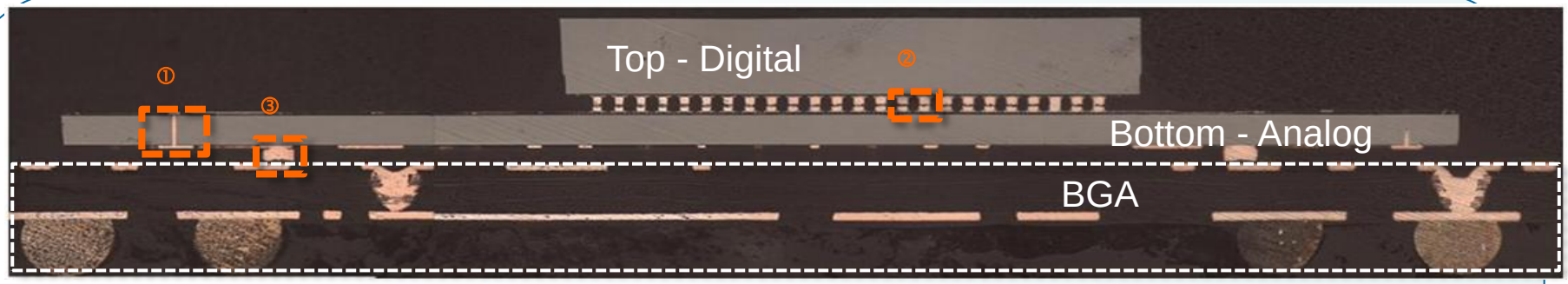


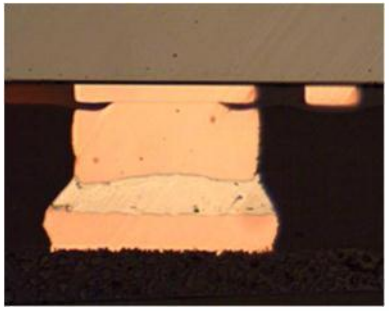




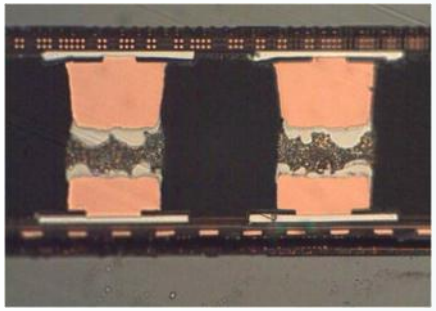
Ken Miyairi, Masahiro Sunohara, Jean Charbonnier et al, IMAPS, San Diego 09/2012

Product example : Active interposer

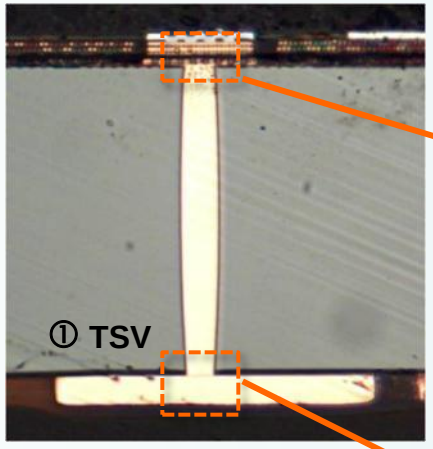


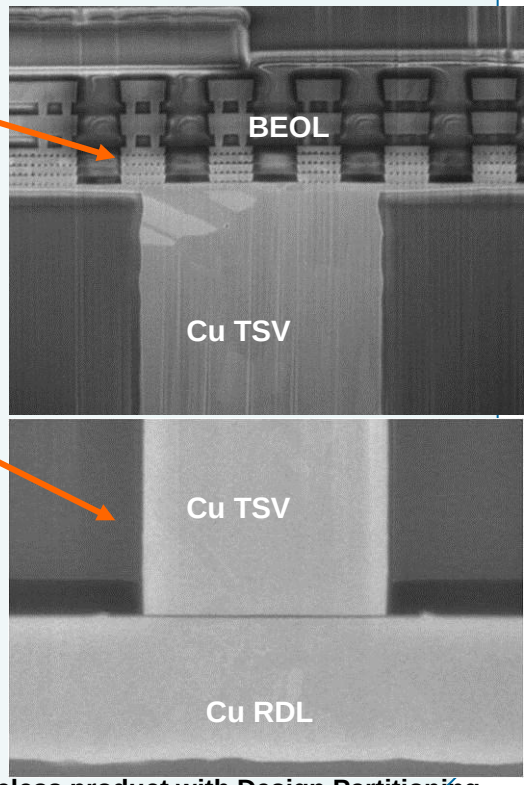


③ Die - BGA connection



② Die - die connection

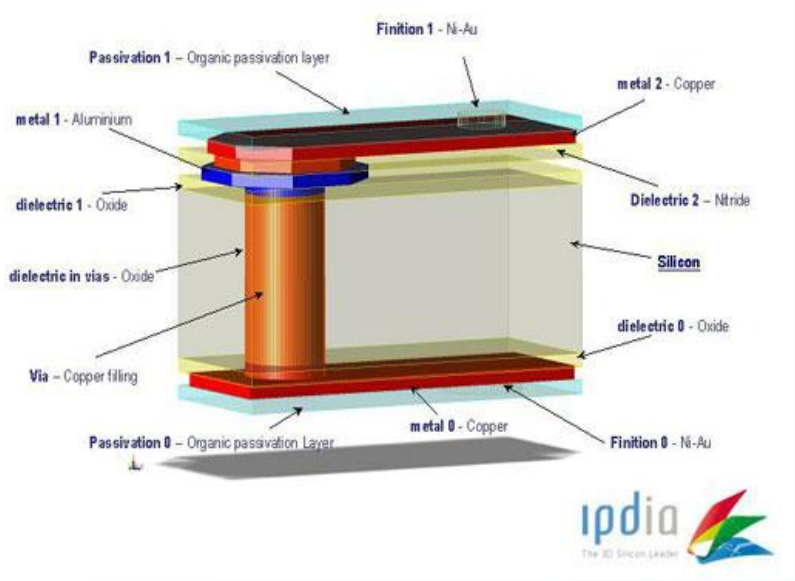




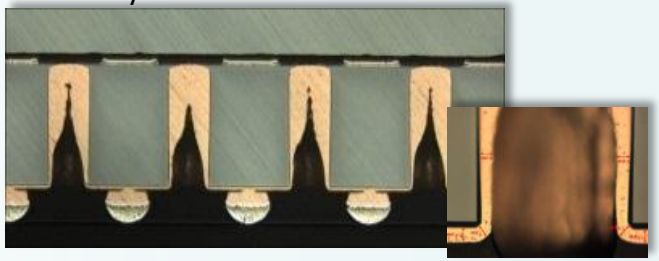
- **Wide I/O**
  - SDRAM JEDEC memory standard released Jan. 2012
- **TSV's**
  - Ø 10 µm, AR 8, Pitch 40 µm, Number 1016
  - Compatible with FD-SOI
- **Chip to Chip Cu Pillars**
  - Ø20 µm, Height 20 µm, Pitch 40 µm, Number 1016
- **SoC to Substrate Cu Pillars**
  - Ø55 µm, Height 40 µm, Pitch >200 µm, Number 933
- **FBGA Package**
  - Size 12x12mm, Ball Pitch 0.4mm,Ball Matrix 29x29, 1.2 mm thickness

3D Integration of a Wireless product with Design Partitioning
G. Druais et al., 3DIC 2012

Product example : Ultra thin 3D capacitors stacking

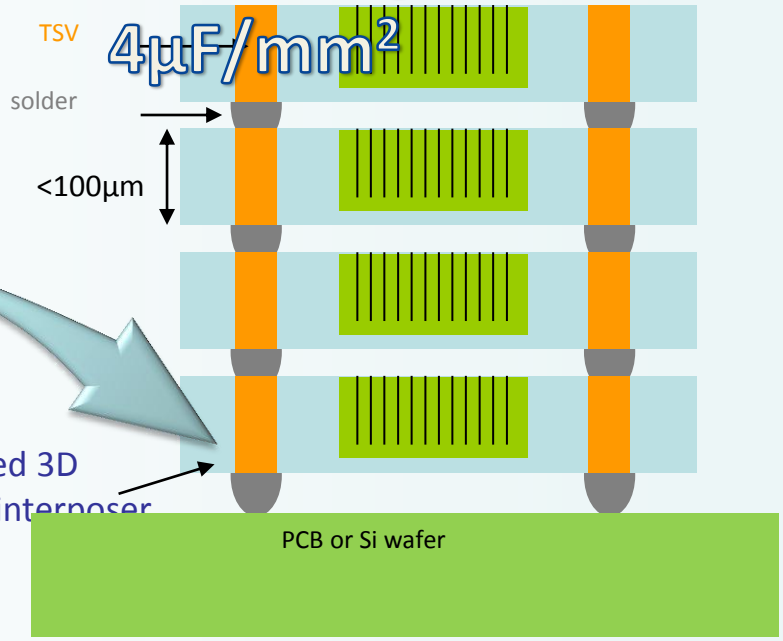


Courtesy of IPDIA



Sample of IPD of 250nF/mm2 thinned at 60µm

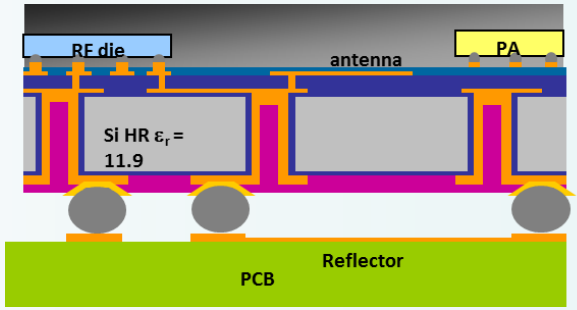
Stack target:
4µF/mm²



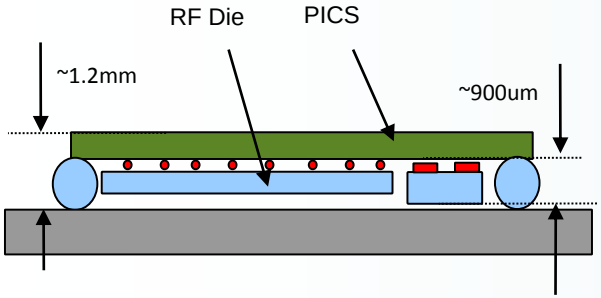
Low profile 3D-IPD for Advanced Wafer Level Packaging
S. Bellenger,et al.IMAPS Miniapad 2011

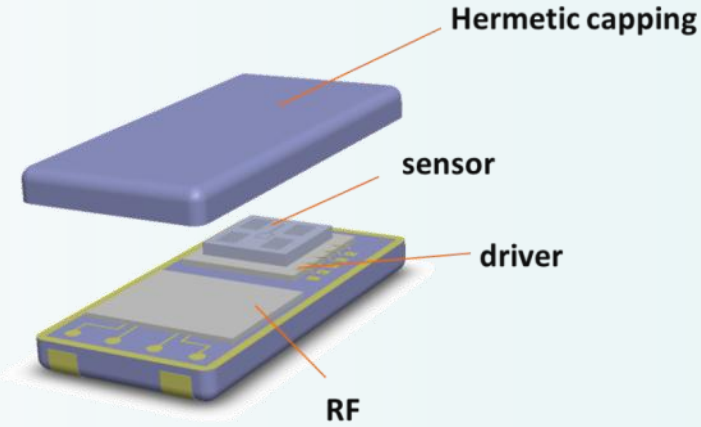
Product example : Other products in development @ LETI

- Smart interposer for RF application
  - Mobile
  - Automotive
  - Telecom
  - Defense / space

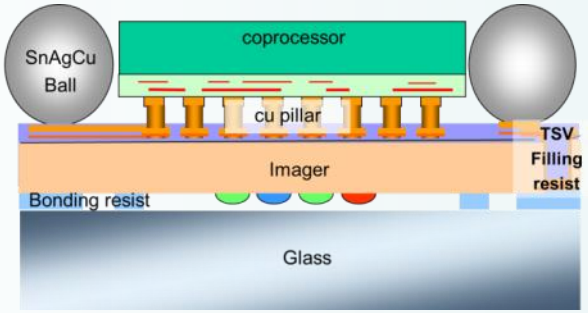


- Smart interposer for medical :
  - Implantable system





- 3D Imager
  - Visible imager + coprocessor
  - Packaging : BGA



Outline

- Introduction
- Medipix 3 project status
- 3D Technological toolbox @ LETI
  - Available technologies / short term projects
  - Technological modules developments / Mid & long term projects
  - Products examples
- **Conclusions / prospects**

Conclusions / Prospects

- Conclusions :
  - LETI has a very long experience in 3D technologies developments
  - We applied successfully our technologies on the wafers of the Medipix 3 project
  - Generally speaking, the philosophy of the 3D developments @ LETI is :
    - To create a technological toolbox supporting by R&D projects
    - To applied those technologies on our customer products
    - To open the “already developed” technologies for other customers
    - To collaborate with material & equipment suppliers in order to access to advanced tools & materials

- Prospects :
  - To fill our toolbox with new technological modules by using new collaboration and R&D projects
  - To Open our technologies access through our Open 3D™ platform

Leti

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