LHCb Upgrade Electronics:

A trigger-less readout architecture & its implementation

Outline

LHCb in brief

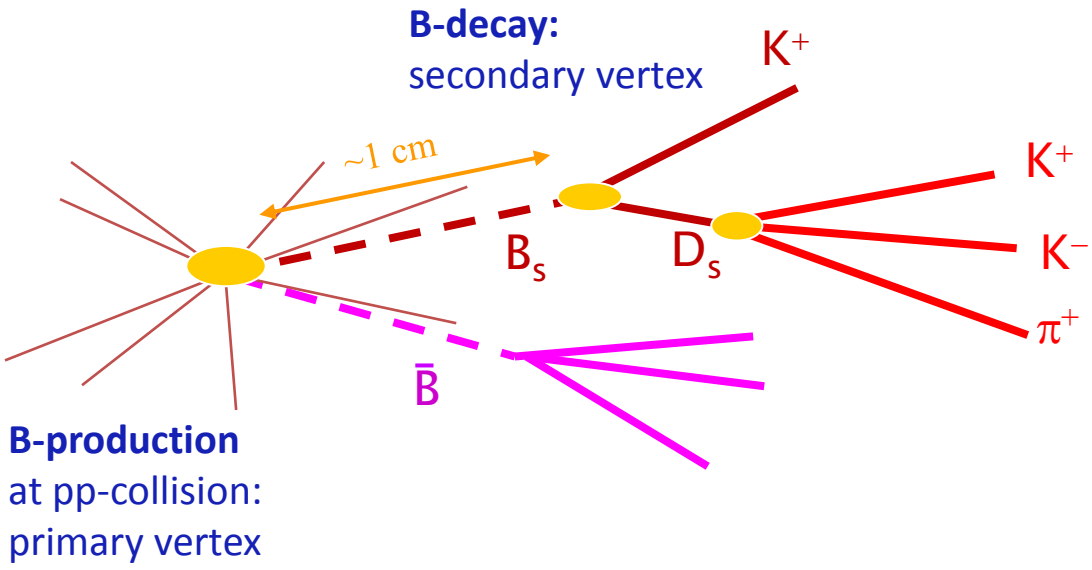
Motivation for upgrade

Architecture

Implementation

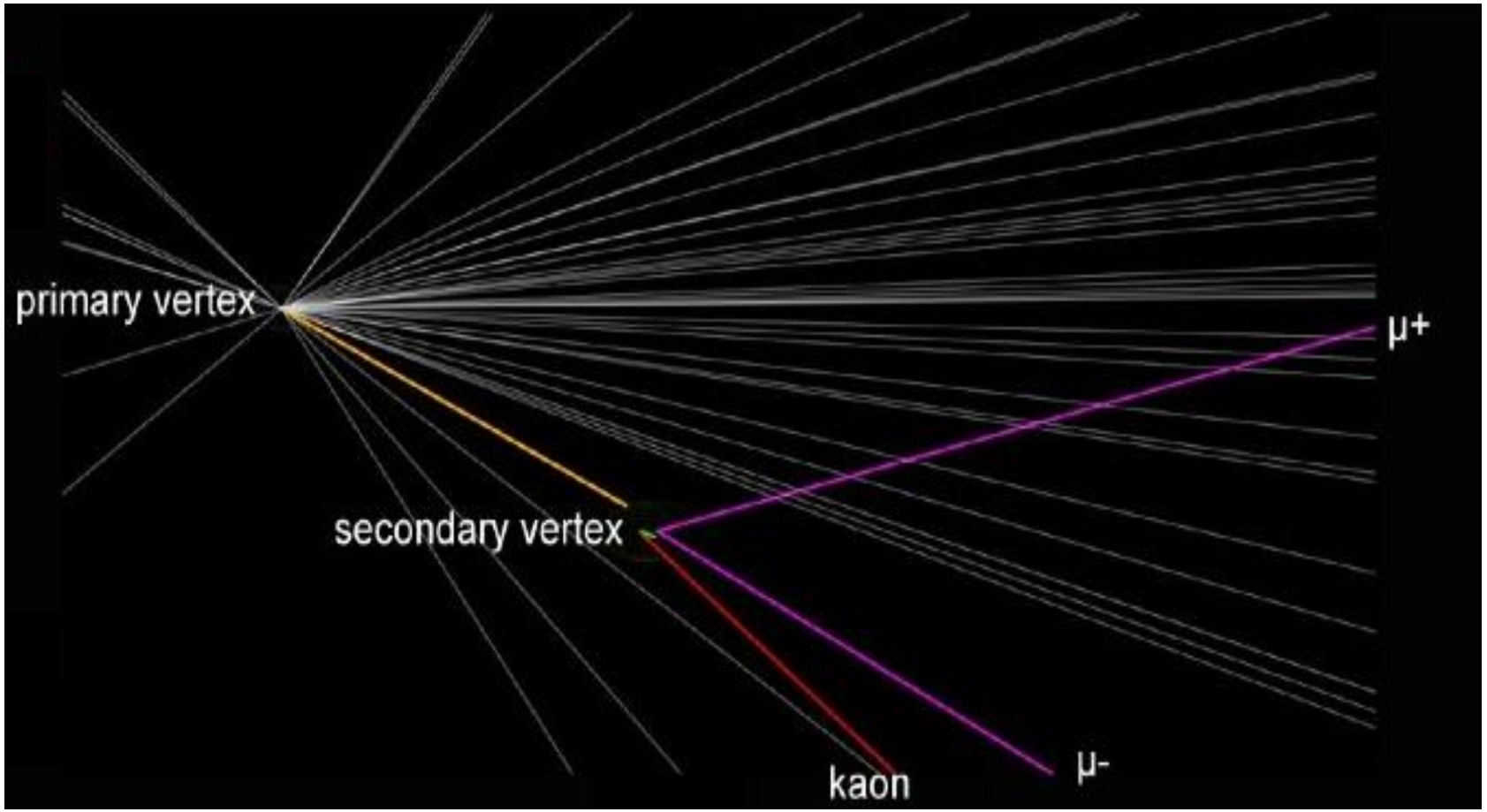
Many thanks to ESE & LHCb colleagues for the material

LHC-beauty

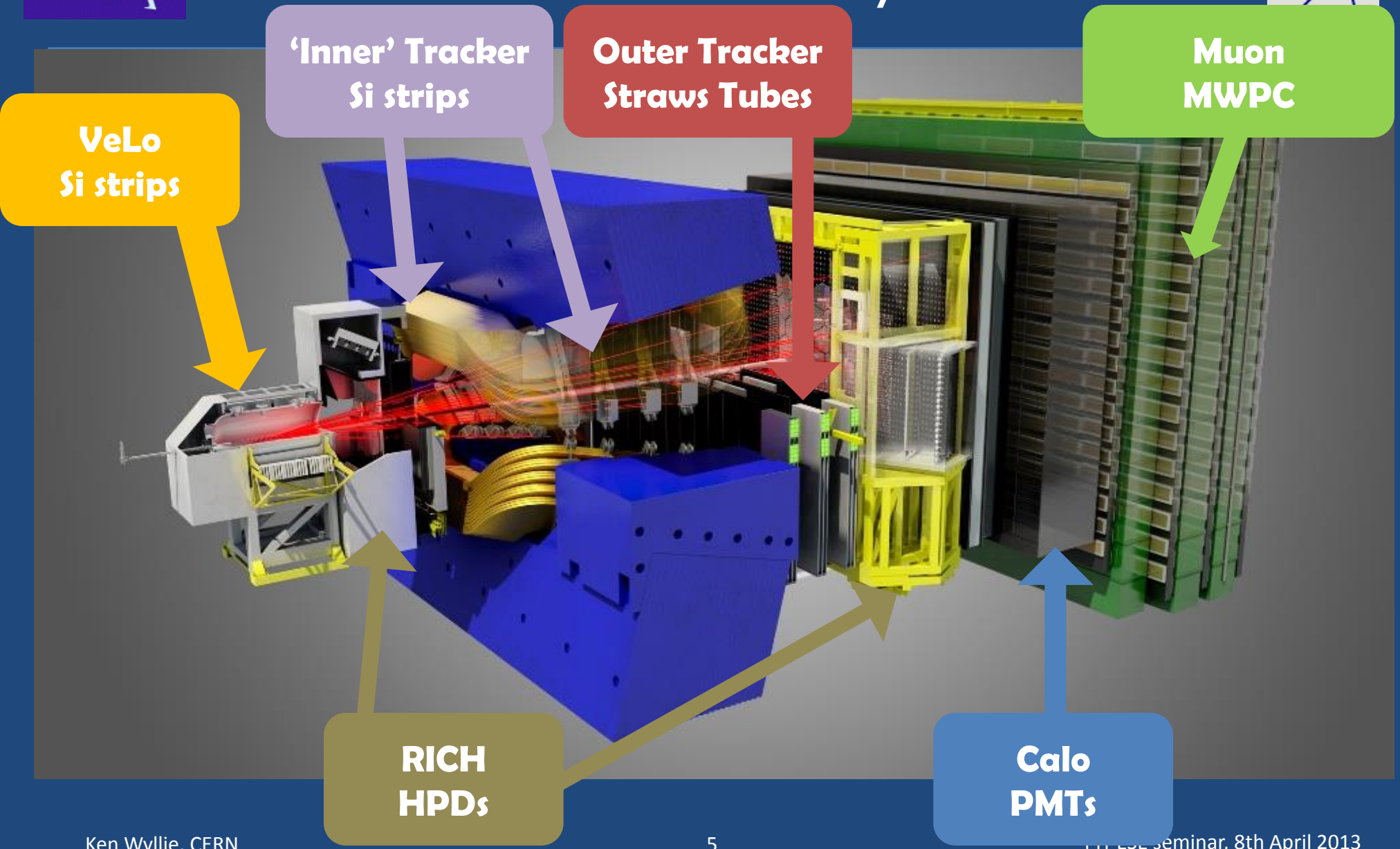


$\sigma(pp \rightarrow b\text{-hadron} + X) = 75 \pm 14\ \mu b$

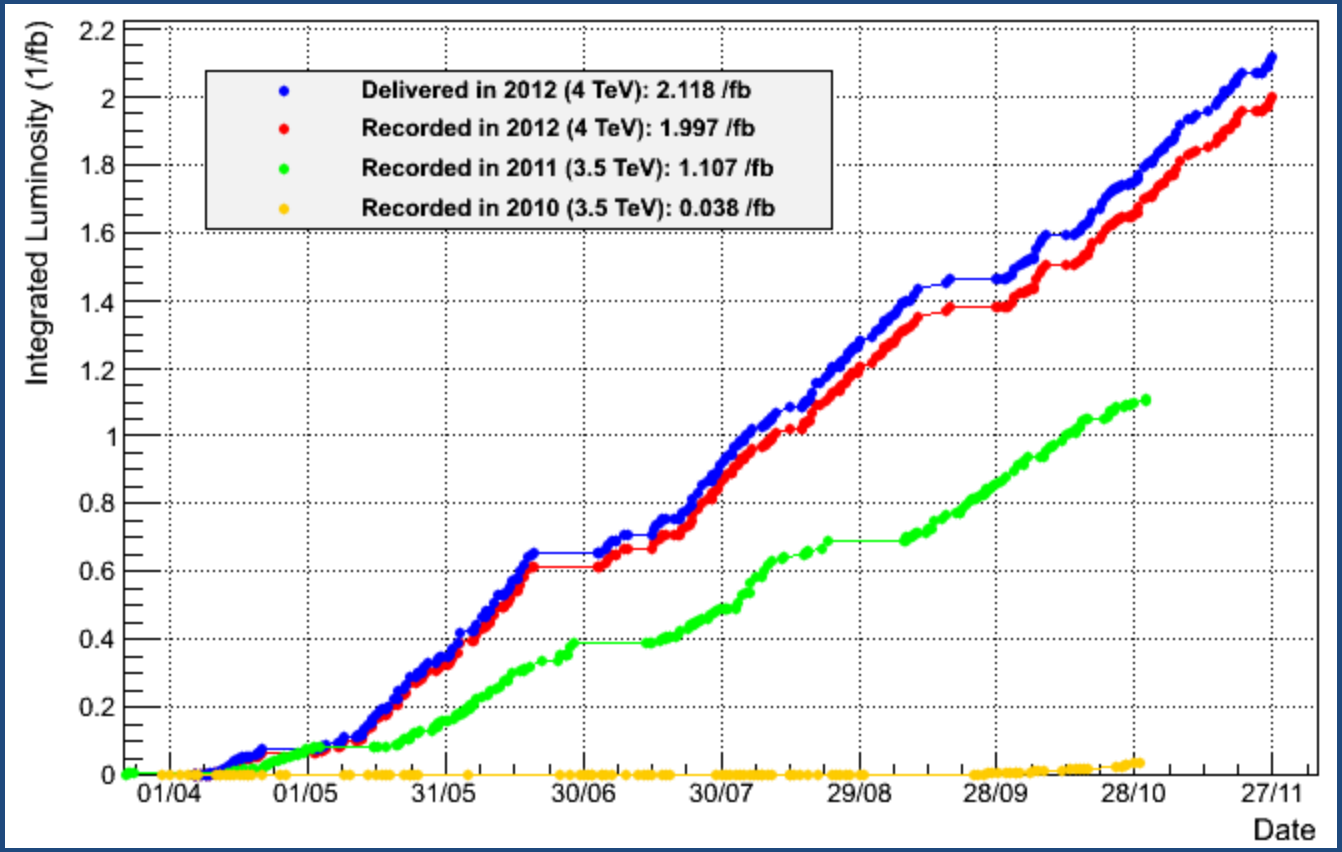
(7 TeV, LHCb acceptance)


primary vertex
μ+
secondary vertex
kaon
μ-

LHCb today


'Inner' Tracker
Si strips
Outer Tracker
Straws Tubes
Muon
MWPC
VeLo
Si strips
RICH
HPDs
Calo
PMTs

LHCb status



Total ~ 3 fb $^{-1}$

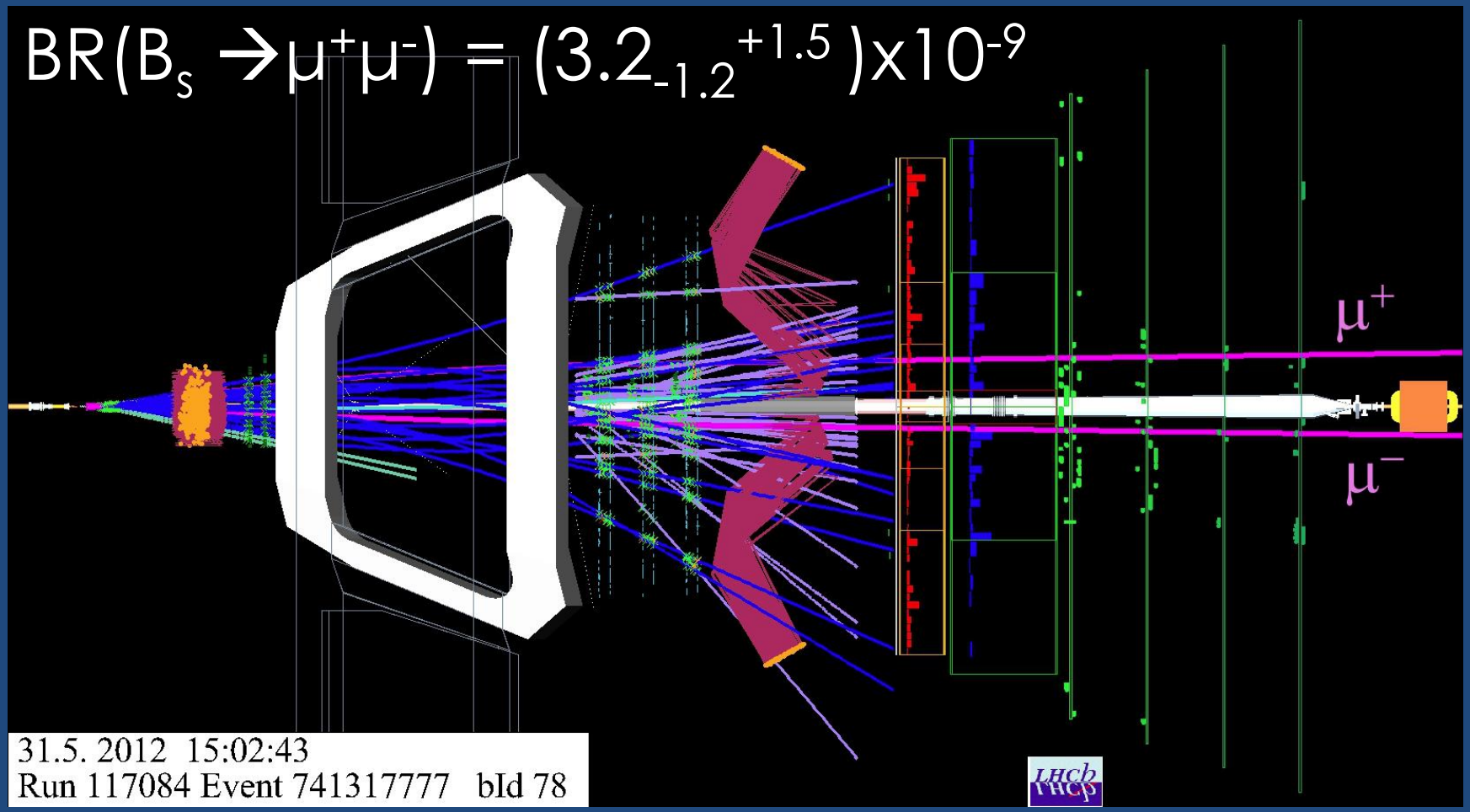
$\Rightarrow$ Billions of b-hadrons

Nominal Luminosity:

2 x 10^{32} $cm^{-2}s^{-1}$

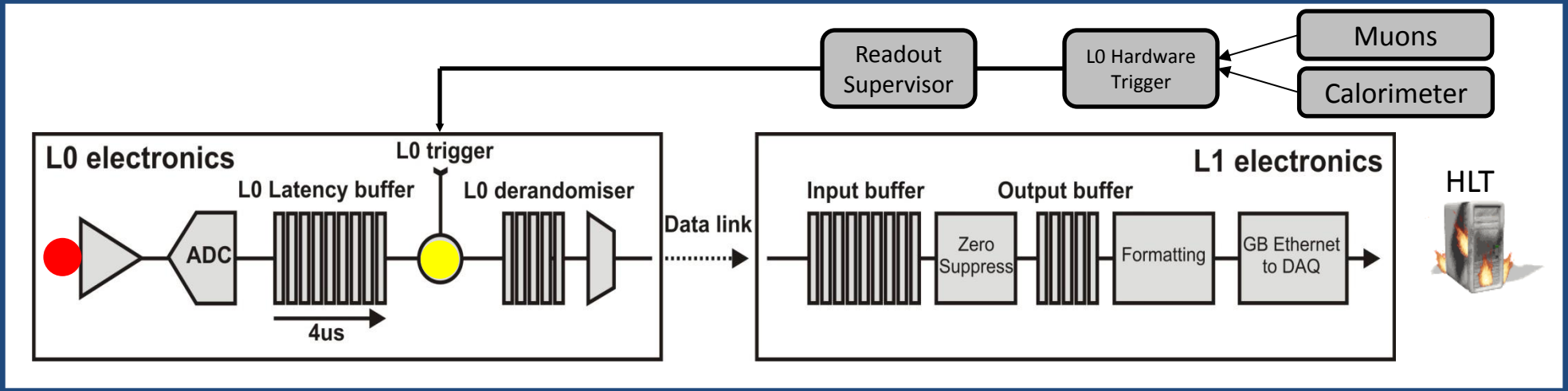
<< ATLAS, CMS

With billions of b-hadrons, can see rare decays



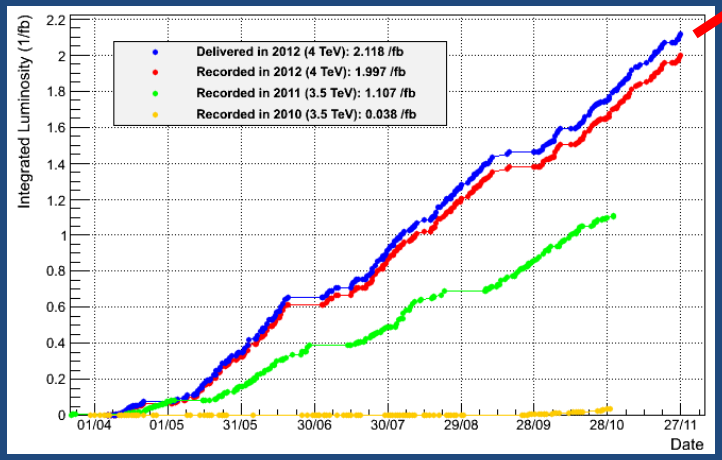
Existing readout system

Bunch crossing rate	40 MHz
L0 trigger rate	1 MHz average
L0 trigger latency	4 μs fixed (160 BXs)
Event readout time	900 ns
Event rate to DAQ	1 MHz



The future……

1 + 2 + 2 fb $^{-1}$



Motivation for upgrade

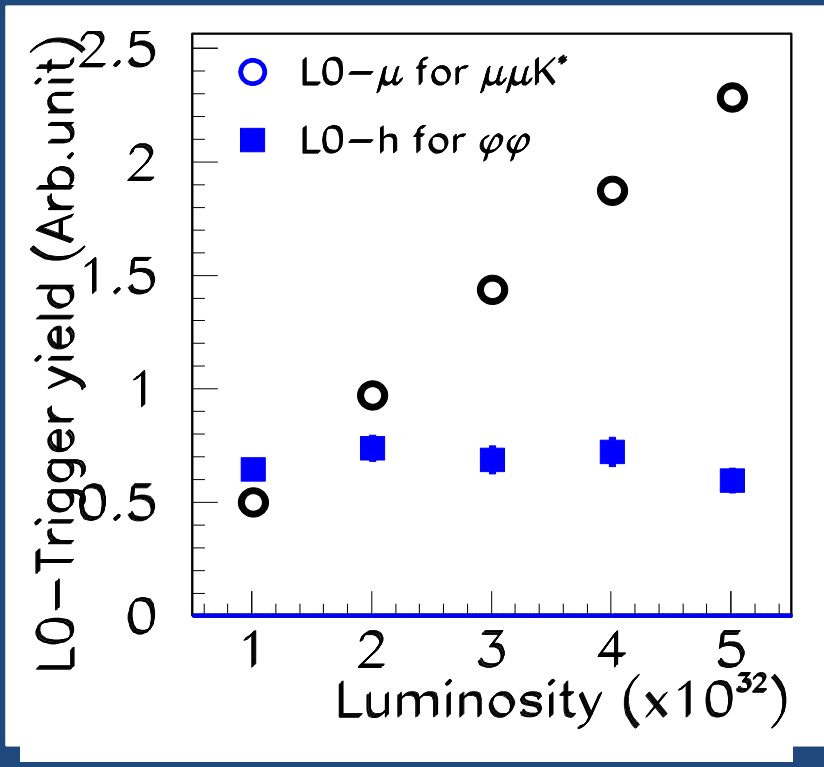
At L = 2(+) x 10^{32} $cm^{-2}s^{-1}$,
beyond 5 fb^{-1}, statistics don't improve much

Big statistical improvement if:

- increase L to 2 x 10^{33}, AND
- improve efficiency of trigger algorithms

BUT ..... with current L0 trigger:

rate & latency limited by electronics
(1 MHz, 4 μs) => saturation



BUT…. efficient trigger decisions require:

- long latencies (>> 4 μs)
- computational power
- data from many (all) sub-detectors (momentum, impact parameter .....)

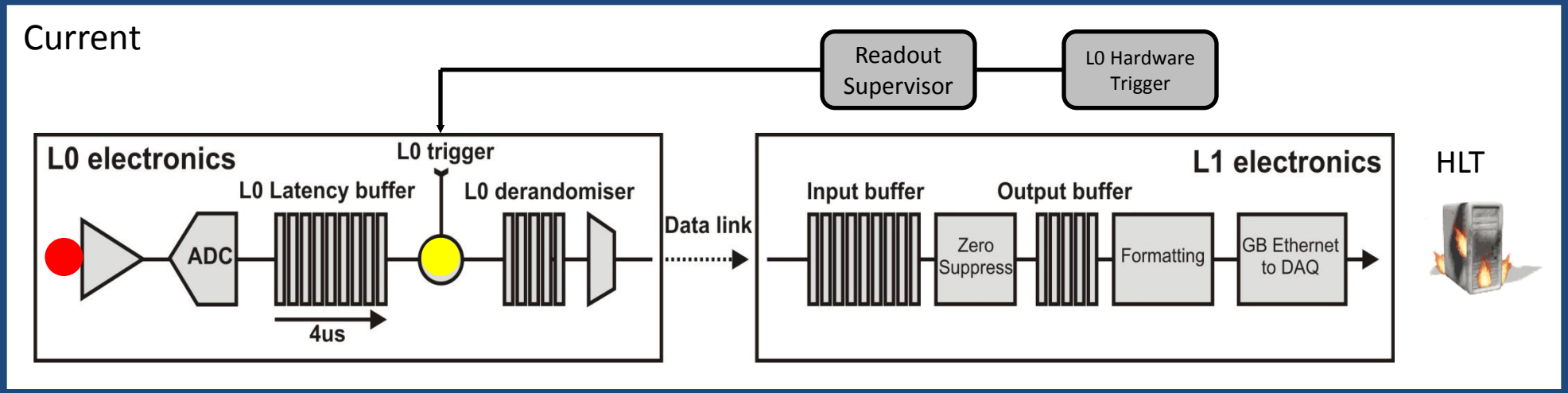
⇒ Trigger in software

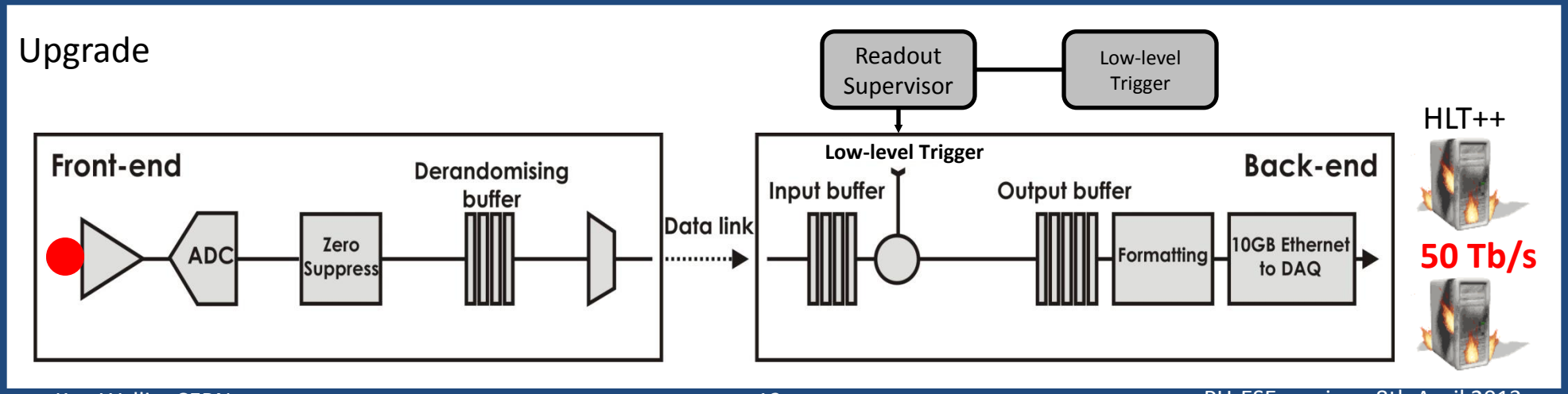
⇒ Use data from every bunch crossing

⇒ Upgrade electronics + DAQ

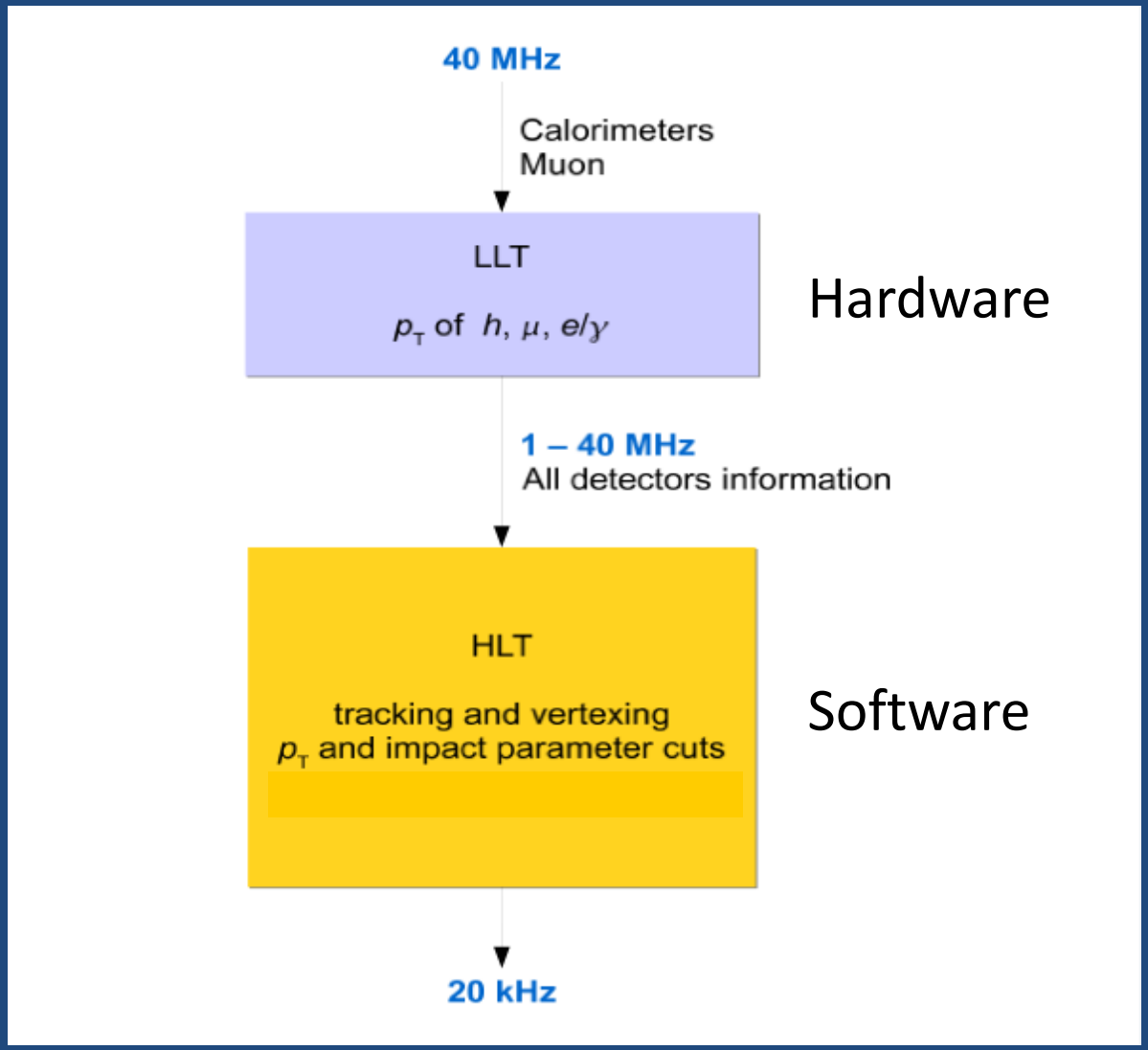
Upgrade architecture

No 'front-end' trigger, Event rate to DAQ nominally 40 MHz





Triggering doesn't completely disappear



Can we do it?

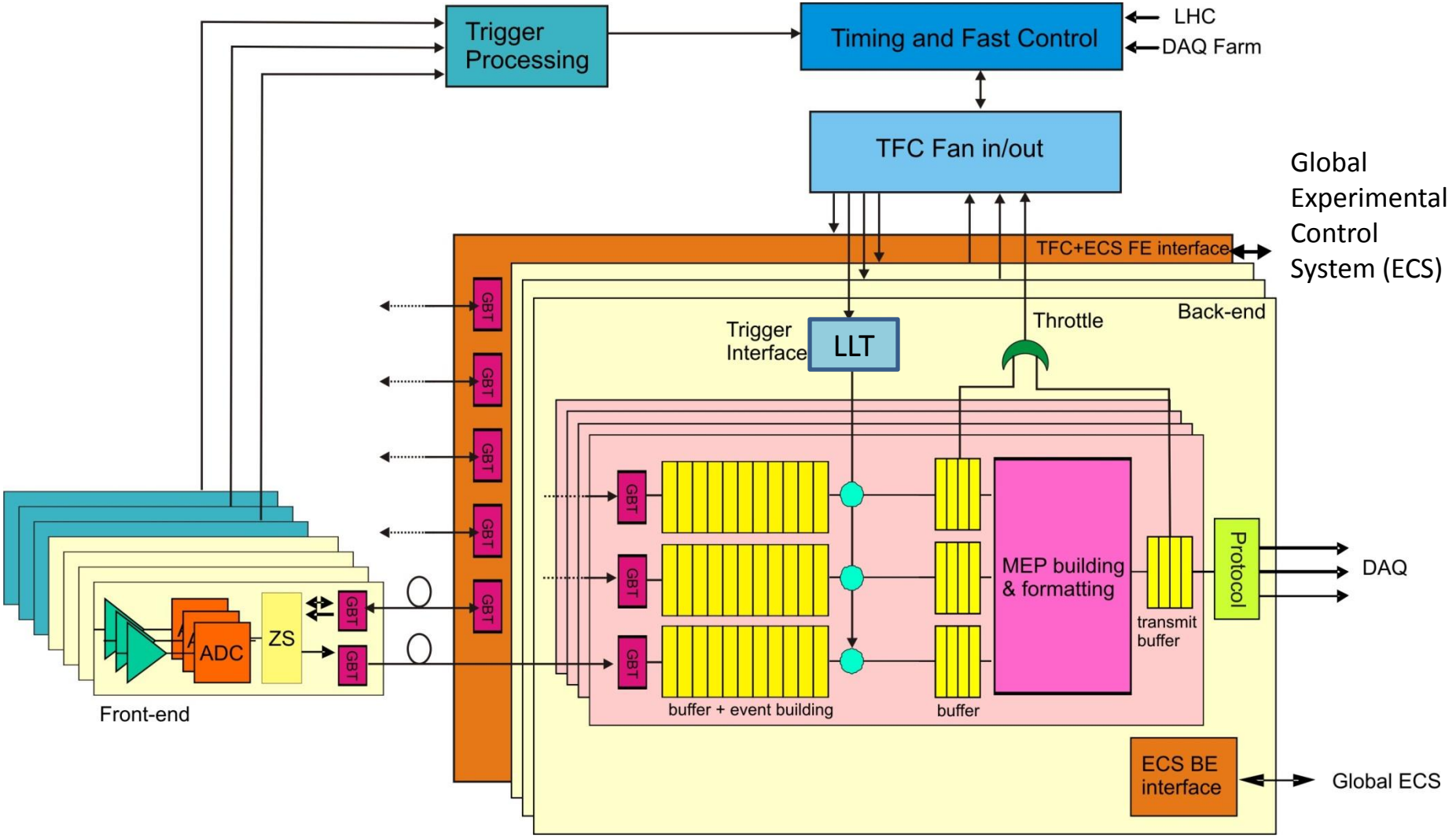
..... actually, can we afford it?

Trends in high speed optical data transmission

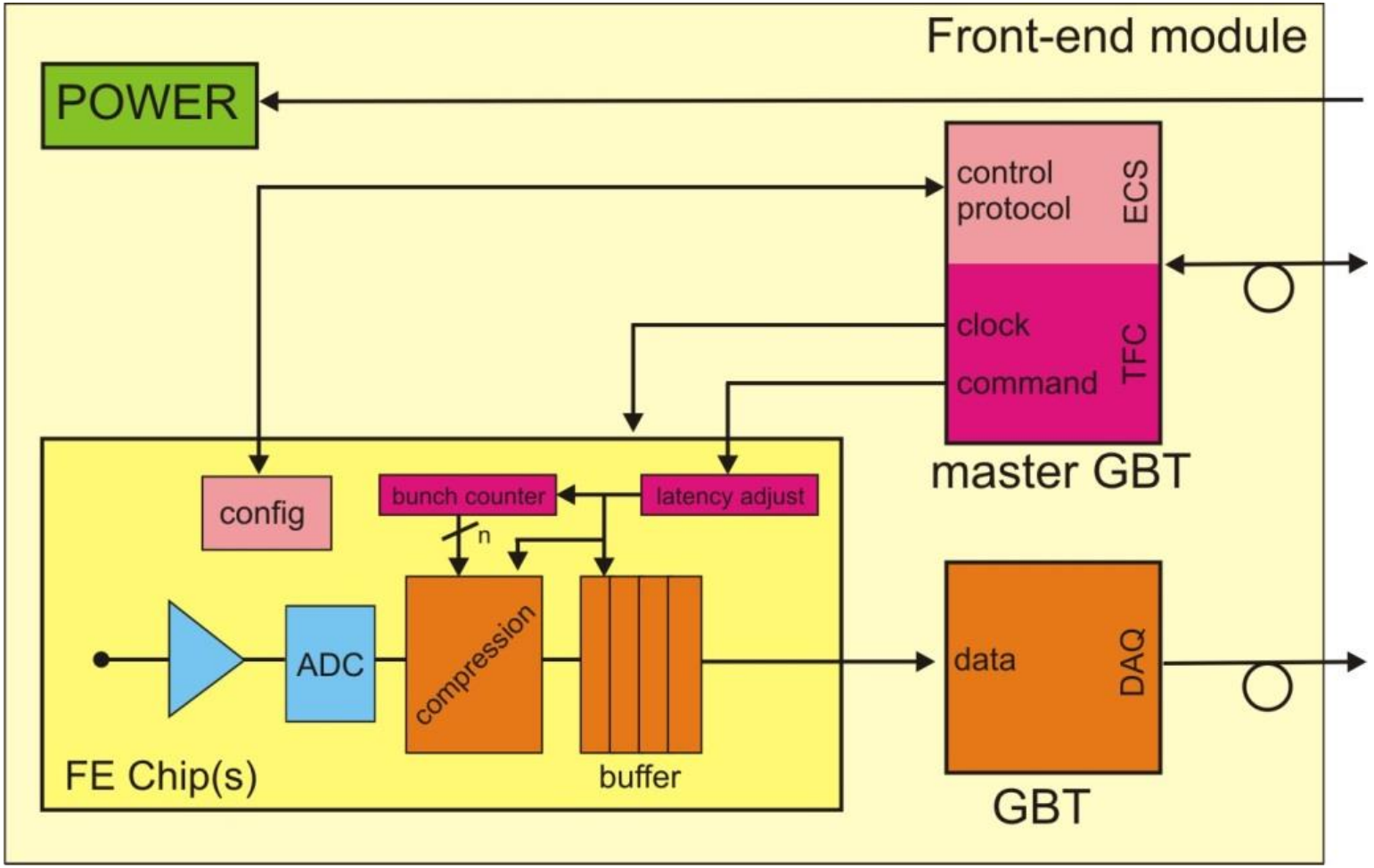
1Gbit/s ➡ 10Gbit/s ➡ 40Gbit/s

..... and strong programme for rad-tolerance
..... and trends in embedded links in FPGAs

Architecture: more detail



Architecture: more detail



Architectural choices 1

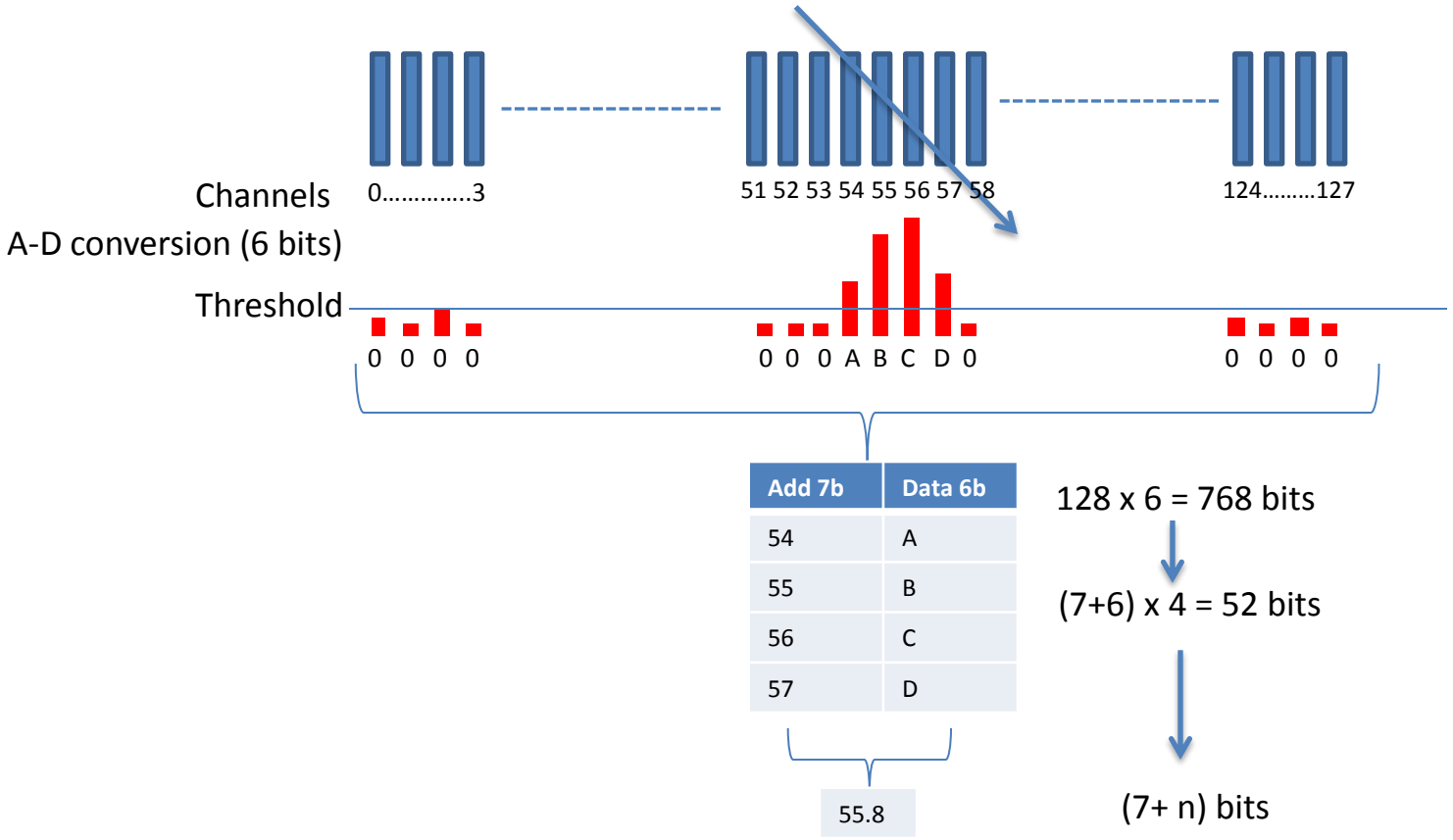
Data compression on front-end driven by cost:

no compression	~ 80,000 links (4.8 Gb/s)	20 MCHF
compression	~ 12,500 links (cf 8,000 today)	3.1 MCHF

Compression (zero-suppression) currently done in FPGAs in readout boards:

careful balance of complexity vs robustness
needed a few iterations get it right

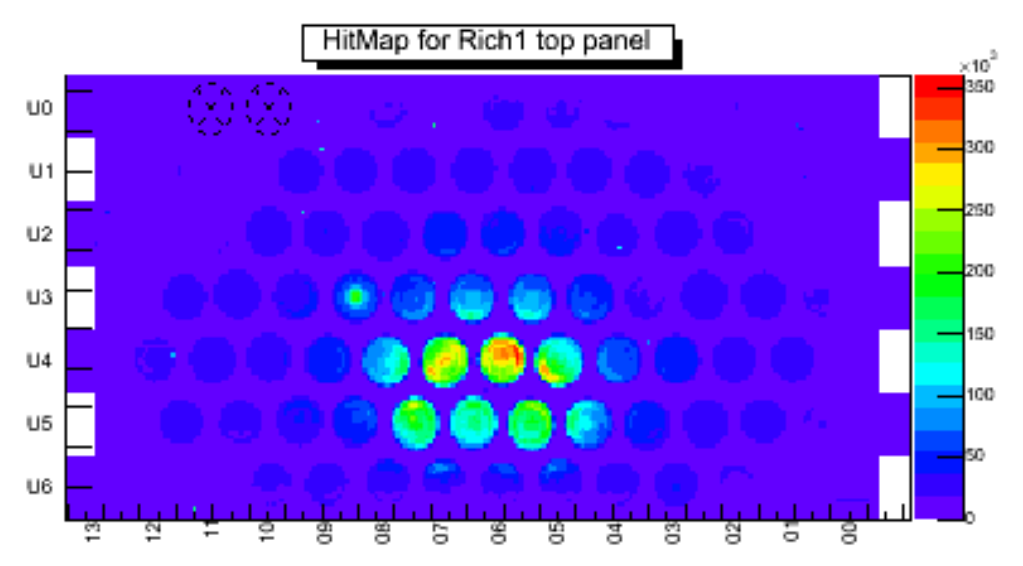
Simple, easy zero-suppression



Complicated by: signal/noise
channel-to-channel gain variations
pedestals & common mode etc etc

But we have different detector environments:

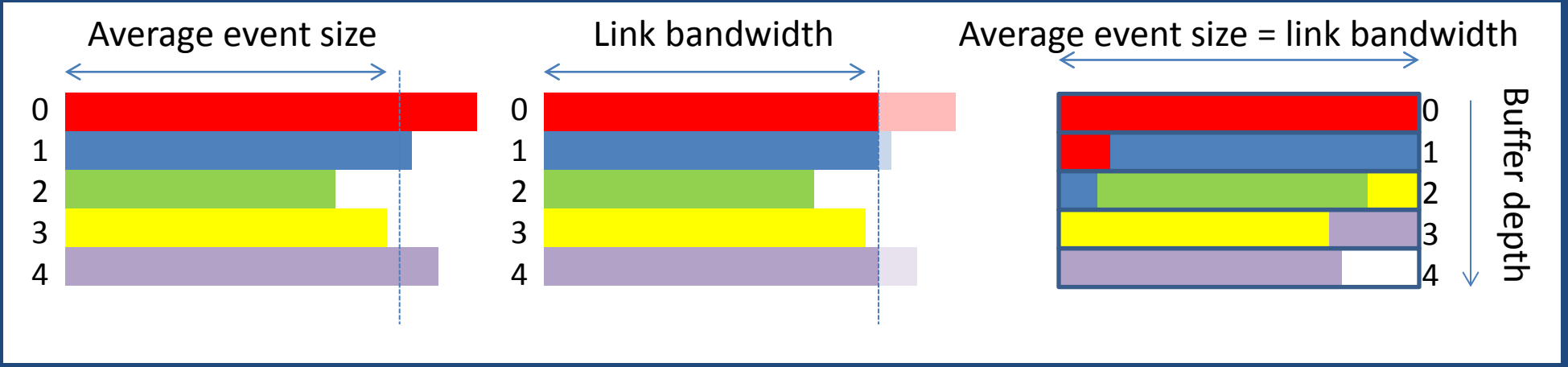
eg RICH hit distribution



low occupancy => zero suppress
high occupancy => buy links $$$
non-uniform occ. => optimise

(with margins + flexibility)

Architectural choices 2



Try to use link bandwidth efficiently: use statistics

- Elastic buffer before link
- Size? Simulate with margin (scale-able system?)
- Overflow => truncation of data (but no loss of synch)

…….. Be careful……

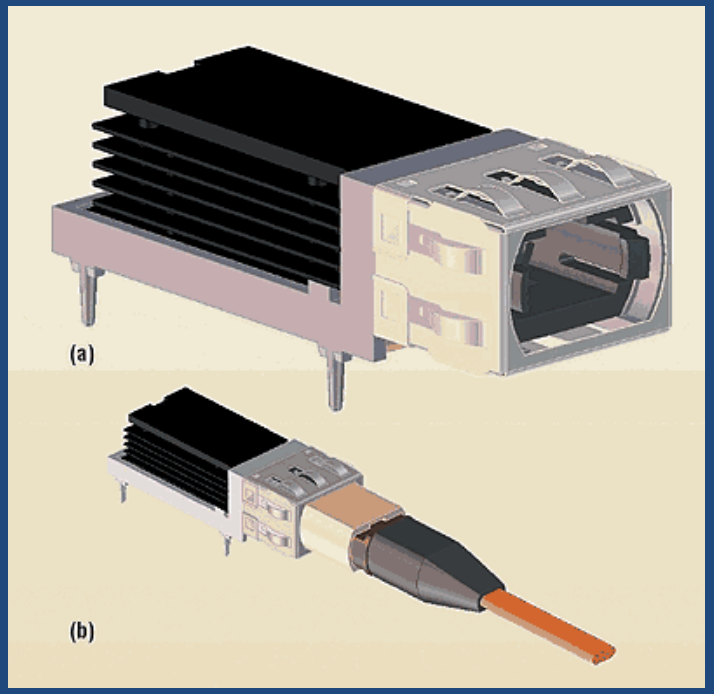
Needs good knowledge of detector data rates (eg backgrounds)

Limits the luminosity?…… we always want more data

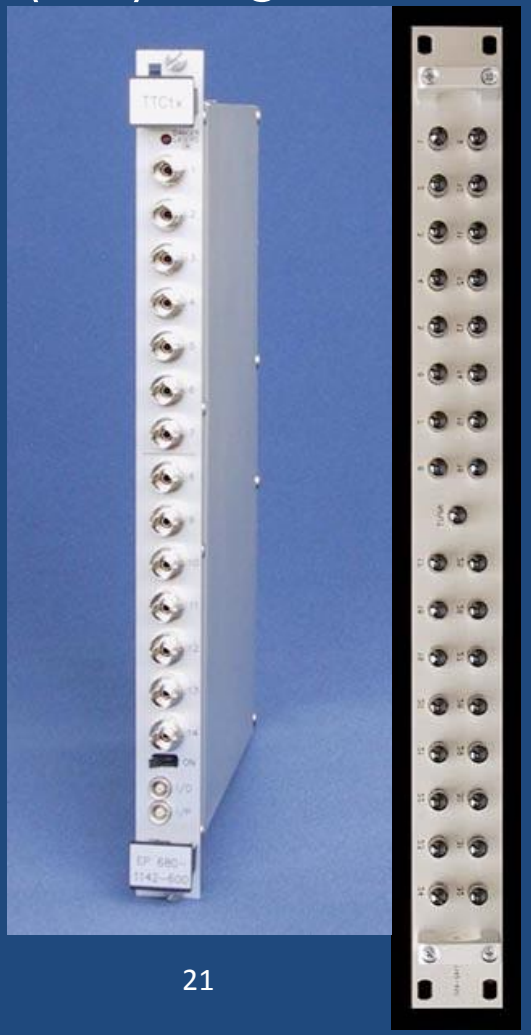
Communications

Current LHCb has 3 different media for transmitting information

Data: multi-mode fibre



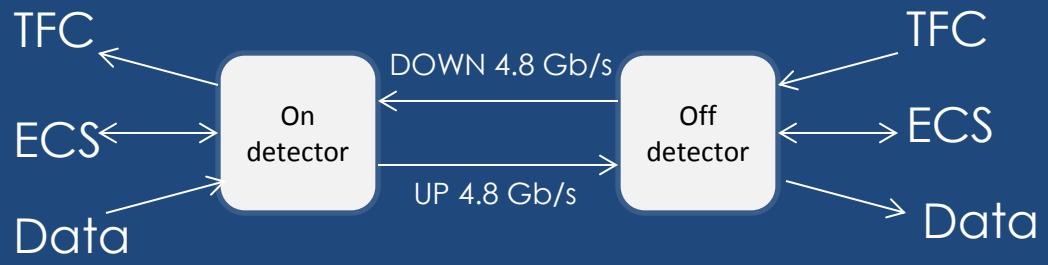
TFC (TTC): single-mode fibre



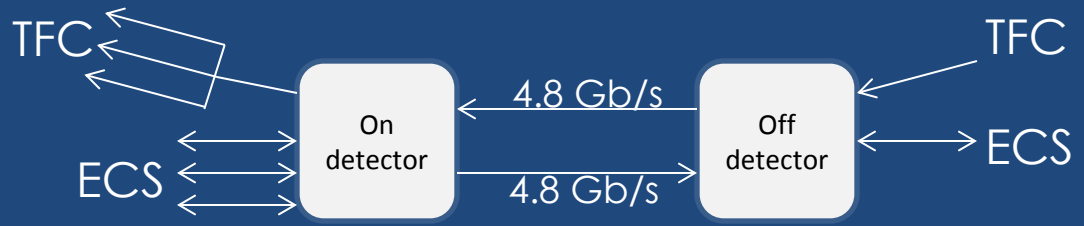
ECS: CAT6 + RJ45

Architectural choices 3

New compact link offers combined Data, TFC, ECS

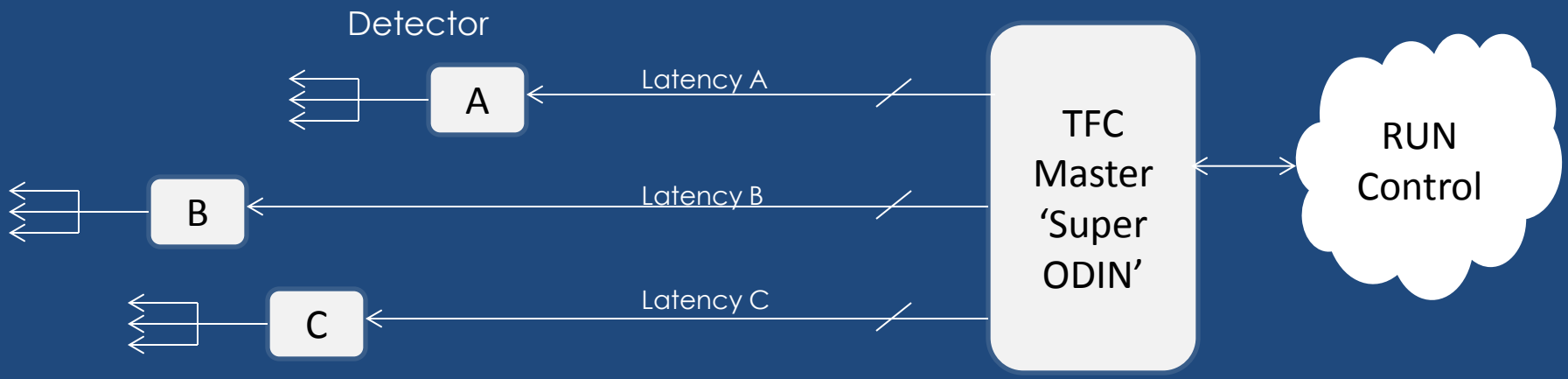


Need UP bandwidth >> DOWN bandwidth
=> Combine TFC+ECS; Separate Data



Control & Synchronisation

Control with synchronised fast commands
eg bunch-counter reset

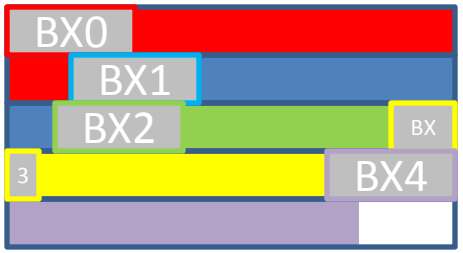


Latencies will be measured => pre-scaling of commands by S-ODIN

Absolute measurement with: pulsed laser
cosmics
low intensity LHC beam collisions

All data tagged with Bunch-Crossing Number (0 - 3563)

- reference for event building
- used for continuous synchro checks
- always transmitted
- identifier for LLT filtering



From ideas to implementation

Implementation Philosophy

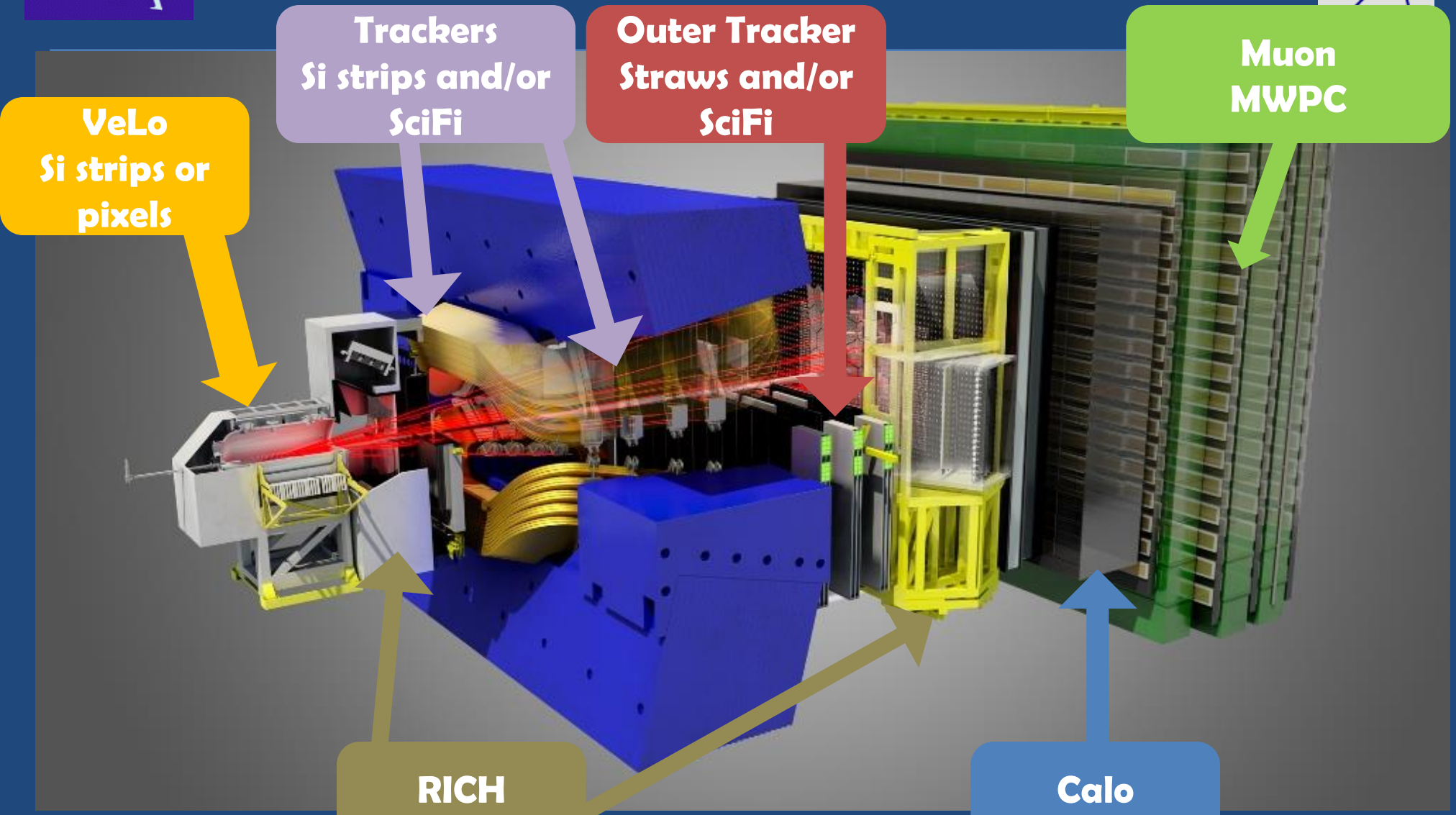
Try to optimise:

- Cost
- Manpower
- Time (development, production, installation)

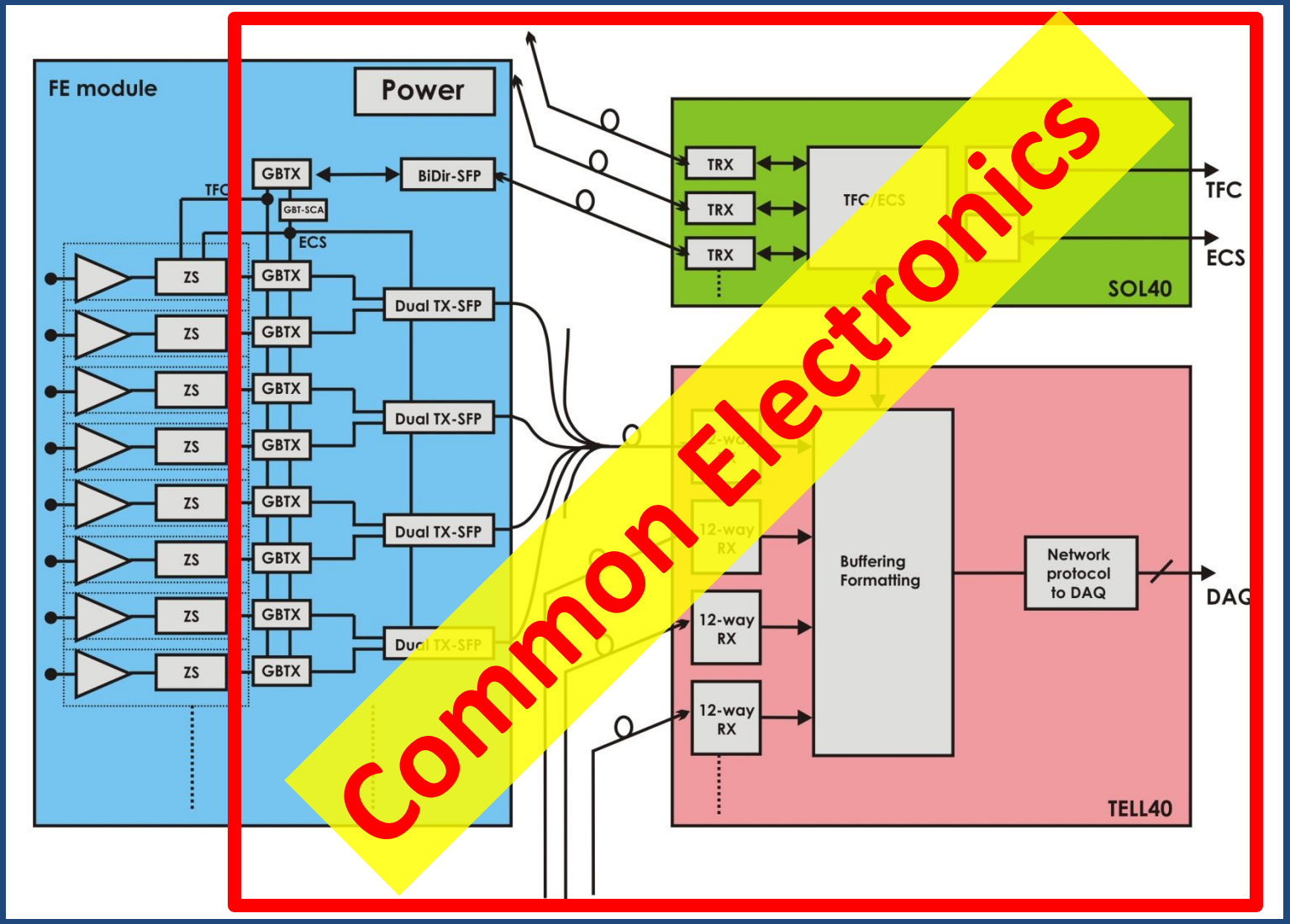
1. Re-use existing electronics & infrastructure if they are proven to do the job

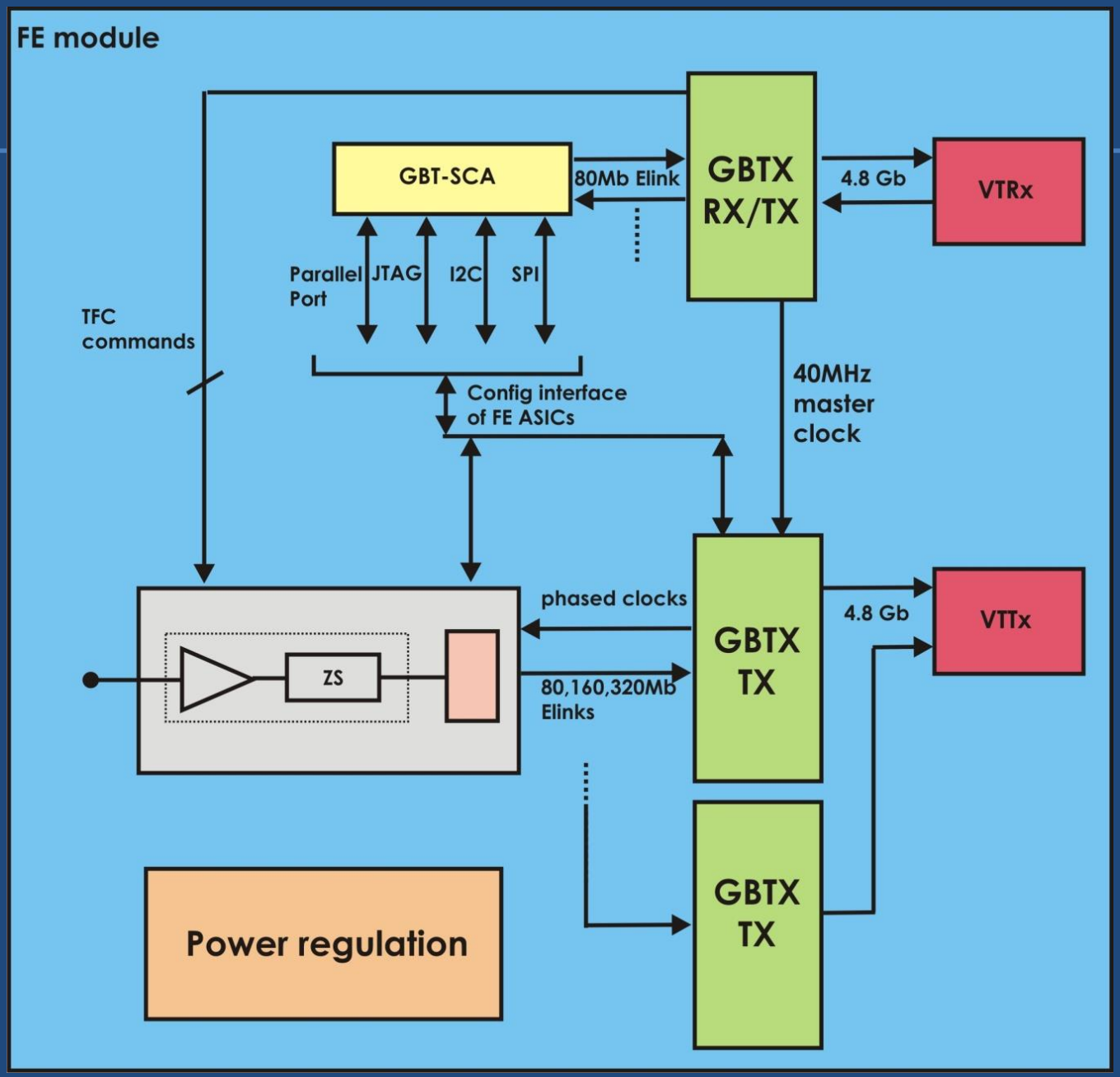
2. Develop common solutions for use by all sub systems

LHCb future


Trackers
Si strips and/or
SciFi
Outer Tracker
Straws and/or
SciFi
Muon
MWPC
VeLo
Si strips or
pixels
RICH
MAPMTs
Calo
PMTs

Generic Implementation





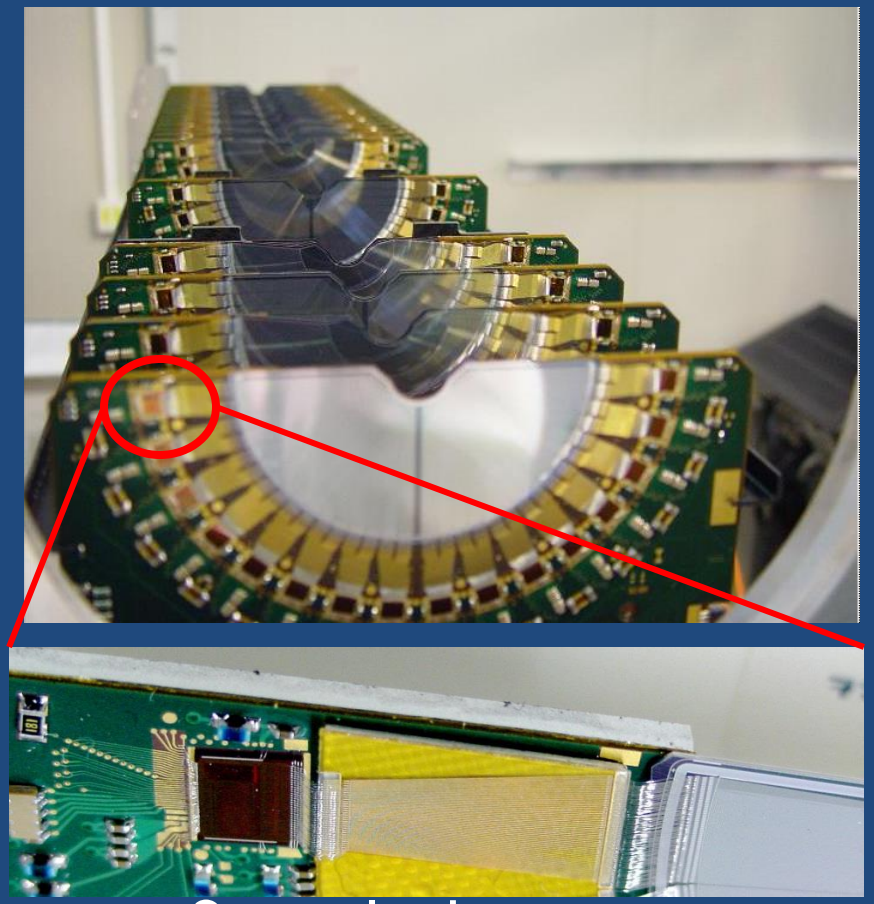
100% robust

Can allow a small rate of errors
BUT
No loss of synch

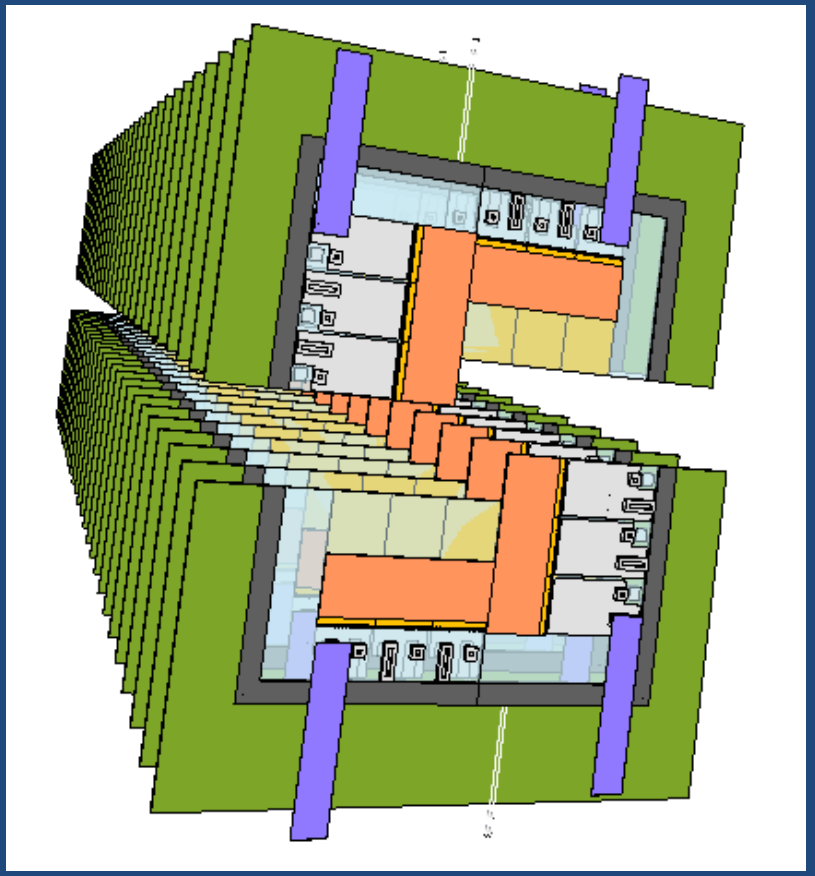
Non-exhaustive overview of implementation

VeLo

Si micro-strips or Si pixels



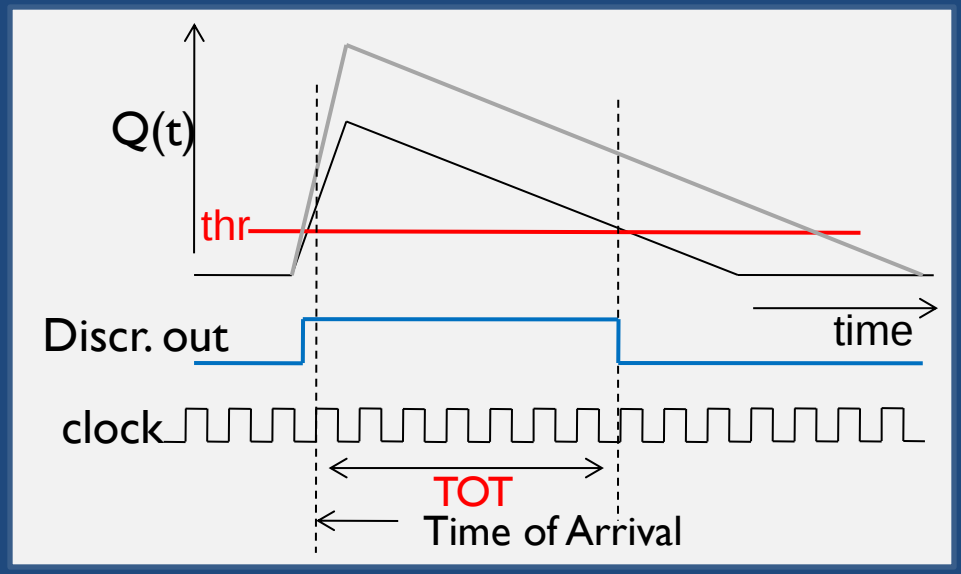
See later



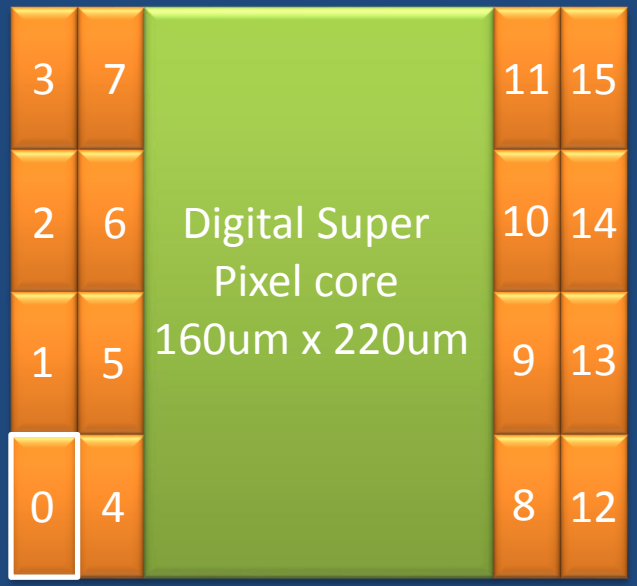
VeLoPix

55um pixels, 256 x 256 array
130nm CMOS: rad-hard, low power, density

ToT for pulse height from Timepix

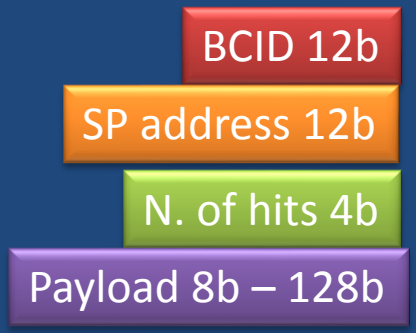


Matrix = 64 x 64 super-pixels

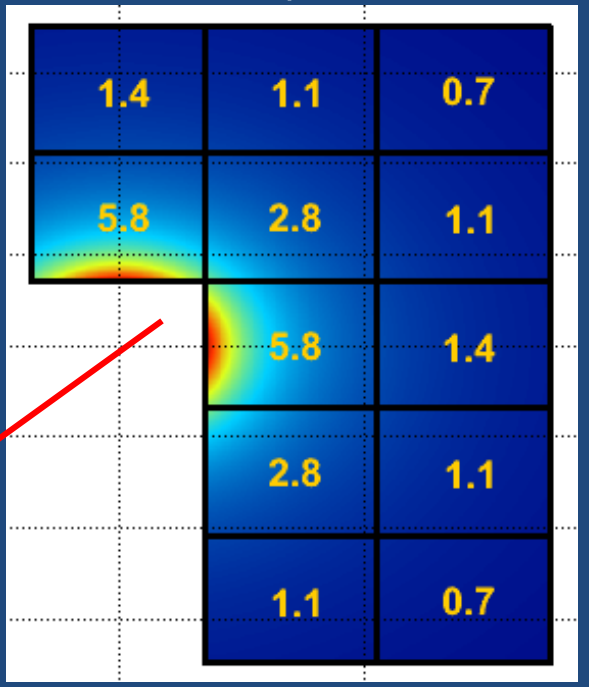


Front-end

Data packet



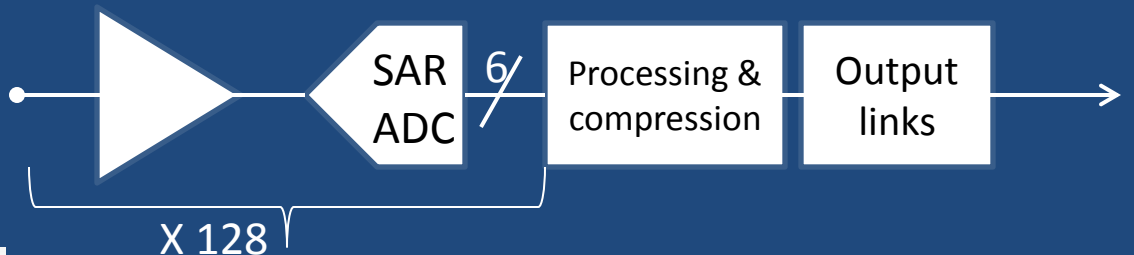
tracks per 25ns

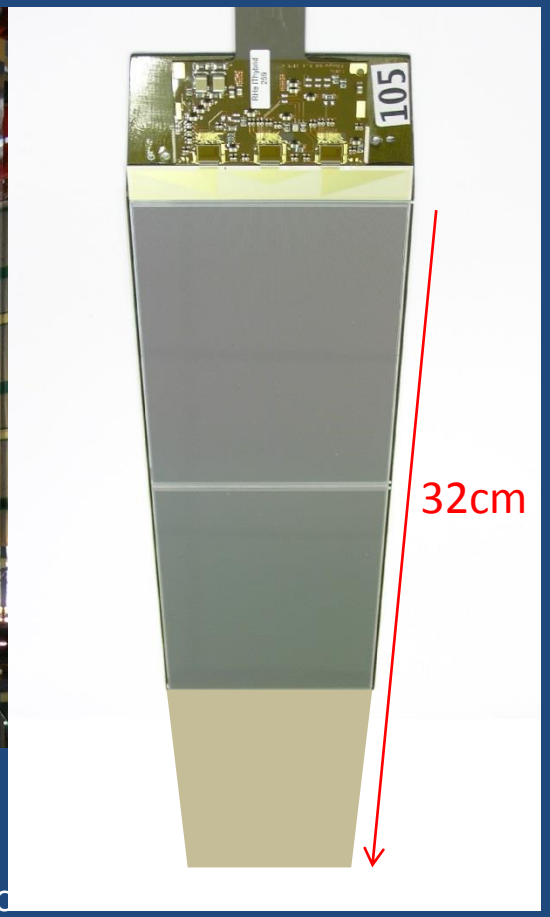


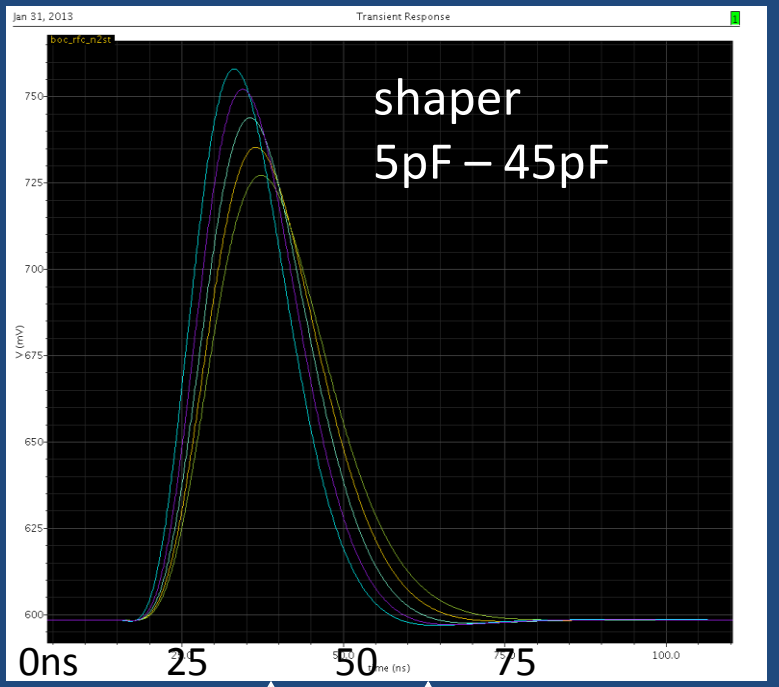
Hottest chip: 12.2 Gbit/s of data

Silicon-strip Trackers

ASIC in 130nm CMOS
rad-hard
low power

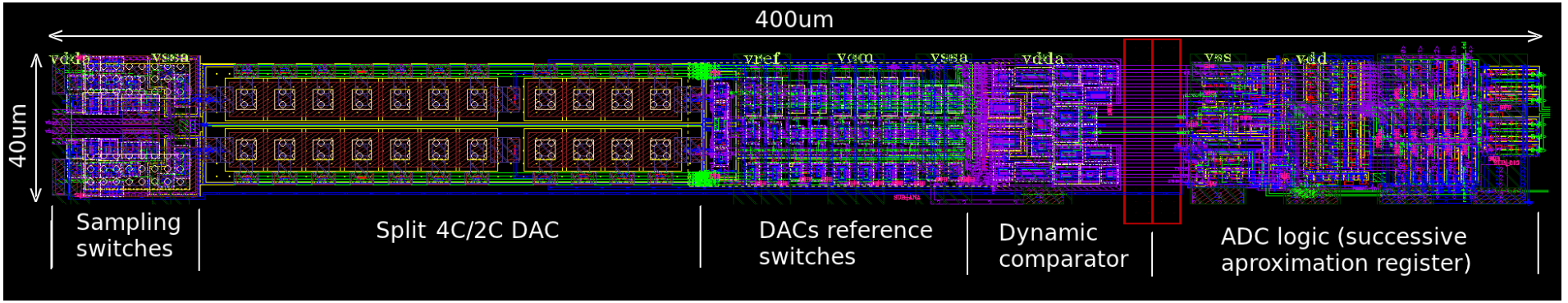


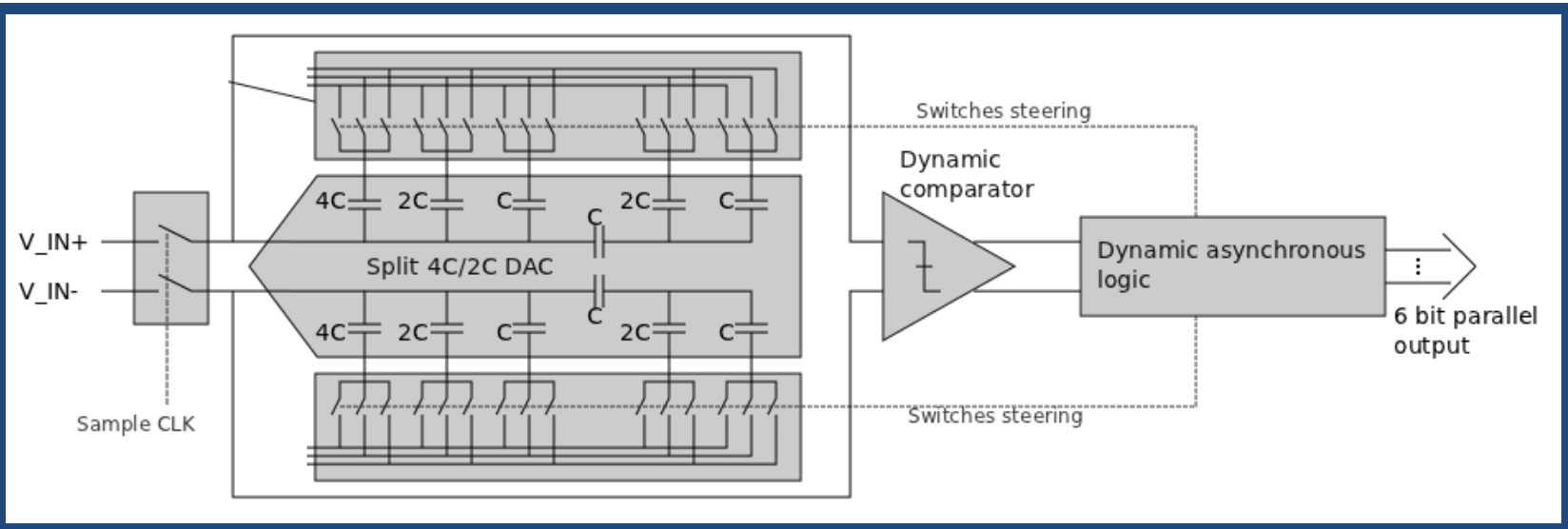




Small spillover 25ns after peak

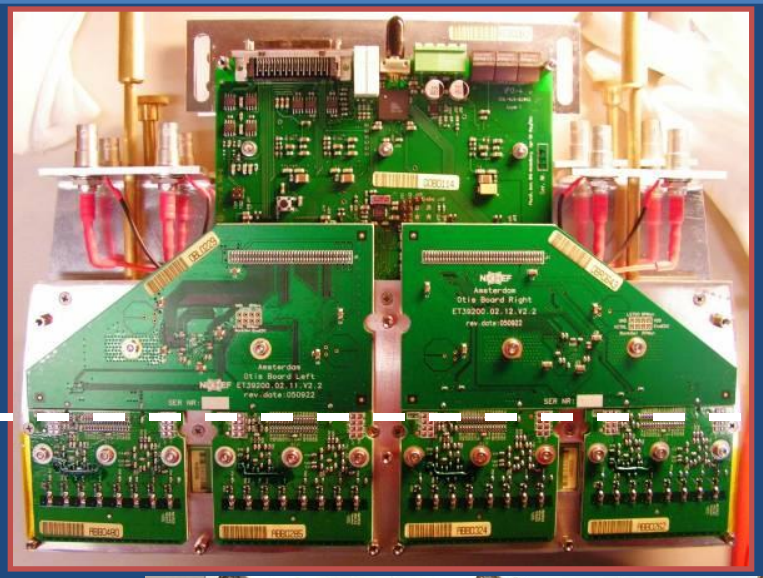
SAR ADC





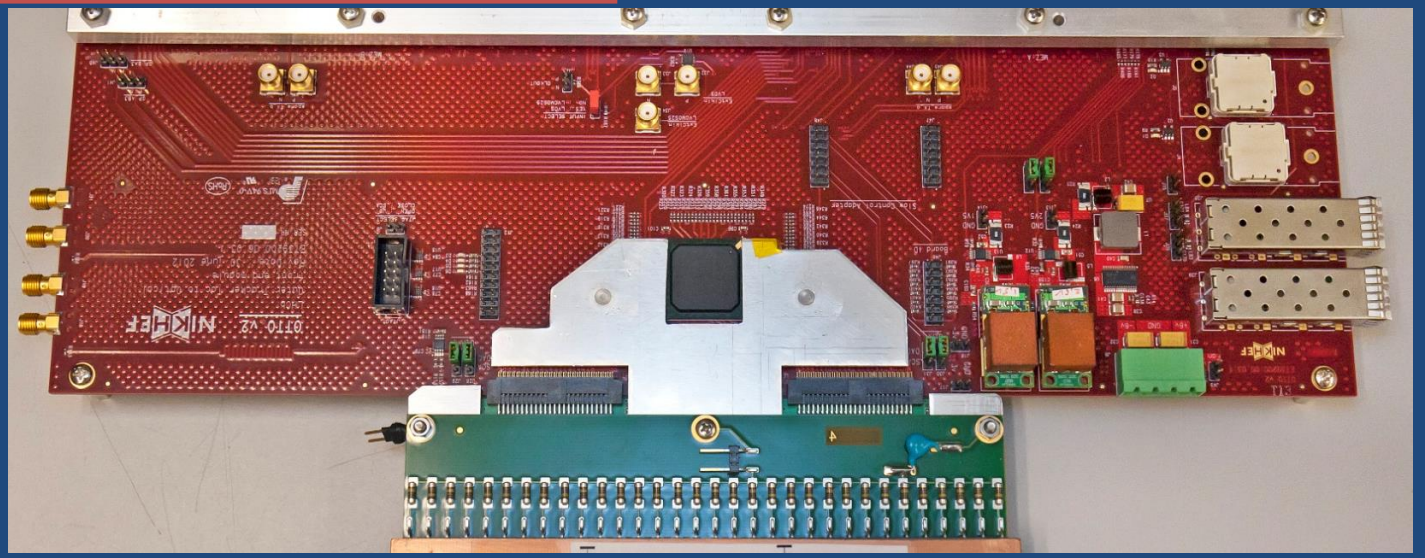
Under test, expected power < 0.5 mW

Outer Tracker (straw tubes)



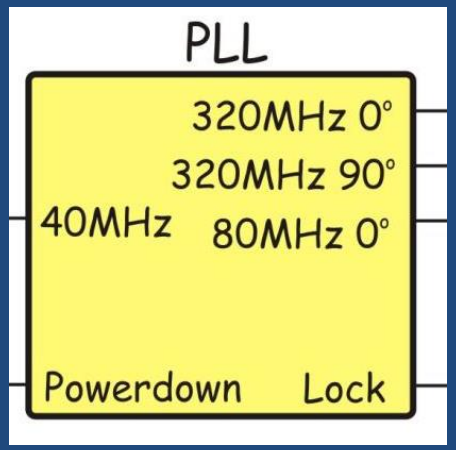
Re-use existing front-end

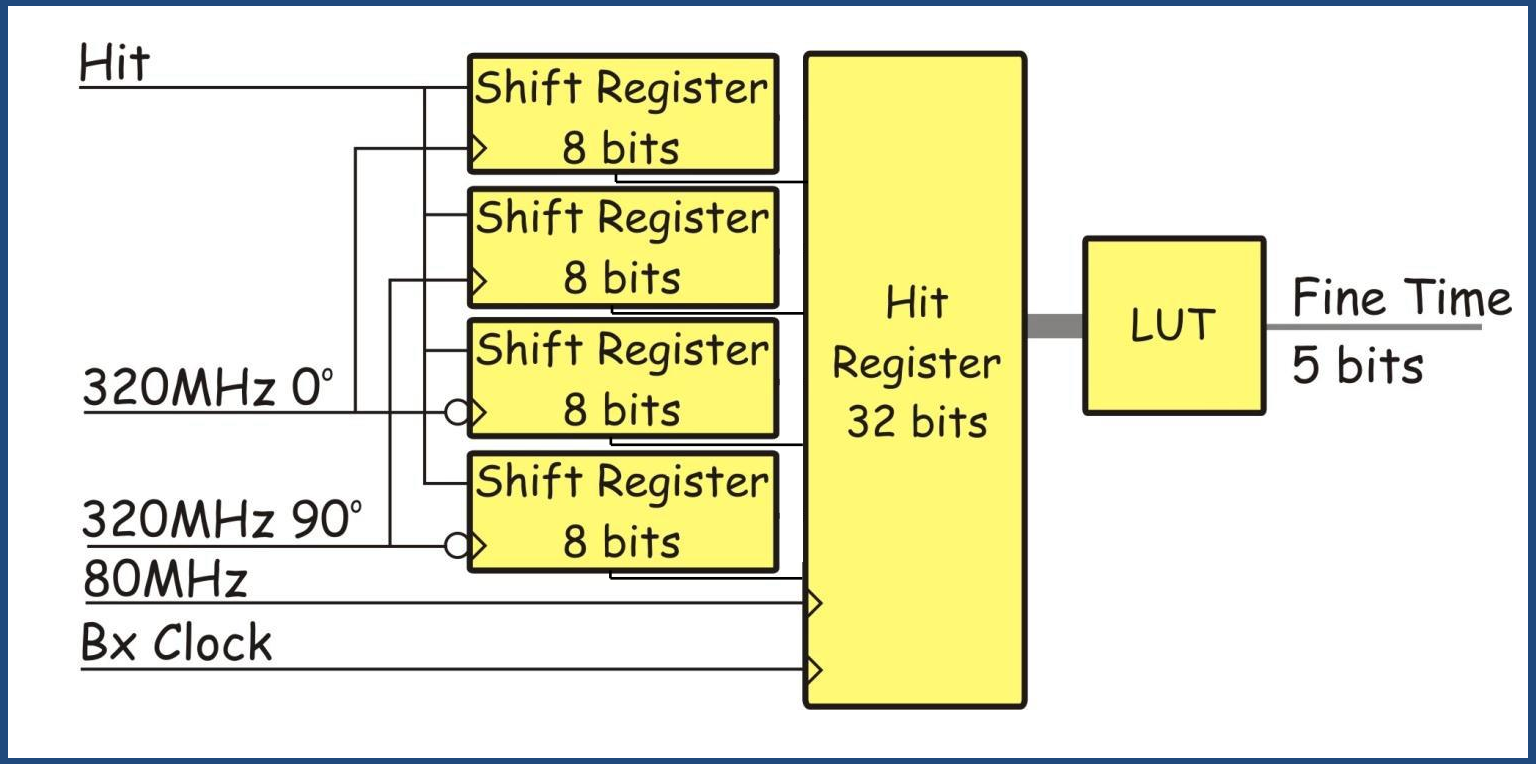
TDC (ASIC) mapped to
- flash FPGA
- SRAM FPGA



TDC in flash-FPGA

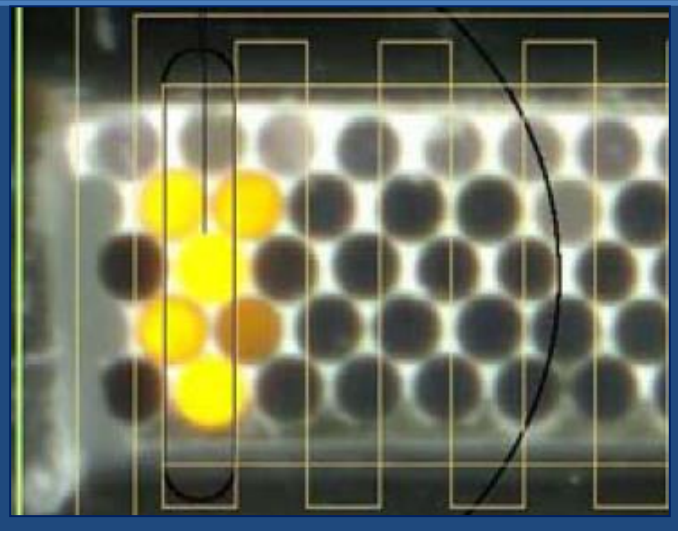
32 bins,
0.78 ns

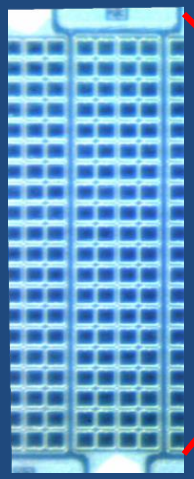


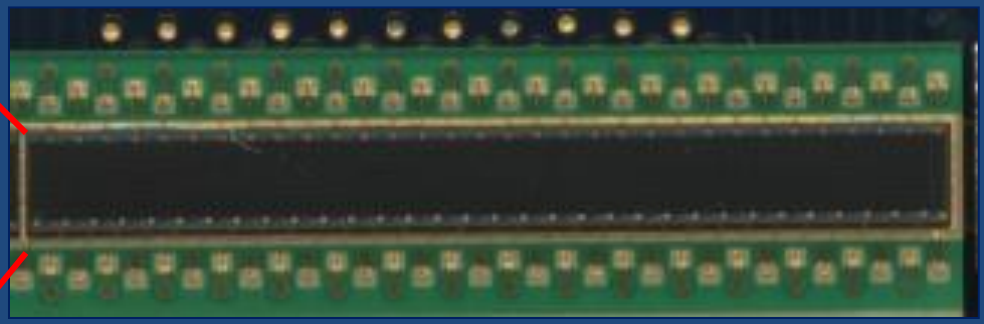


OK in radiation……?

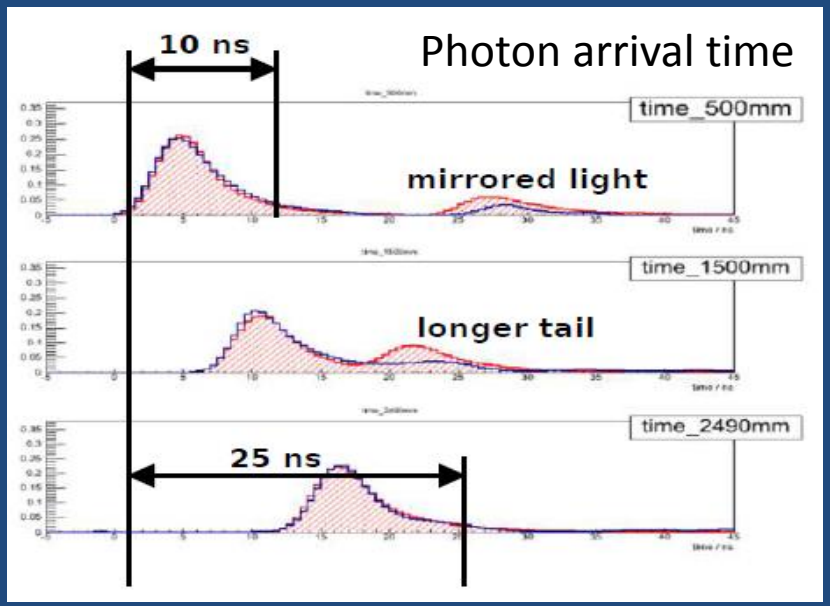
SciFi Tracker (SiPMs)

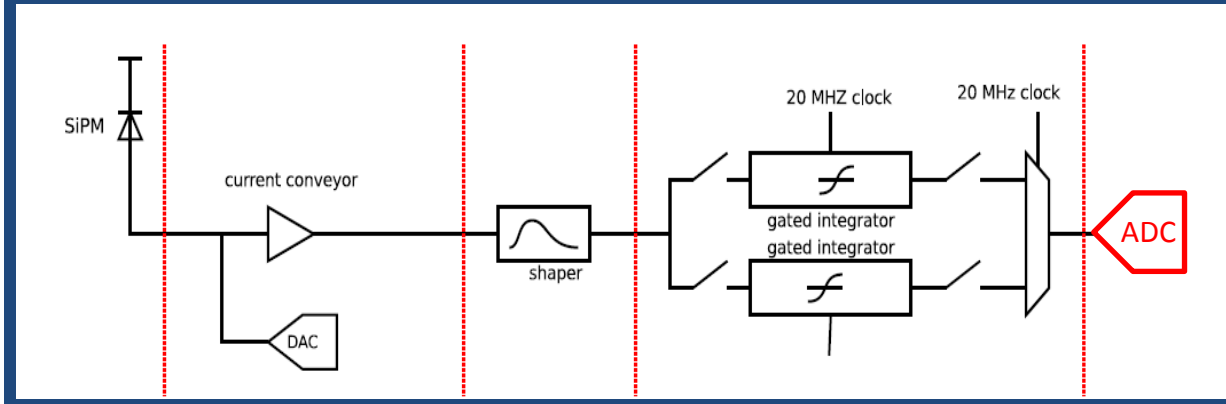






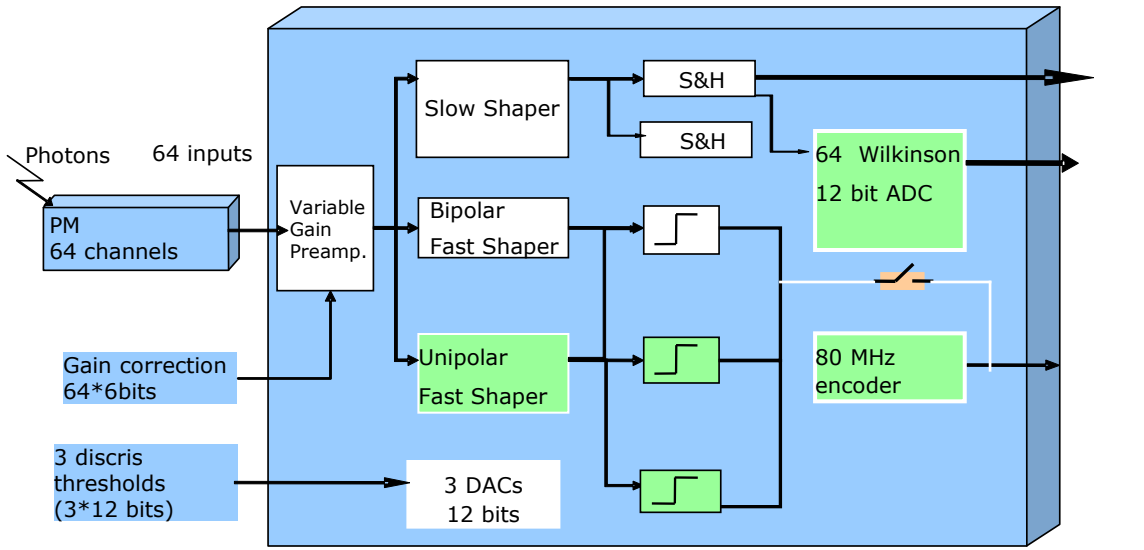
Signal shape!
Gain variations ?
Clustering to reduce noise



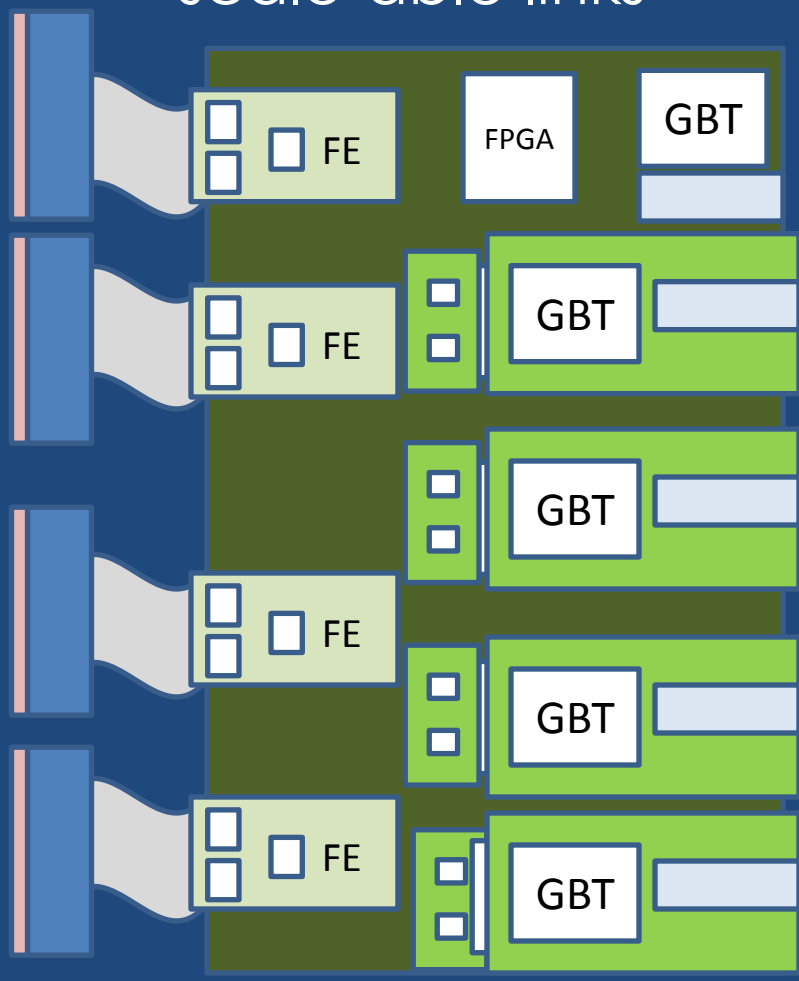


RICH (MAPMTs)

Adjustable gains in front-end MAROC3 or CLARO

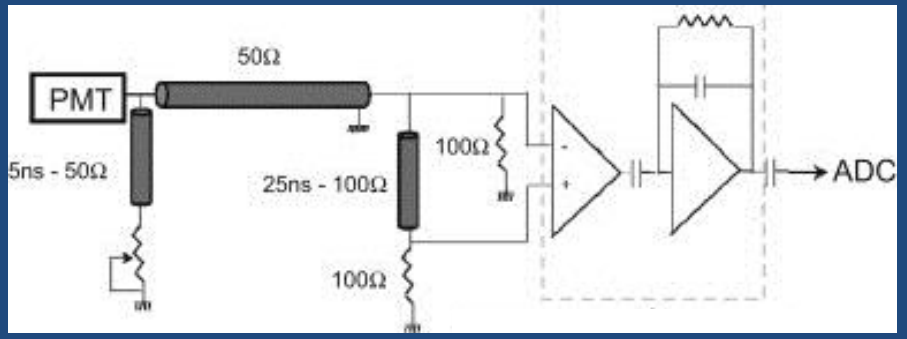


Non-uniform occupancy scale-able links

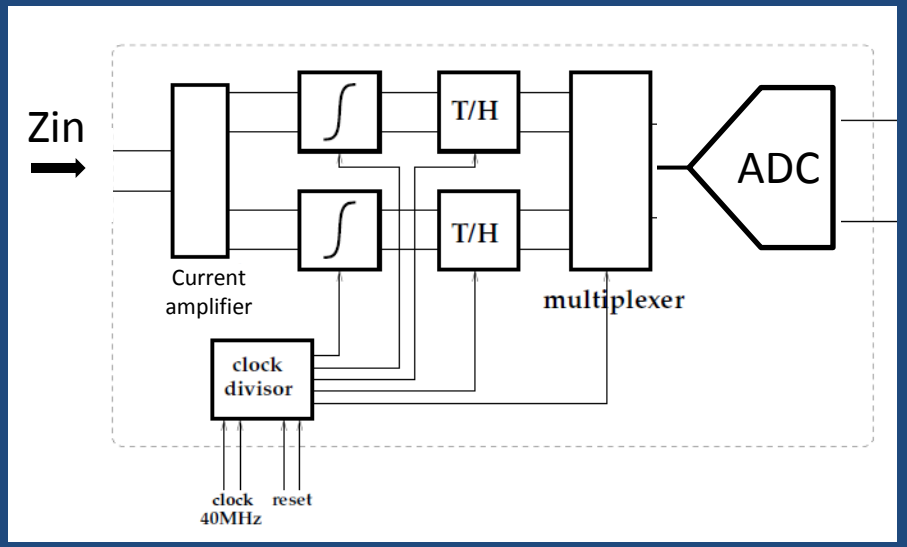


Calorimeter (ECAL/HCAL)

Current LHCb:
Remove deadtime by clipping signals



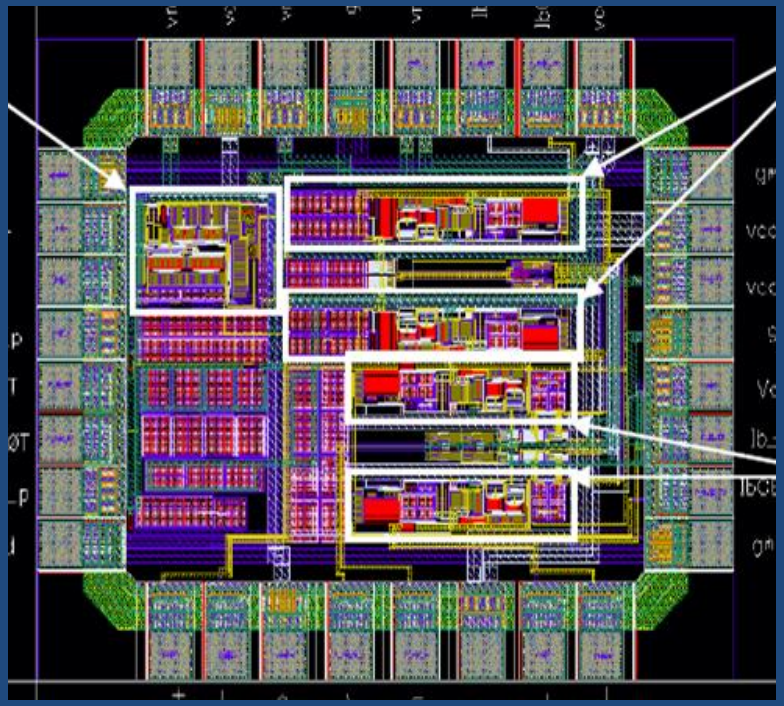
Upgrade:
Reduce gain of PMT (to increase lifetime)
⇒ remove clipping: it decreases signal
⇒ reduce noise by removing Rterm



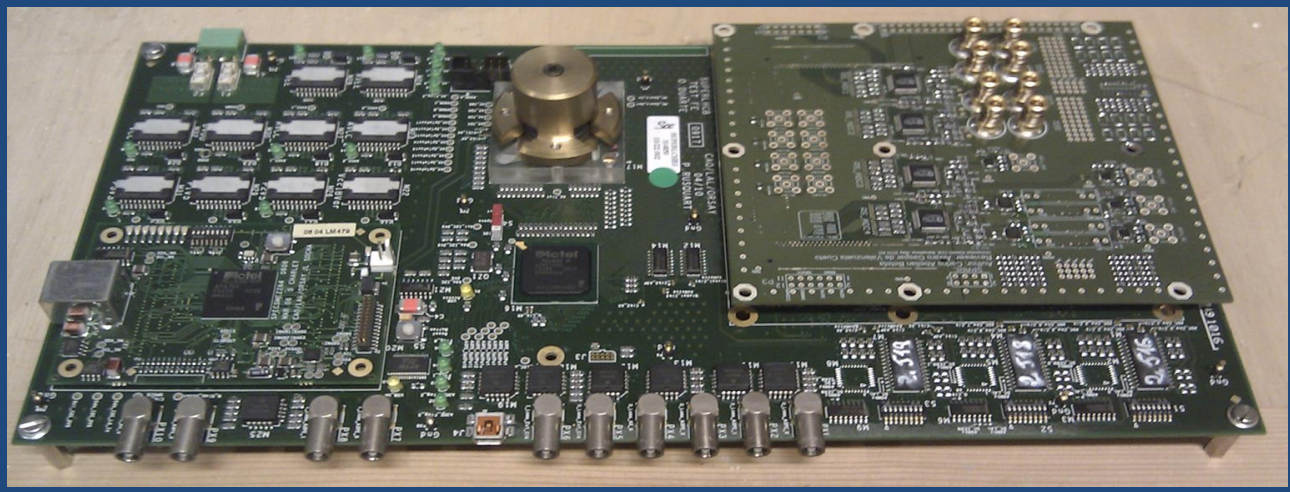
Active termination in ICECAL ASIC

Switched integrators: no deadtime
used successfully in LHCb PS/SPD calo

ICECAL ASIC in 0.35μm



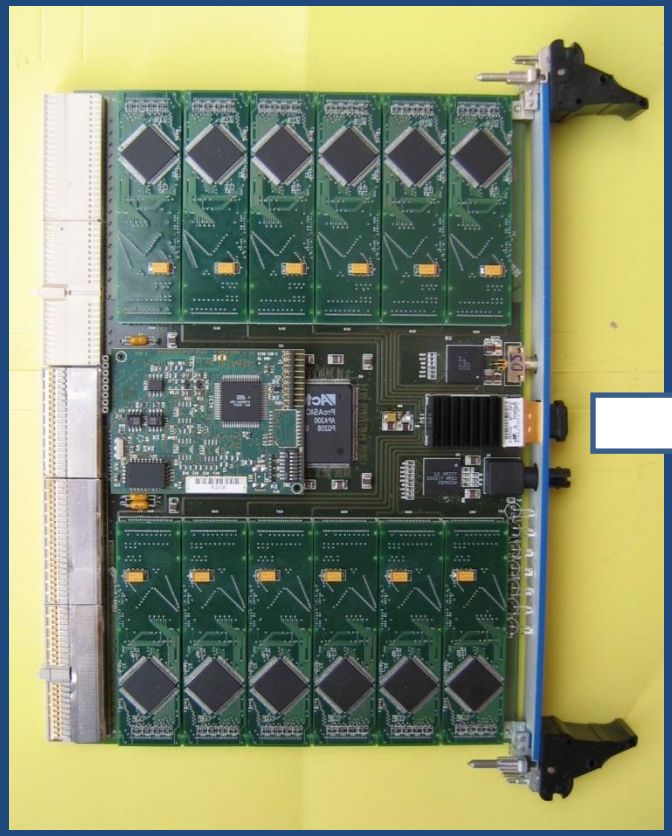
Digital in flash-FPGA



Muons

Default: OK for 40 MHz operation

Front-end ASICs on chambers (CARIOCA + DIALOG)



Questions on obsolescence

Studies on upgrade started

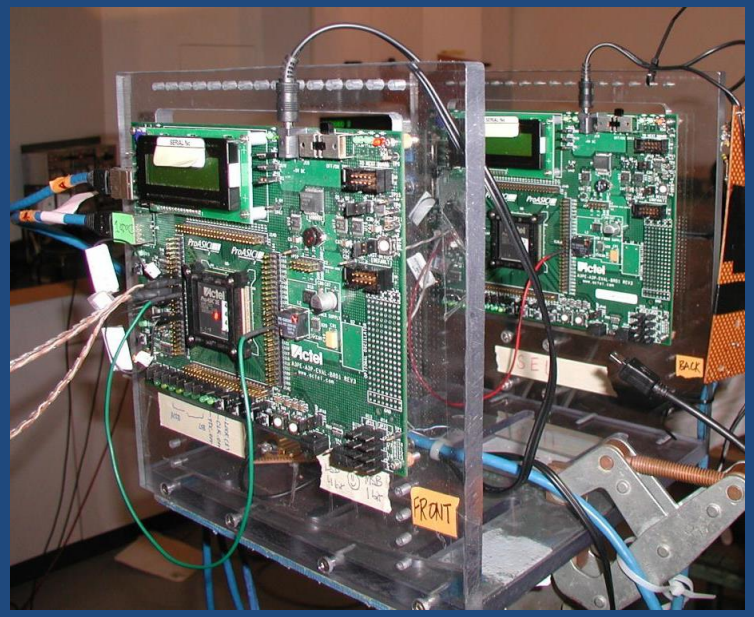
40 MHz data to trigger

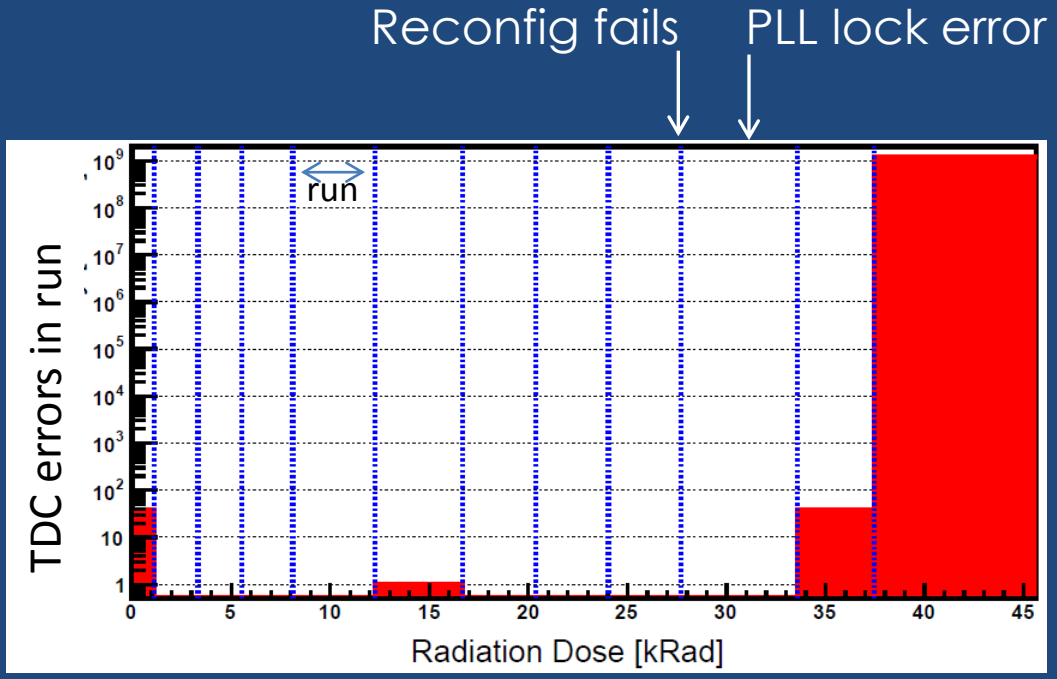
FPGAs in front-end

Big advantage: re-programmeability
=> tune algorithms
=> scale system

Good past experience with flash FPGAs (ACTEL/MICROSEMI)

Irradiation program with full TDC code, 320MHz from internal PLL

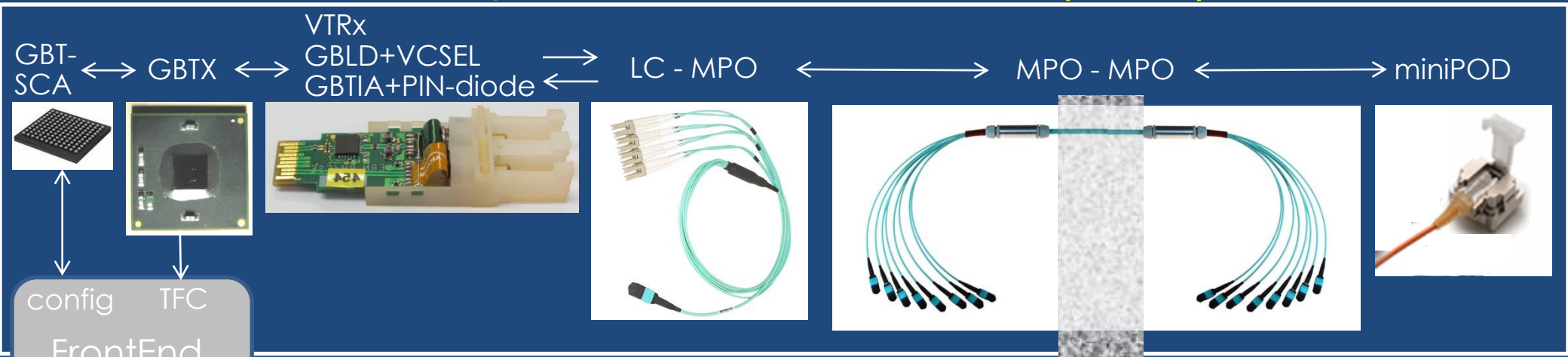




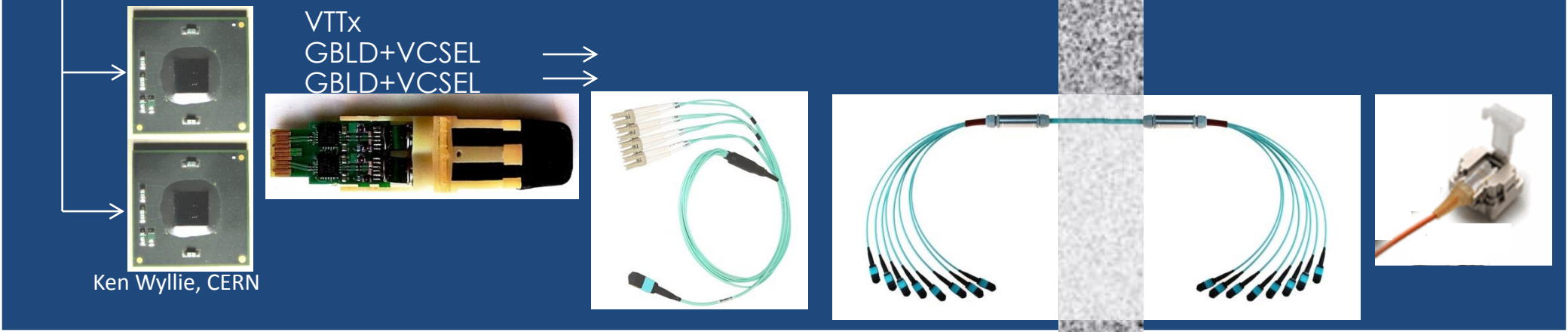
Detector Links, optical: 4.8 Gbit/s

Generic Link: GBT chips + Versatile Link + commercial components

Duplex Master Control Link (2,500)



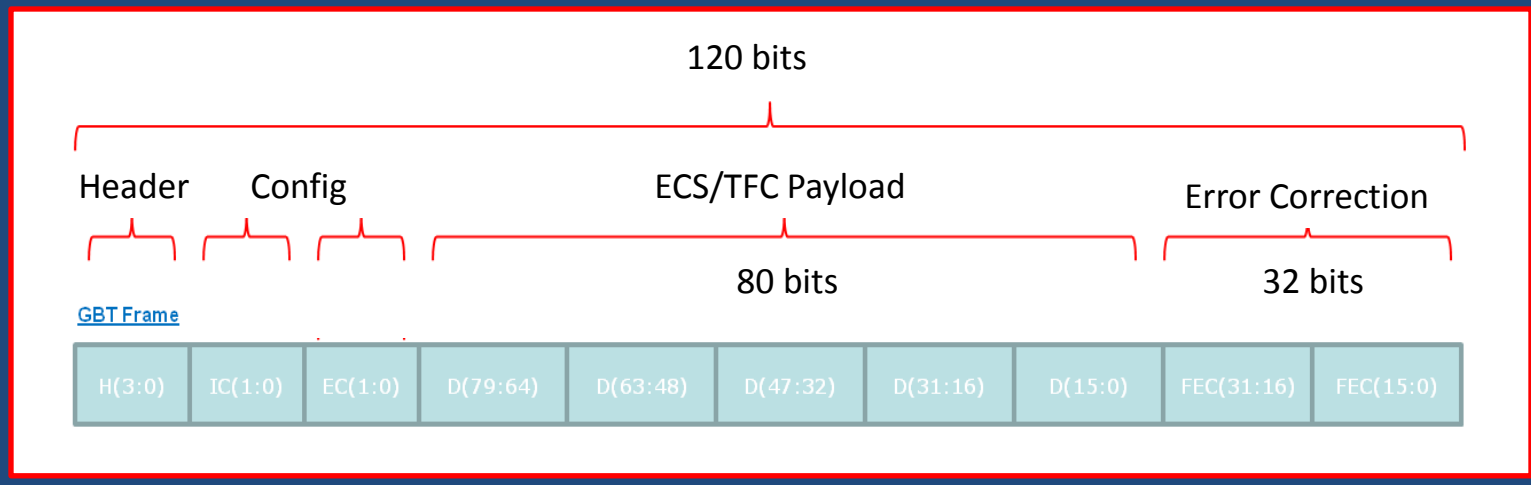
Simplex Data Link (12,500)



Ken Wyllie, CERN

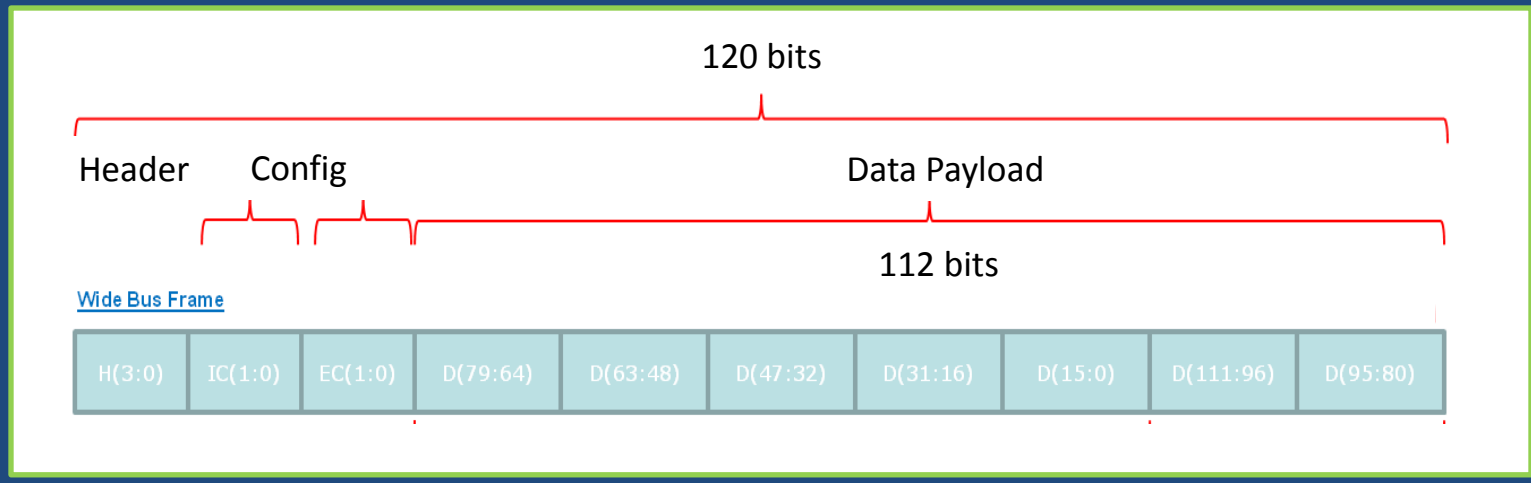
Master Link:
Bandwidth not critical
Robustness is critical:
Use GBT protocol with error correction

3.2 Gbit/s

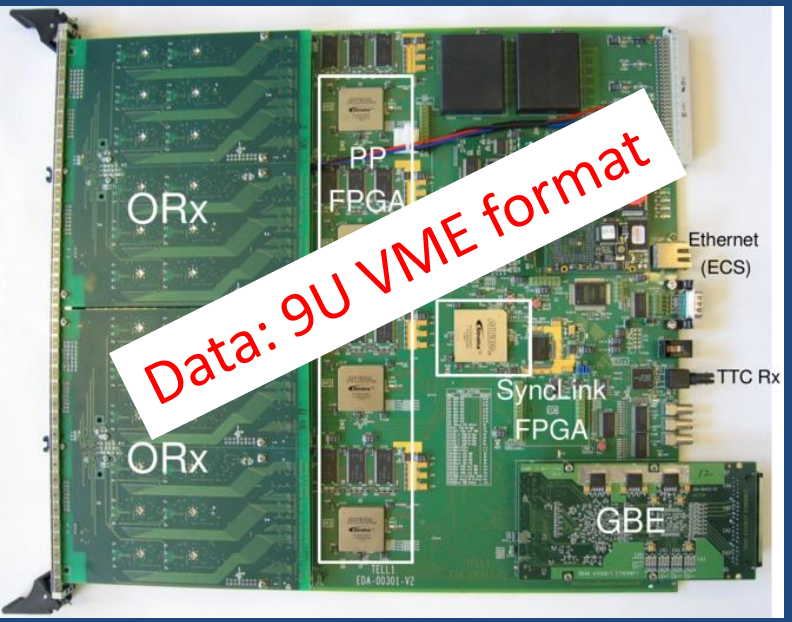


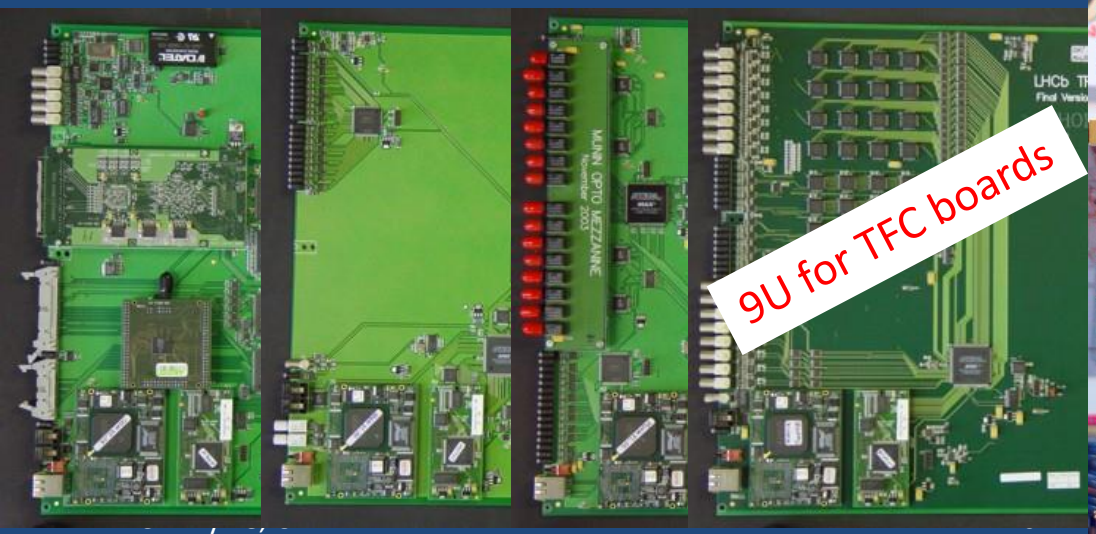
Data link:
Bandwidth may be critical.
If robustness not at risk, use GBT 'wide-bus' mode

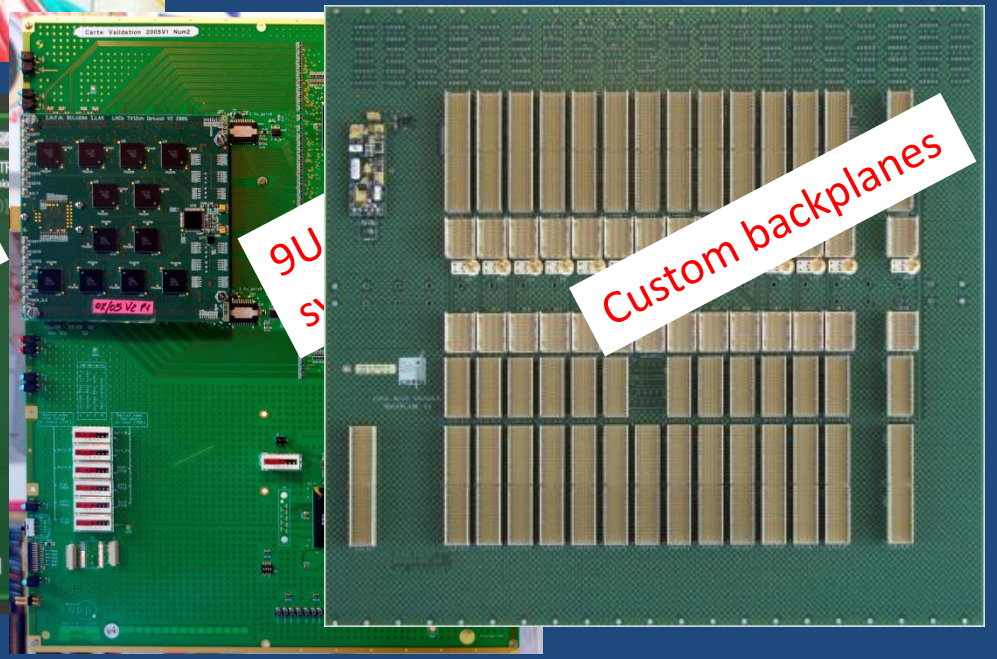
4.48 Gbit/s



Back-end boards in LHCb







New readout board

GOAL: Generic hardware for many tasks:

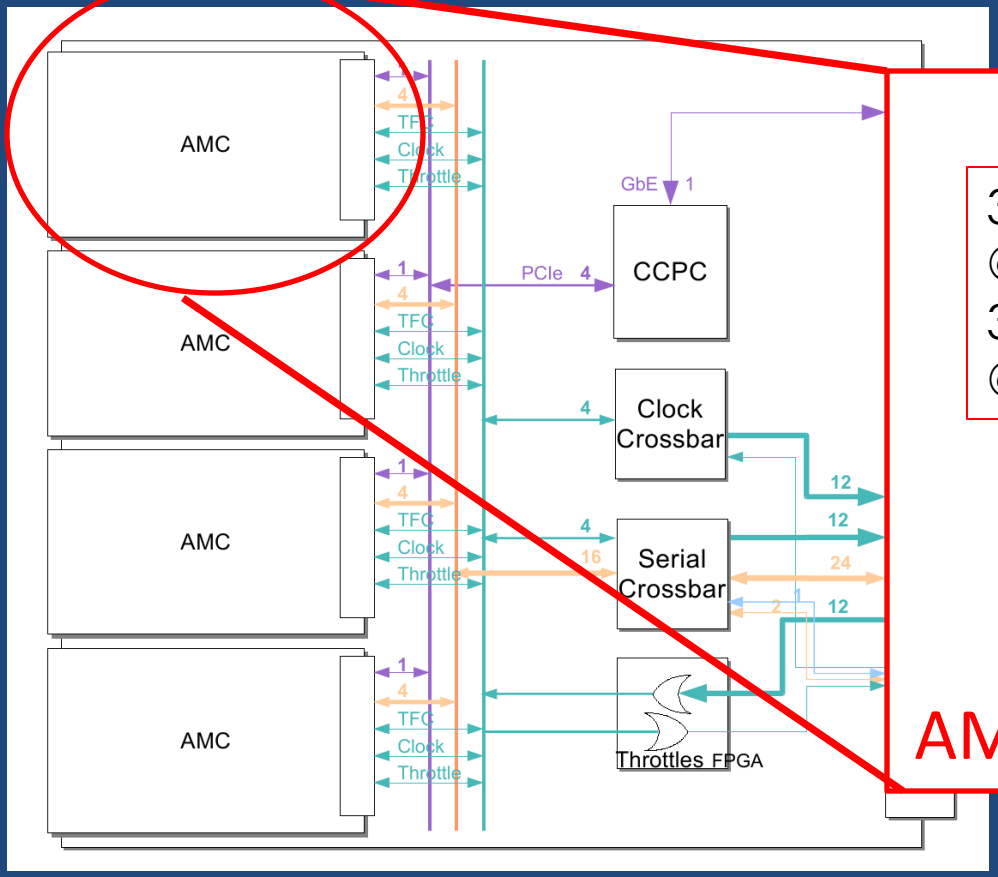
- TELL40 for Data
- SOL40 for ECS/TFC
- TRIG40 for LLT

each with different firmware flavours

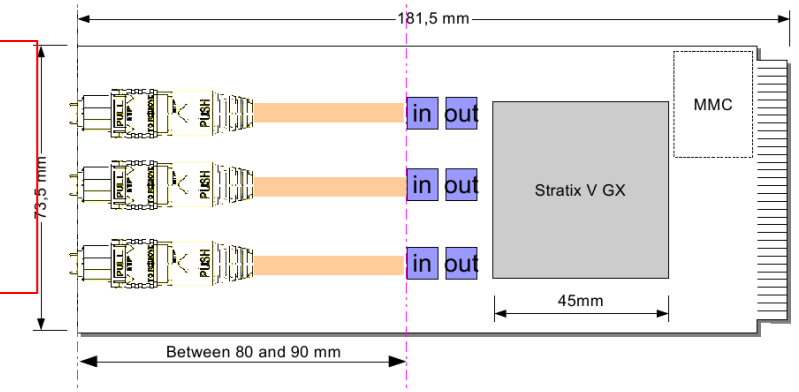
Choice of ATCA + mezzanine approach

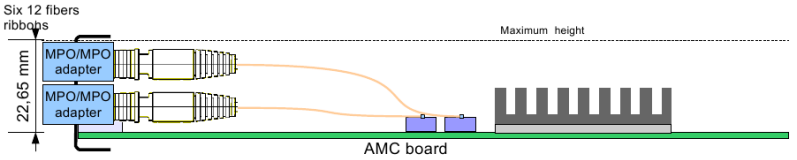
ATCA: a 'standard' (but maybe too flexible….)
redundancy
comprehensive control (maybe too much!)
high speed standard backplane

Hardware



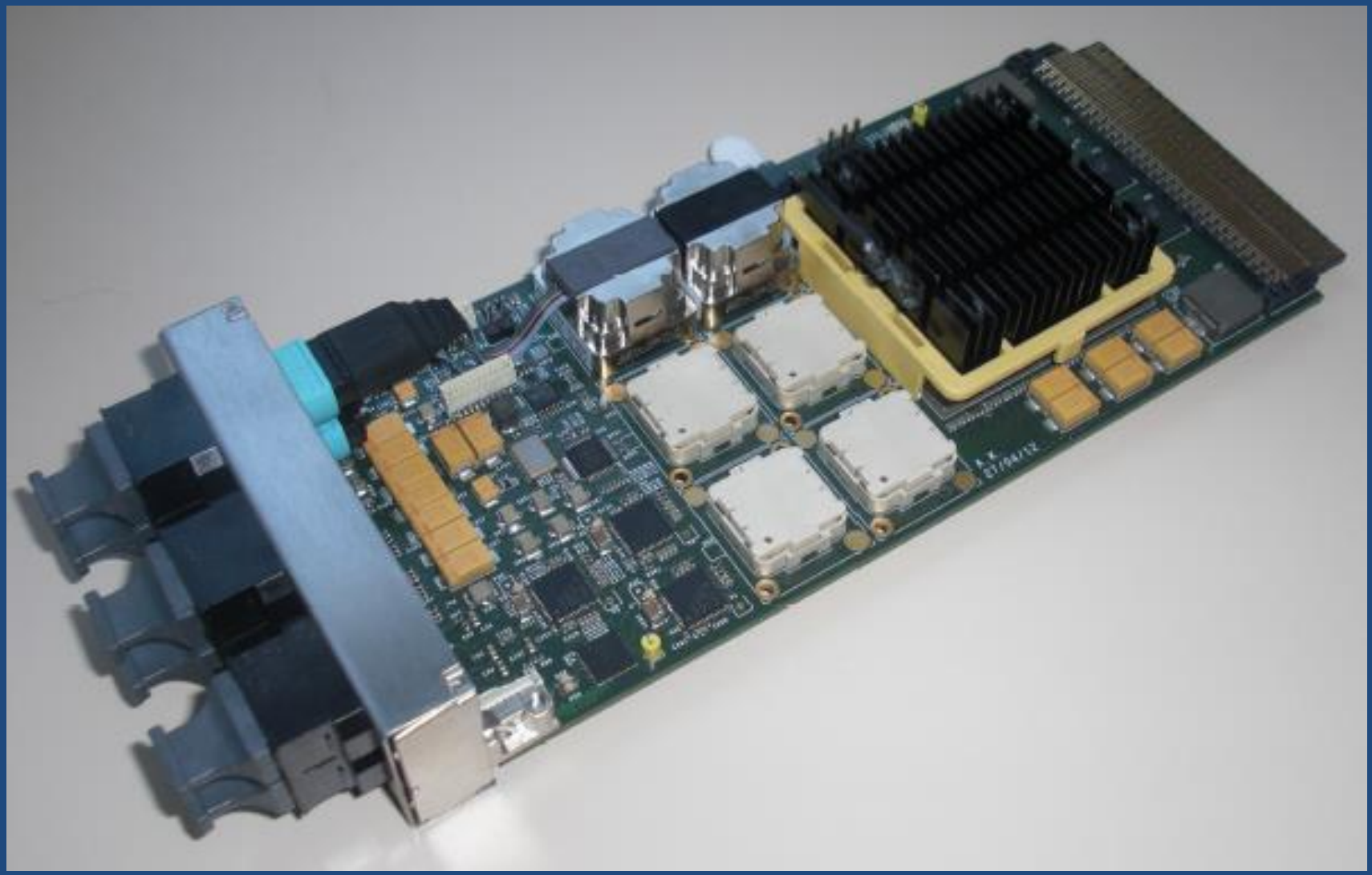
36 inputs
@ 10Gb
36 outputs
@ 10Gb



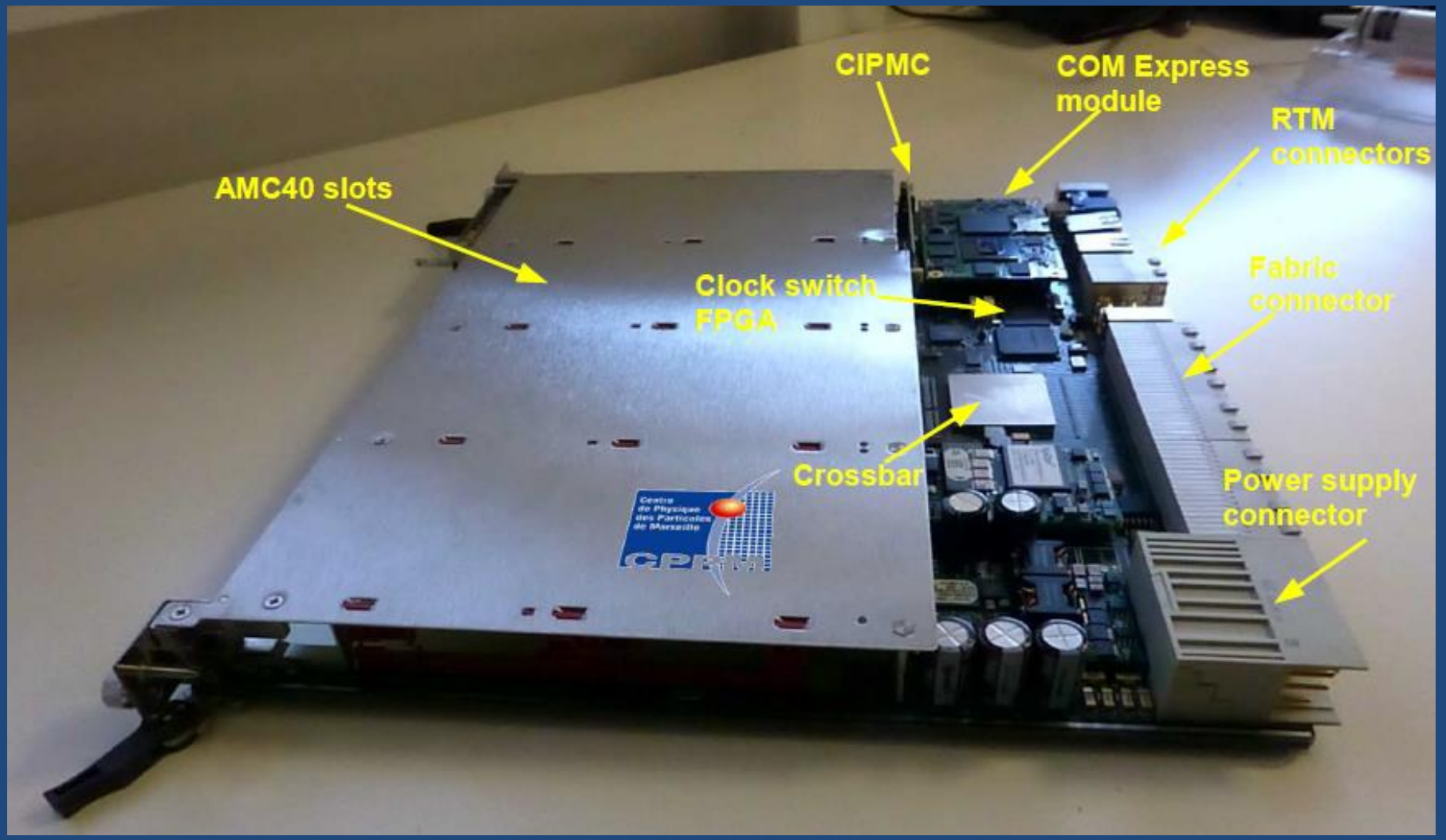


AMC

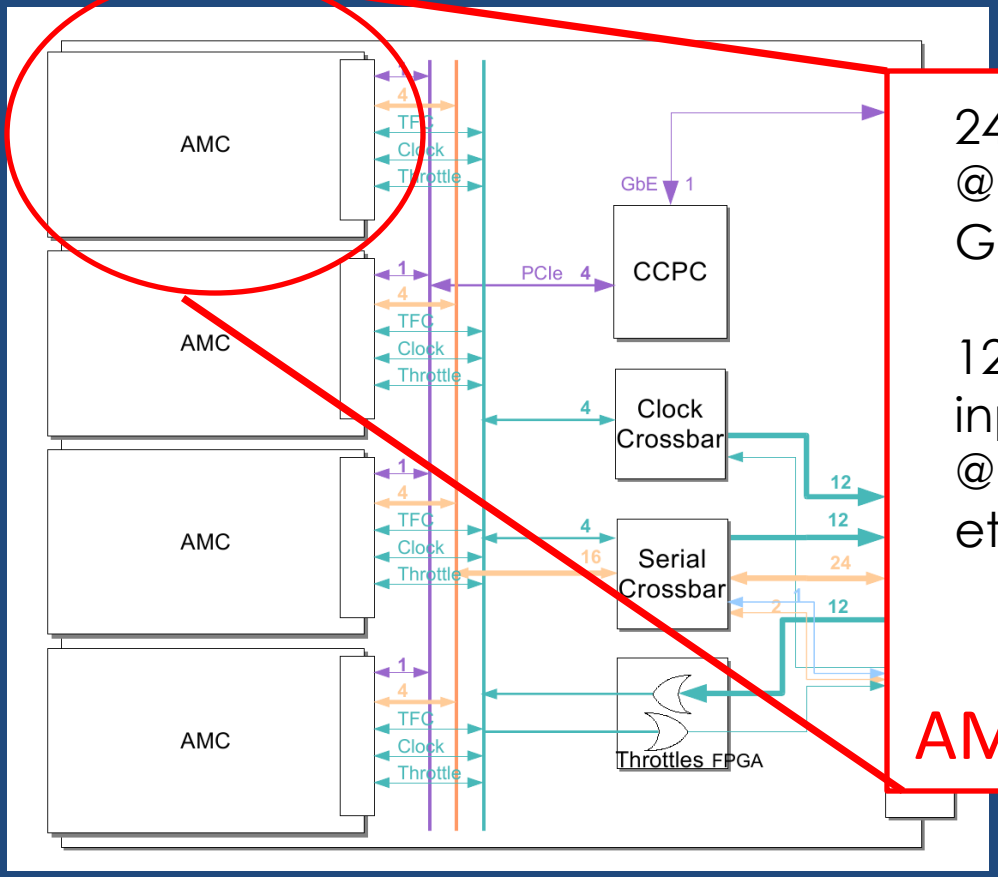
AMC40



ATCA40

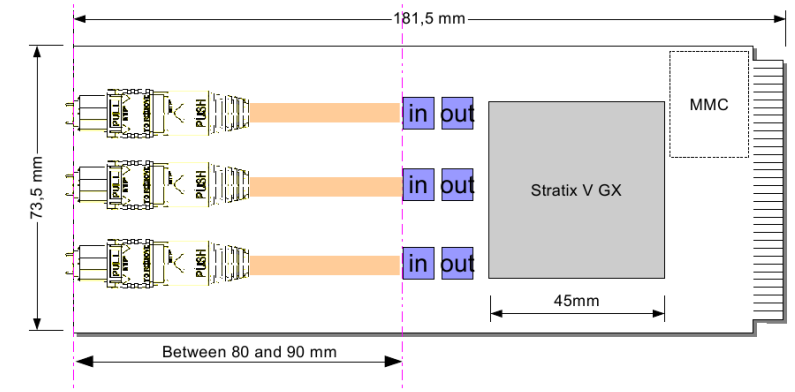

CIPMC
COM Express module
RTM connectors
AMC40 slots
Clock switch FPGA
Fabric connector
Crossbar
Power supply connector

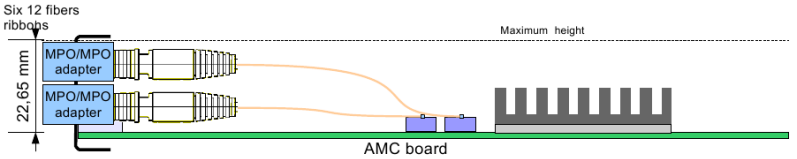
Example: TELL40



24 inputs
@ 4.8 Gb
GBT format

12 outputs/
inputs
@ 10Gb
ethernet

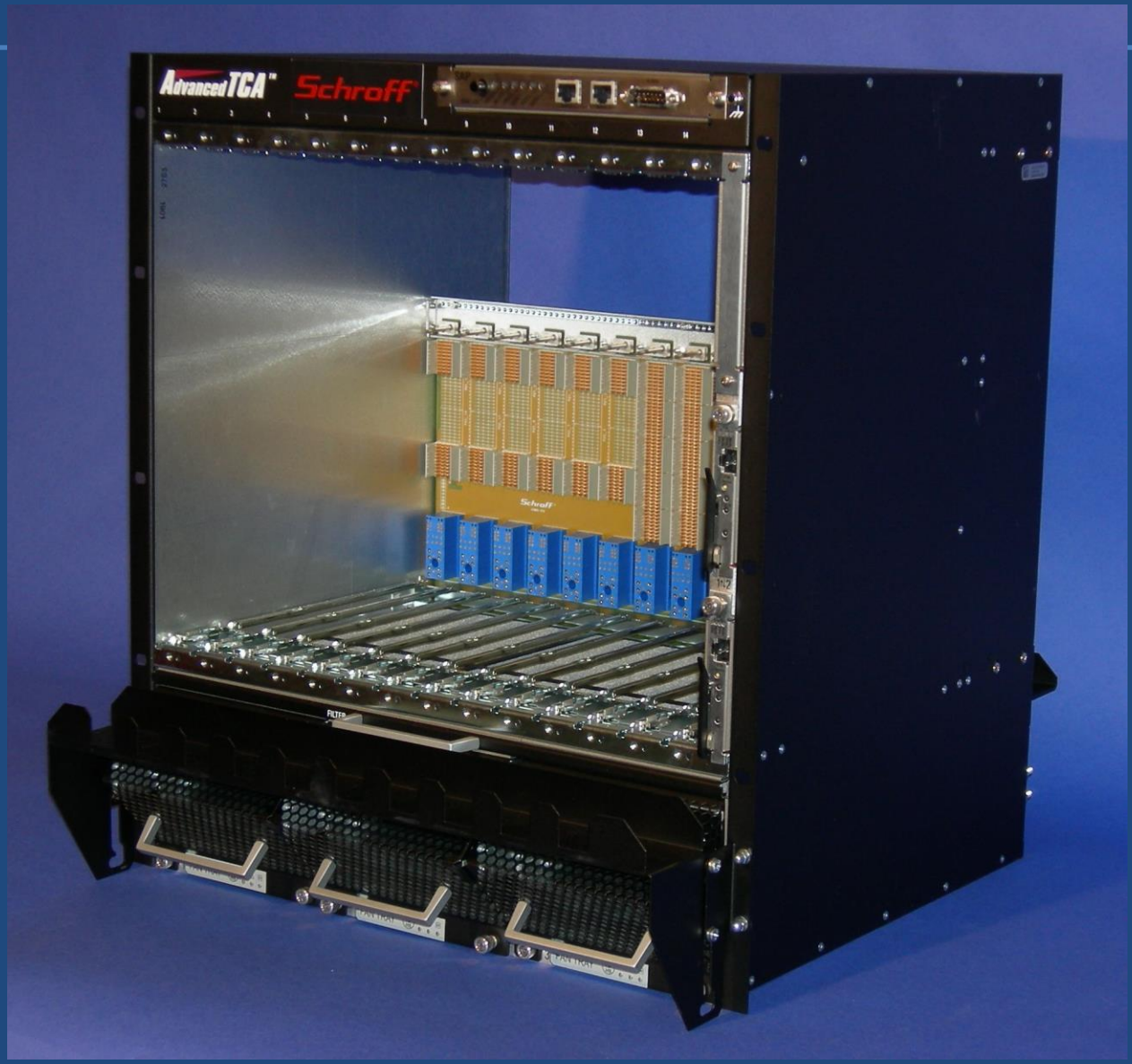




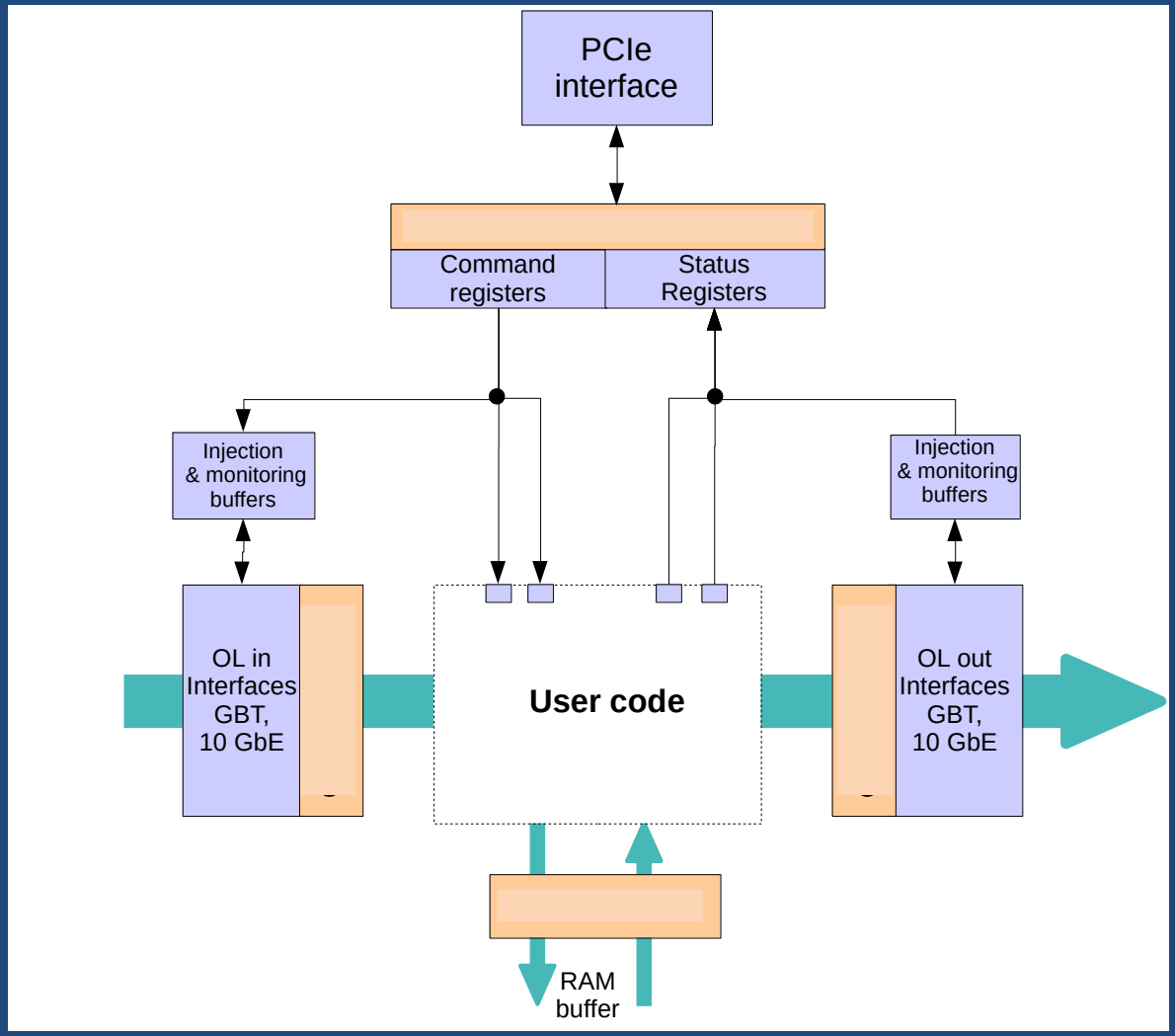
AMC

96 inputs @ 4.8 Gb ➡ processing in FPGA ➡ 48 10G ethernet ports

ATCA crate mechanics



TELL40 firmware



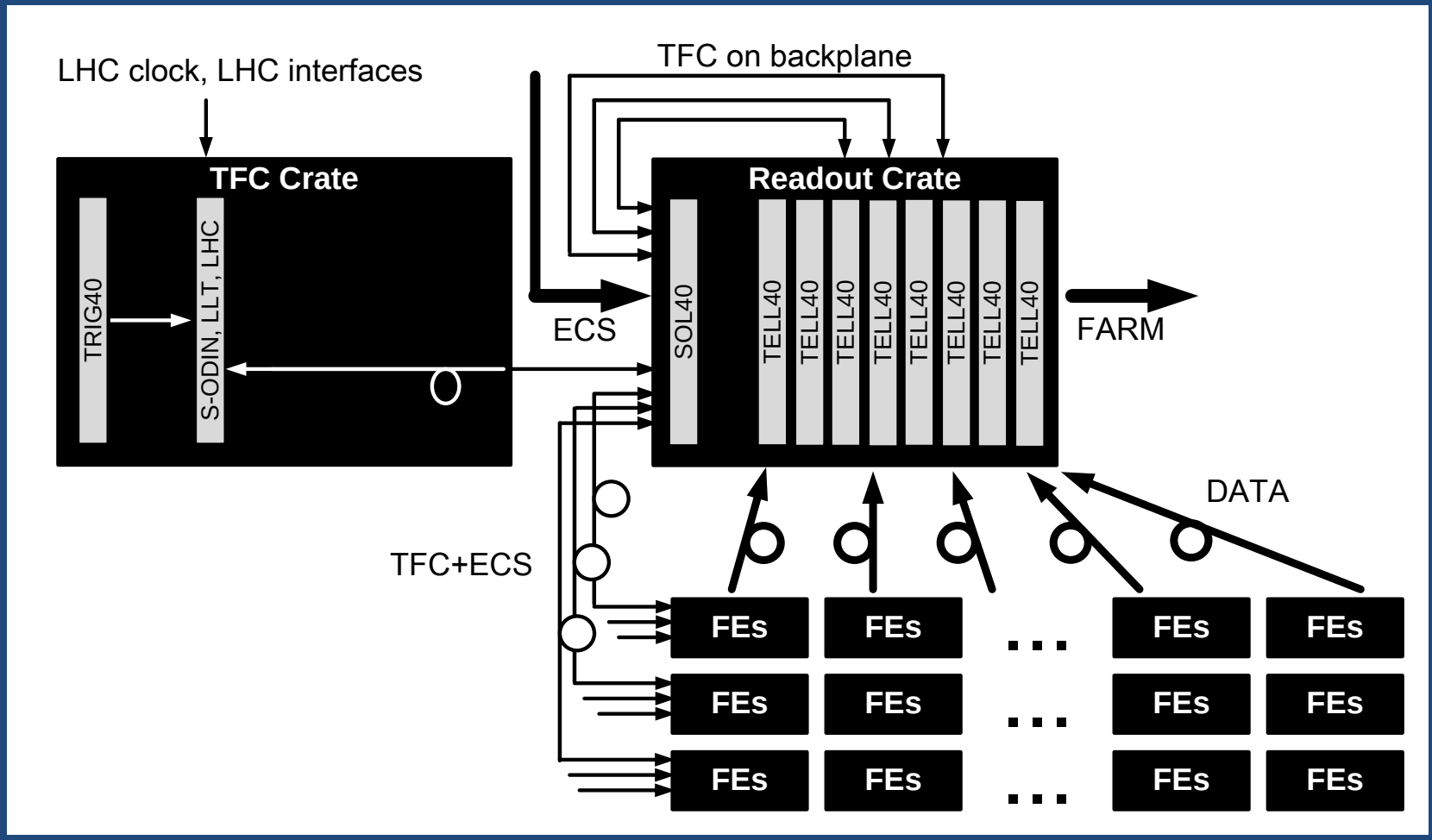
Project across many groups

Centrally coordinated

Common interfaces

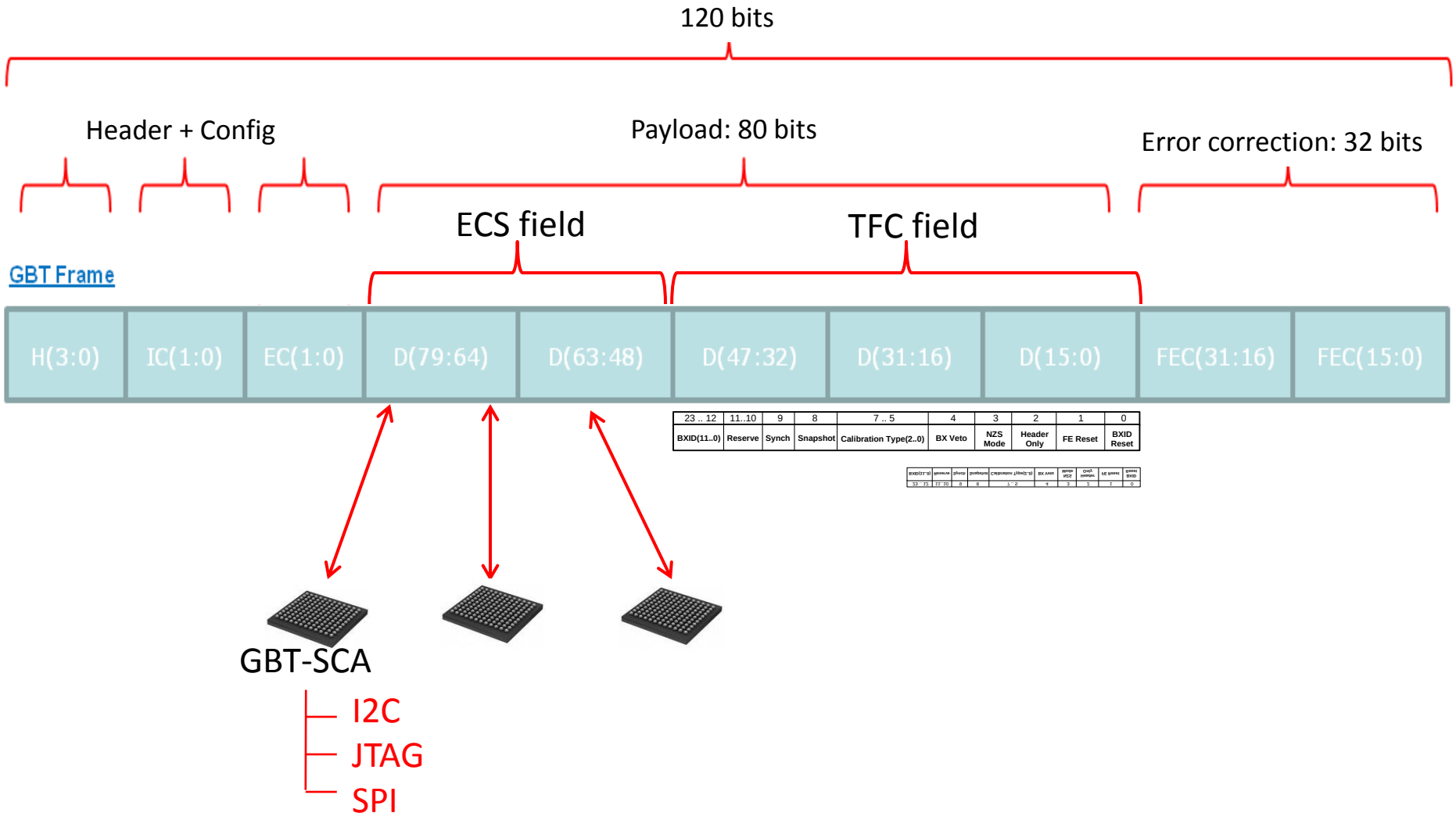
User code for data processing

TFC + ECS via SOL40



23 .. 12	11..10	9	8	7 .. 5	4	3	2	1	0
BXID(11..0)	**Reserve**	**Synch**	**Snapshot**	**Calibration Type(2..0)**	**BX Veto**	**NZS Mode**	**Header Only**	**FE Reset**	**BXID Reset**

ECS (slow controls)



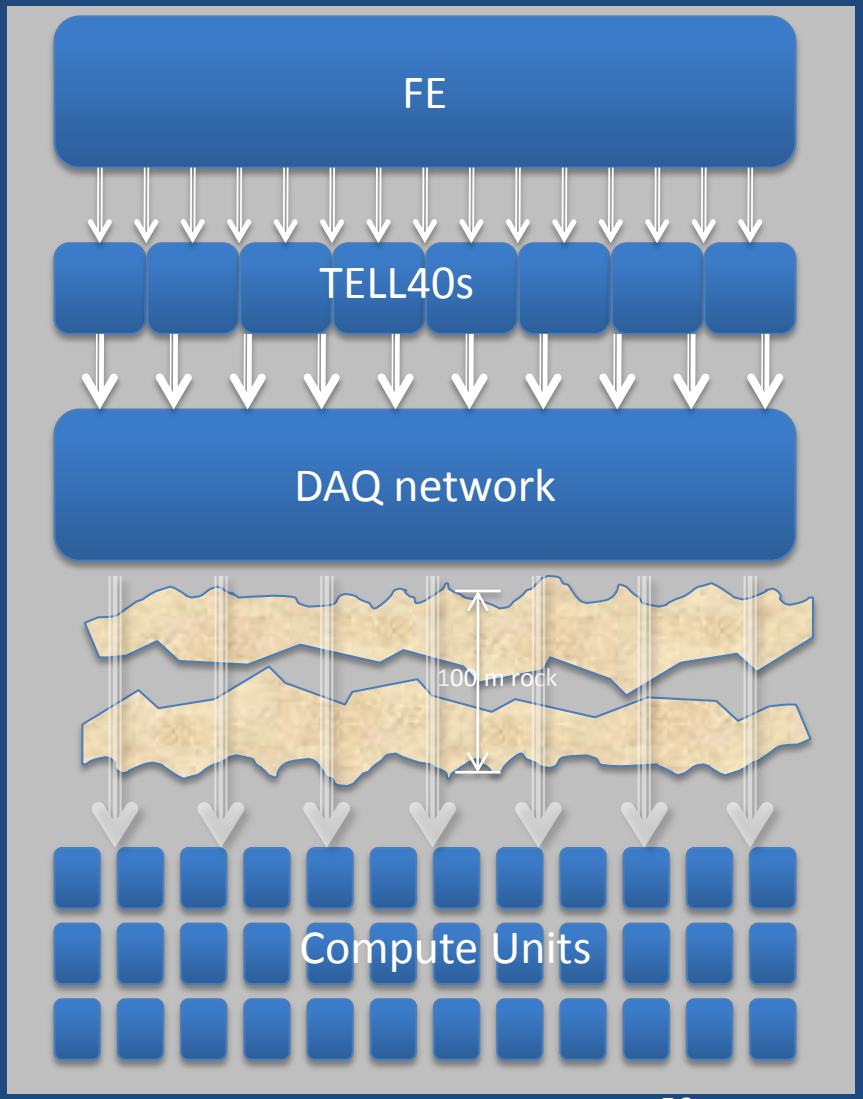
23 .. 12	11..10	9	8	7 .. 5	4	3	2	1	0
BXID(11..0)	Reserve	Synch	Snapshot	Calibration Type(2..0)	BX Veto	NZS Mode	Header Only	FE Reset	BXID Reset

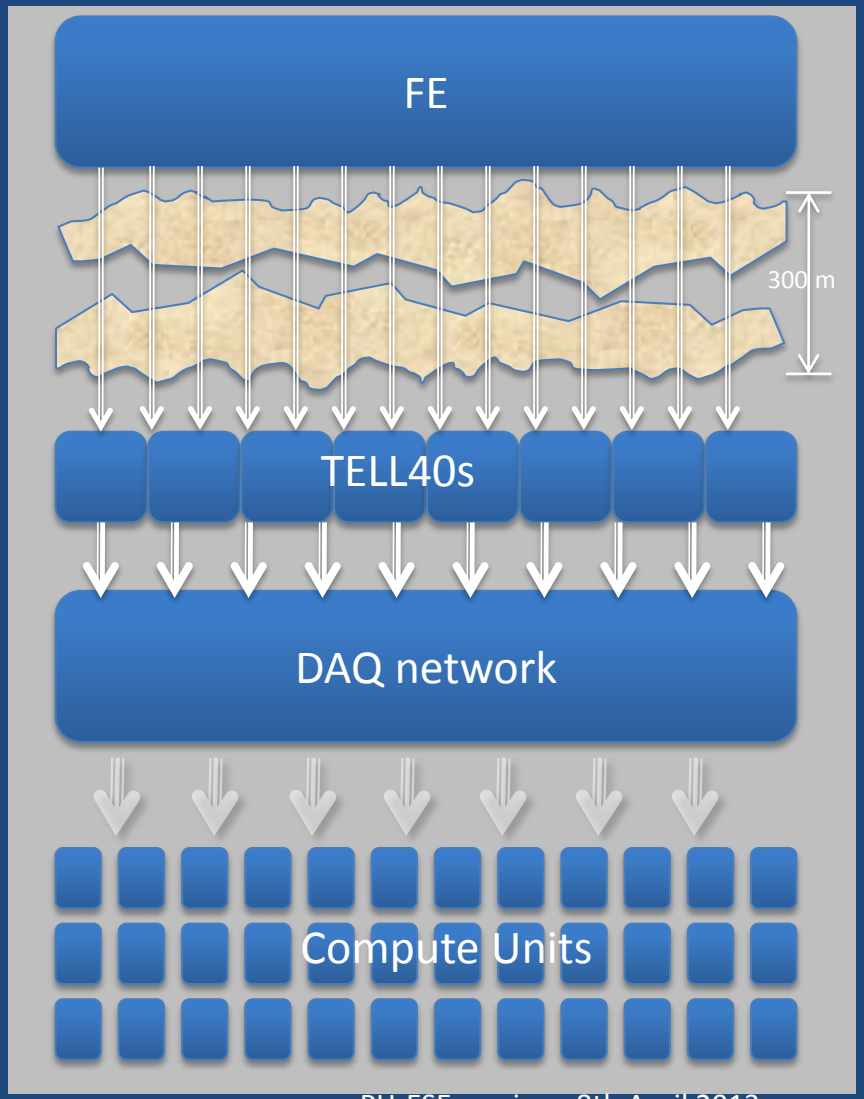
Long distance transmission?

4.8 Gbit/s

10/40 Gbit/s Ethernet or Infiniband

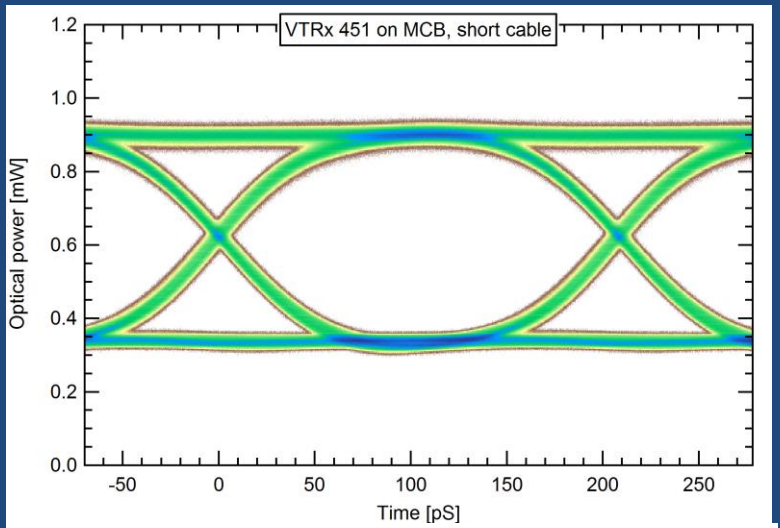
100 Gbit/s Ethernet or Infiniband

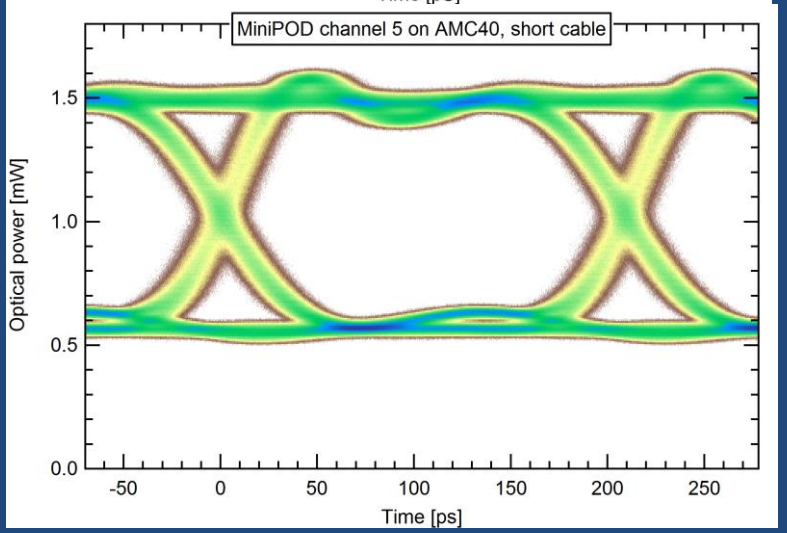




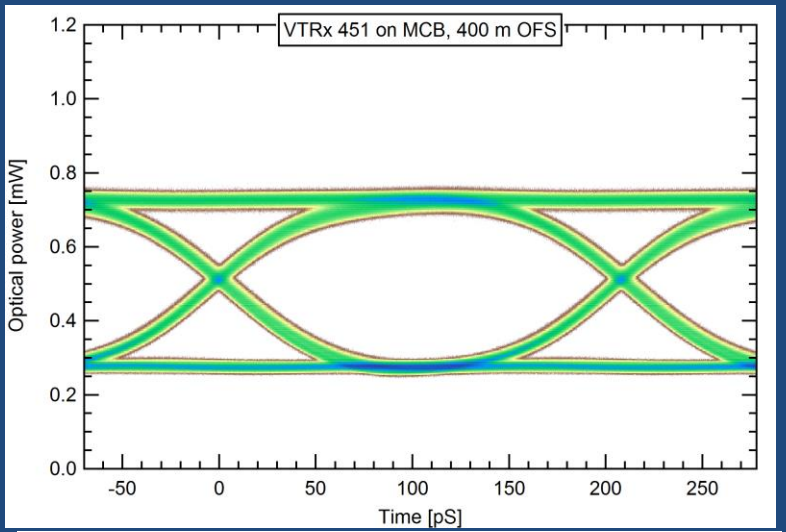
Long distance transmission?

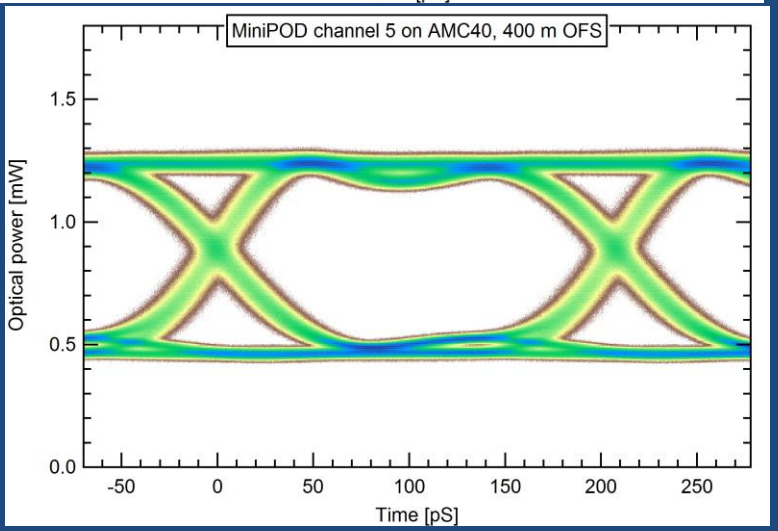
Short fibre



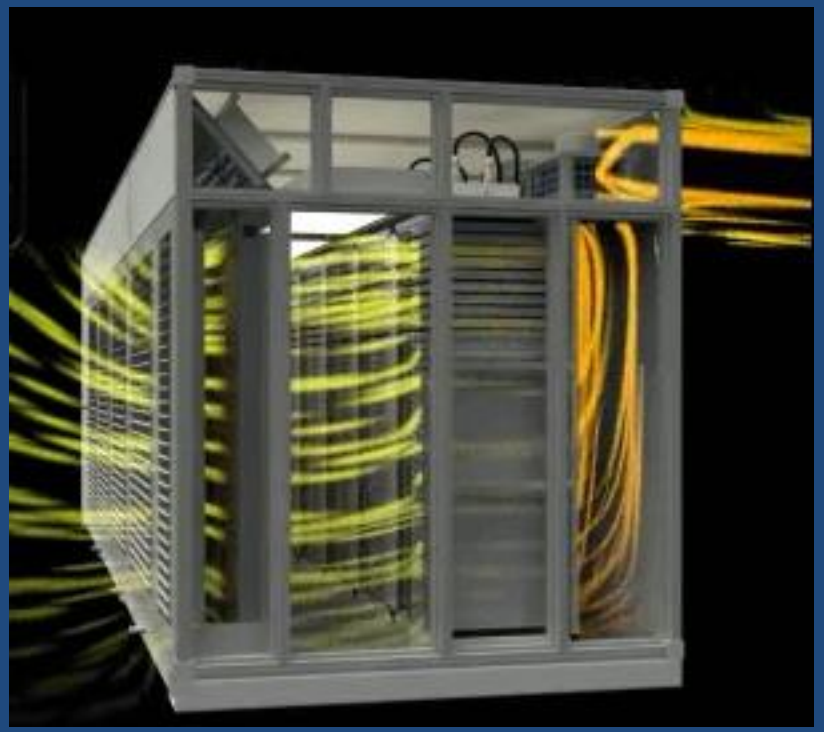


400m OM4 fibre





All data in a box



Schedule

- in 2018/19: installation (18 months according to planning!)
- 2016-17: quality control & acceptance tests
- 2014-16: tendering & serial production
- Q3/Q4 2013: TDRs & prototype validation
- Q1/Q2 2013: technical reviews & choice of technologies

✓ 2012/2013: continue R&D towards technical choices

✓ 2012: "Framework TDR" submitted & endorsed

✓ June 2011: LoI submitted & encouraged to proceed to TDRs

Conclusions

Good motivation for upgrade

Clear architecture concept
with many common items

We are happy to use new generic developments
(in fact, we rely on them!)

Implementation is now

Manpower is a crucial issue……

Our schedule is tight…….

References

LHCC-2008-007 (Expression of Interest)
LHCC-2011-001 (Letter of Intent)
LHCC-2012-007 (Framework TDR)